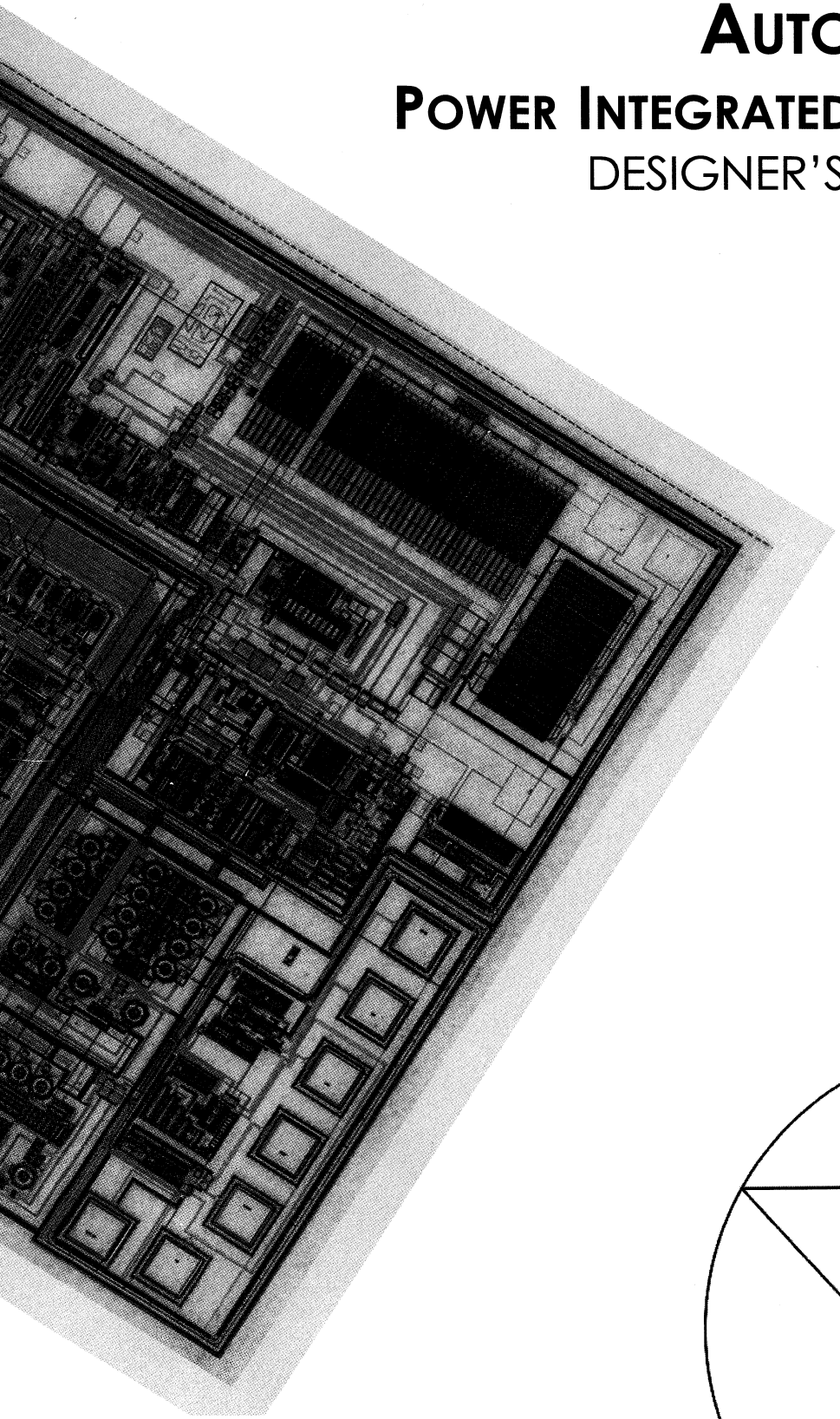
AUTOMOTIVE
POWER INTEGRATED CIRCUIT
DESIGNER'S MANUAL



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IOR Rectifier

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Automotive Power Integrated Circuit
Designer's Manual

from International Rectifier

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				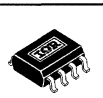	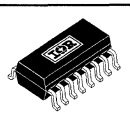	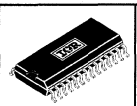	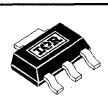	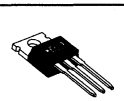		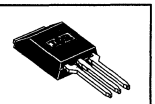
Topology	Rds(on) @25°C (mΩ)	Over-current protection	Over-temperature protection (165°C)	8 Lead SOIC Narrow Body	16 Lead SOIC Narrow Body	28 Lead SOIC WideBody	SOT223	TO220	SMD220	Super220
Low Side	5	100A Isd (latched)	latched							**IPS0551T(C)**
	25	35A Isd (latched)	latched					**IPS0151(C)**	**IPS0151S(C)**	
	60	12A Isd (latched)	latched					**IPS031(C)**	**IPS031S(C)**	
	70	12A Isd (latched)	latched	**IPS031G(C)**						
	150	5A Isd (latched)	latched				**IPS021L(C)**	**IPS021(C)**	**IPS021S(C)**	
	200	5.5A limit (linear)	hysteretic				**IRSF3021L(C)**	**IRSF3021(C)**		
		4A Isd (latched) dual input Vth	latched				**IRSF3031L(C)**	**IRSF3031(C)**		
	500	2A Isd (latched)	latched				**IPS041L(C)**			
Low Side (2 channels)	70	12A Isd (latched)	latched		**IPS032G(C)**					
	150	5A Isd (latched)	latched	**IPS022G(C)**						
	500	2A Isd (latched)	latched	**IPS042G(C)**						
Low Side (4 channels)	150	5A Isd (latched)	latched		**IPS024G(C)**					
High Side	5	100A Isd (latched)	latched							**IPS5551T(C)**
	25	35A Isd (latched)	hysteretic					**IPS5451(C)**	**IPS5451S(C)**	
	80	10A limit (linear)	hysteretic					**IPS521(C)**	**IPS521S(C)**	
	100	10A limit (linear)	hysteretic	**IPS521G(C)**						
		10A limit (PWM)	hysteretic					**IR6220(C)**	**IR6220S(C)**	
		20A limit (PWM)	hysteretic					**IR6224(C)**	**IR6224S(C)**	
		20A limit (linear)	hysteretic					**IR6226(C)**	**IR6226S(C)**	
	130	5A limit (linear)	hysteretic					**IPS511(C)**	**IPS511S(C)**	
	150	5A limit (linear)	hysteretic	**IPS511G(C)**						
	200	5A limit (PWM)	hysteretic					**IR6210(C)**	**IR6210S(C)**	
		10A limit (linear)	hysteretic					**IR6216(C)**	**IR6216S(C)**	
High Side (2 channels)	150	5A limit (linear)	hysteretic		**IPS512G(C)**					

Application Selection Codes	**Automotive**
	C

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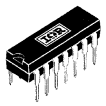
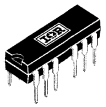
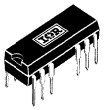
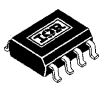
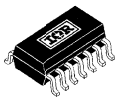
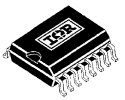
Automotive IC Navigator

IOR International Rectifier

MOSFET GATE DRIVERS

Function	Features	Voltage Offset	8 Lead DIP	14 Lead DIP	14 Lead DIP w/o Lead 4	16 Lead DIP w/o Leads 4 & 5	8 Lead SOIC Narrow Body	14 Lead SOIC Narrow Body	16 Lead SOIC Wide Body
Dual Low Side	basic	n/a	IR4426 IR4427 IR4428				IR4426S IR4427S IR4428S		
High Side	Overcurrent shutdown	600	IR21271				IR21271S		
Independent High & Low Side	Basic	600	IR2181 IR2186				IR2181S IR2186S		
	Basic w/ Separate Logic/Power Grounds	600		IR21814				IR21814S	
	Shutdown & separate logic supply	500		IR2110	IR2110-1	IR2110-2			IR2110S
		600		IR2112 IR2113	IR2112-1 IR2113-1	IR2112-2 IR2113-2			IR2112S IR2113S
Half-Bridge	Basic	600	IR2183 IR2184 IR2189				IR2183S IR2184S IR2189S		
	Shutdown & Adjustable Deadtime	600		IR21834 IR21844				IR21834S IR21844S	
	Application Selection Codes		Automotive  C						

5/00

SPECIAL FUNCTION IC's

Function	Features	Voltage Offset	8 Lead DIP	8 Lead SOIC Narrow Body	16 Lead SOIC Wide Body	20Lead SOIC Wide Body	TO220	SMD220
LINEAR CURRENT SENSING IC motor phase current sensing through an external shunt resistor. A/D conversion with level shifting	Basic	600	**IR2171**	**IR2171S**	**IR21716S**			
	Overcurrent trip signal	600	**IR2172**	**IR2172S**	**IR21726S**			
PROGRAMMABLE CURRENT SENSING HIGH SIDE SWITCH A fully protected high side switch with linear current feedback and a programmable current shutdown	Basic	40					**IR3310**	**IR3310S**
FULLY PROTECTED H-BRIDGE FOR DC MOTOR. Over-current and over-temperature protected. It is a complete H-bridge with PWM soft-start sequence, braking mode, and sleep mode	Basic	40				**IR3220S**		
	Application Selection Codes		**Automotive**  **C**					

IPS DATA SHEETS

IPS DATA SHEETS

IPS DATA SHEETS

International
IOR Rectifier

Data Sheet No.PD60144-I

IPS0151/IPS0151S

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

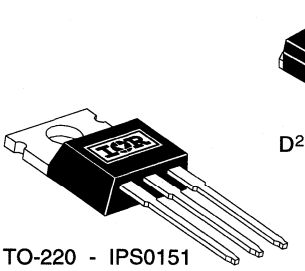
Description

The IPS0151/IPS0151S are fully protected three terminal SMART POWER MOSFETs that feature over-current, over-temperature, ESD protection and drain to source active clamp.These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 35A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

Product Summary

$R_{ds(on)}$	25mΩ (max)
V_{clamp}	50V
Ishutdown	35A
T_{on}/T_{off}	1.5µs

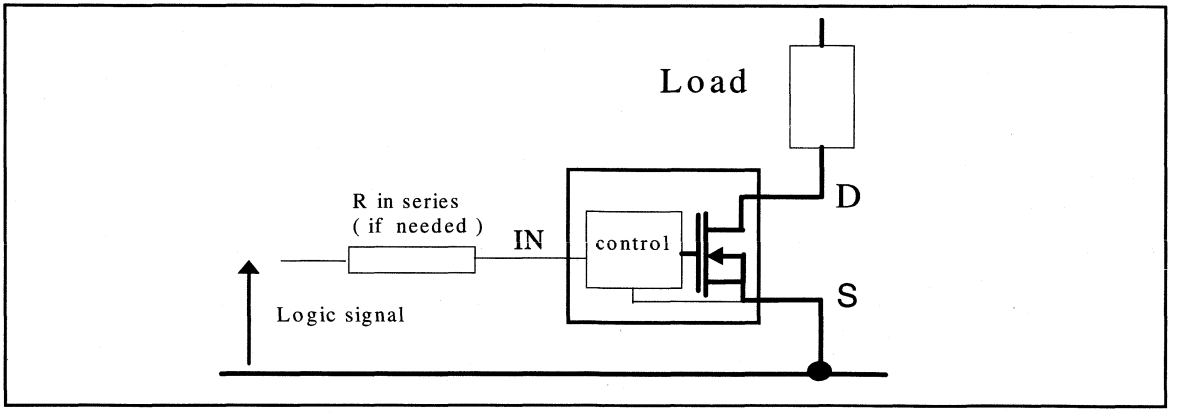
Packages



D²Pak (SMD220)
IPS0151S

TO-220 - IPS0151

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum Input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	rth=62°C/W IPS0151	—	2.8		TO220 free air
	rth=5°C/W IPS015135	—	35		TO220 with Rth=5°C/W
	rth=80°C/W IPS0151S	—	2.2		SMD220 Std footprint
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	45		
P_d	Maximum power dissipation(1)			W	
	(rth=62°C/W) IPS0151	—	2		
	(rth=80°C/W) IPS0151S	—	1.56		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance free air	—	55	—	°C/W	TO-220
R_{th} 2	Thermal resistance junction to case	—	60	—		
R_{th} 1	Thermal resistance with standard footprint	—	60	—		D^2PAK (SMD220)
R_{th} 2	Thermal resistance with 1" square footprint	—	35	—		
R_{th} 3	Thermal resistance junction to case	—	2	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} Tamb=85°C	Continuous drain current			A
	(TAmbient = 85°C, IN = 5V, rth = 60°C/W, Tj = 125°C) IPS0151	—	4.3	
	(TAmbient = 85°C, IN = 5V, rth = 80°C/W, Tj = 125°C) IPS0151S	—	3.8	
R_{in}	Recommended resistor in series with IN pin	0.2	5	kΩ
$T_{r\text{-}in\ (max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	μS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. Notes.

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	10	20	25	mΩ	V_{in} = 5V, I_{ds} = 1A
	T_j = 150°C	—	35	45		
I_{dss1} @Tj=25°C	Drain to source leakage current	0	0.5	25	µA	V_{cc} = 14V, T_j = 25°C
I_{dss2} @Tj=25°C	Drain to source leakage current	0	5	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	47	52	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	55	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to source clamp voltage	7	8.1	9.5		I_{in} = 1 mA
$V_{in\ th}$	IN threshold voltage	1	1.6	2		I_d = 50mA, V_{ds} = 14V
$I_{in,\ -on}$	ON state IN positive current	25	90	200	µA	V_{in} = 5V
$I_{in,\ -off}$	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 3Ω, Rinput = 50Ω, 100µs pulse, T_j = 25°C, (unless otherwise specified).

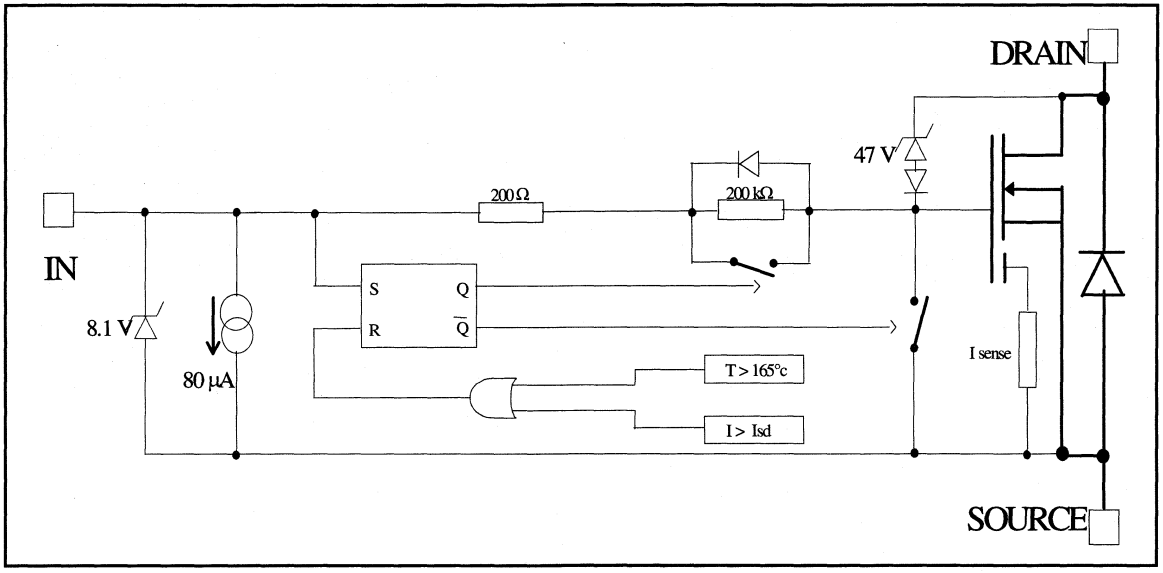
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.05	0.25	0.6	µs	See figure 2
T_r	Rise time	0.2	0.9	1.5		
T_{rf}	Time to (final $R_{ds(on)}$ 1.3%)	—	3.8	—		
T_{off}	Turn-off delay time	0.8	1.5	2		See figure 2
T_f	Fall time	0.4	1.1	2		
Q_{in}	Total gate charge	—	30	—	nC	V_{in} = 5V

Protection Characteristics

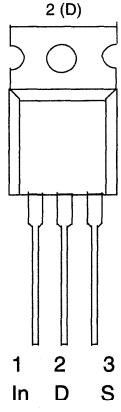
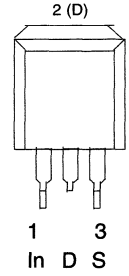
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	20	35	50	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, T_j = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	Vcc = 14V

Functional Block Diagram

All values are typical



Lead Assignments

 TO-220	 D²PAK (SMD220)
IPS0151	**IPS0151S**
Part Number	

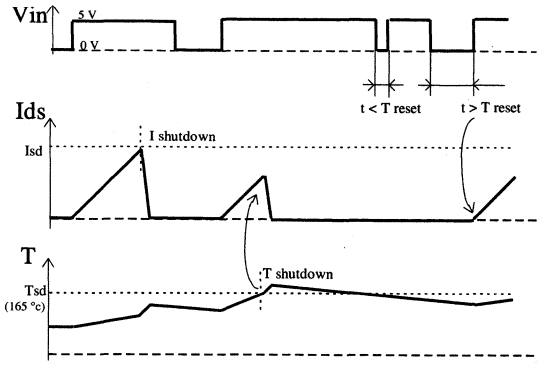


Figure 1 - Timing diagram

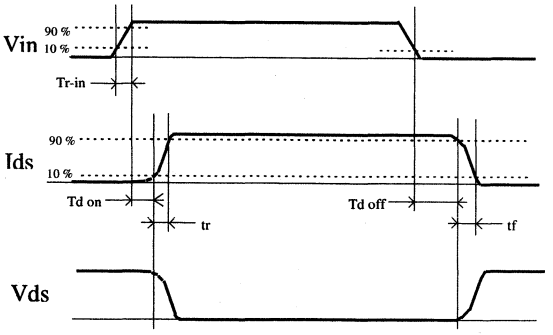


Figure 2 - IN rise time & switching time definitions

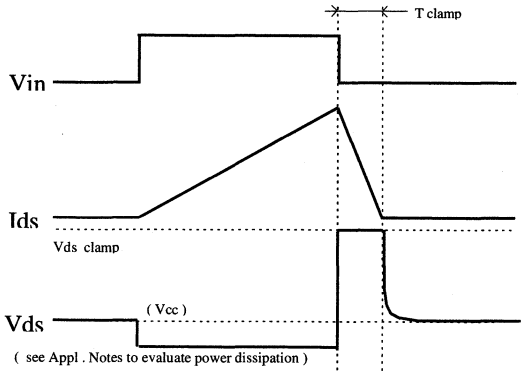


Figure 3 - Active clamp waveforms

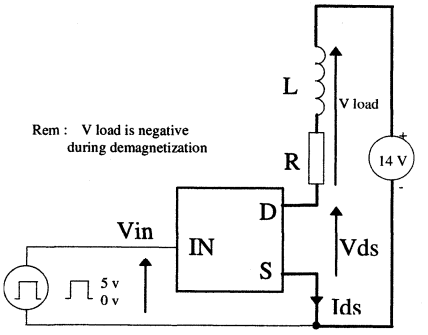


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

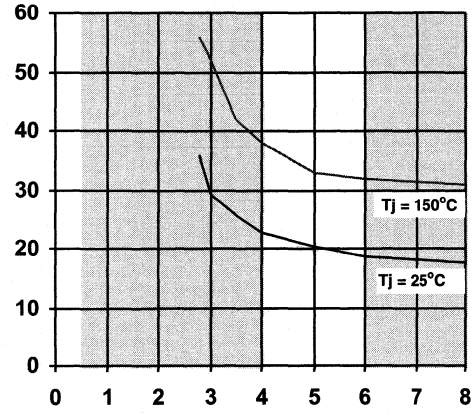


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

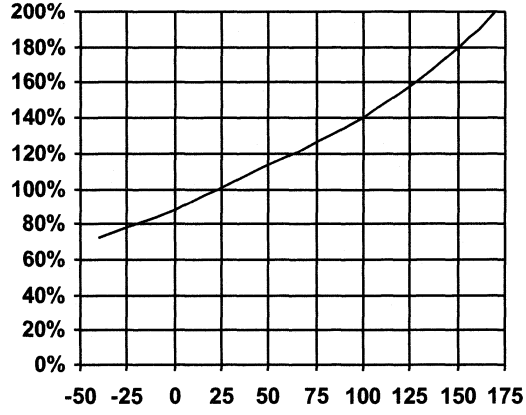


Figure 6 - Normalised Rds ON (%) Vs Tj (°C)

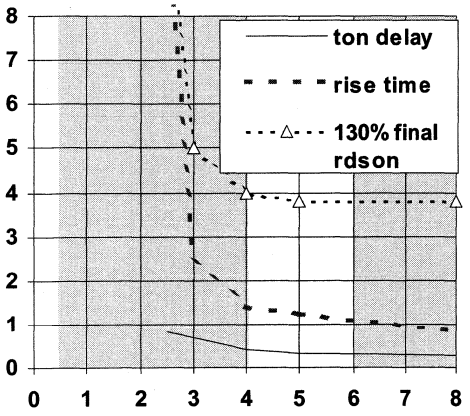


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{ds(on)}$ (us) Vs Input Voltage (V)

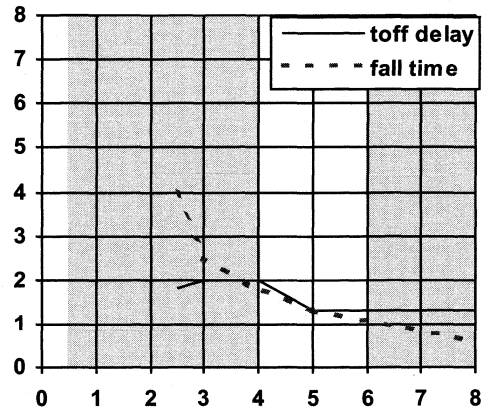


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

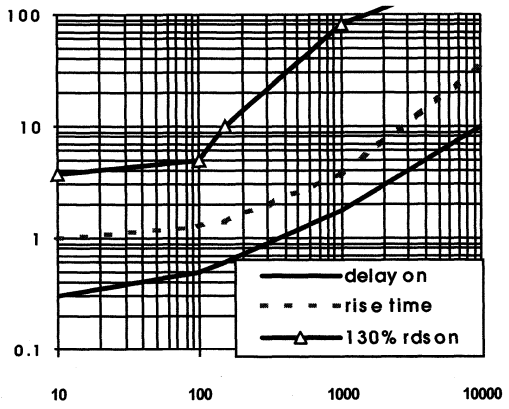


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs IN Resistor (Ω)

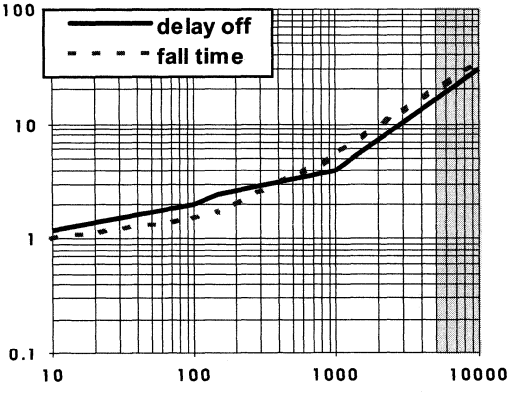


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

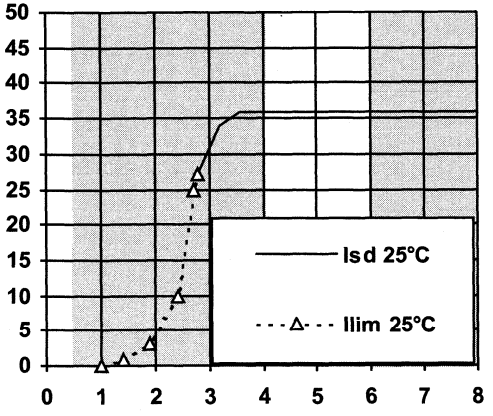


Figure 11 - Current lim. & Ishutdown (A) Vs Vin (V)

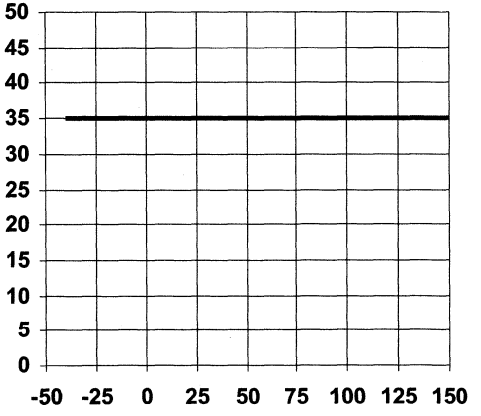


Figure 12 - Ishutdown (A) Vs Temperature (°C)

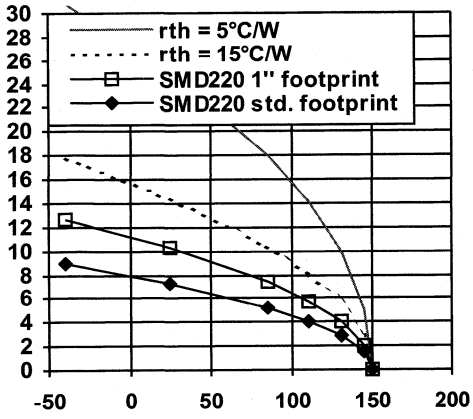


Figure 13 - Max.Cont. Ids (A) Vs Ambient Temperature (°C)

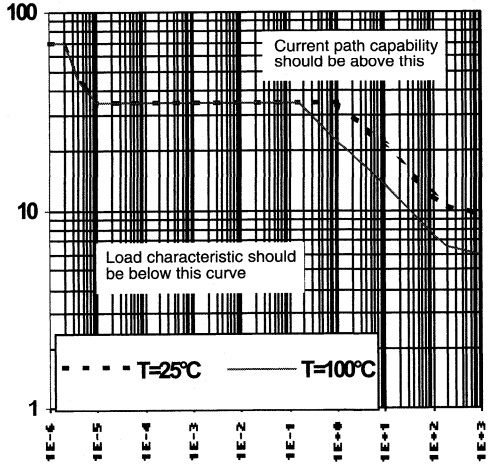


Figure 14 - Max.Cont. Ids (A) Vs Ambient Temperature (°C)

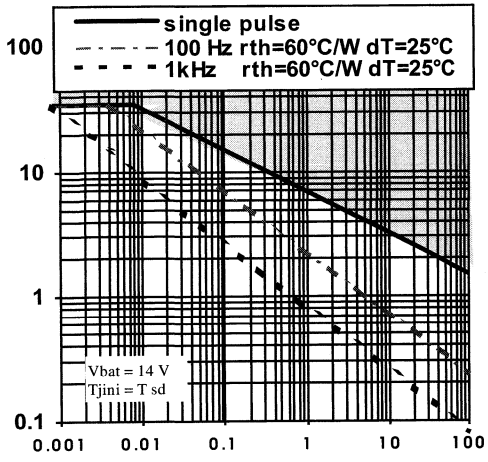


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

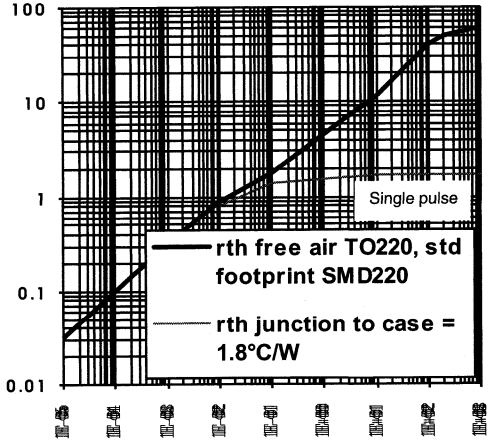


Figure 16 - Transient Thermal Imped. (°C/W) Vs Time (s) - IPS0151/IPS051S

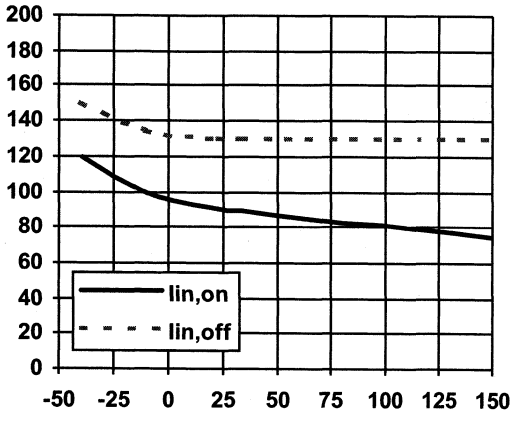


Figure 17 - Input current (μA) Vs Junction (°C)

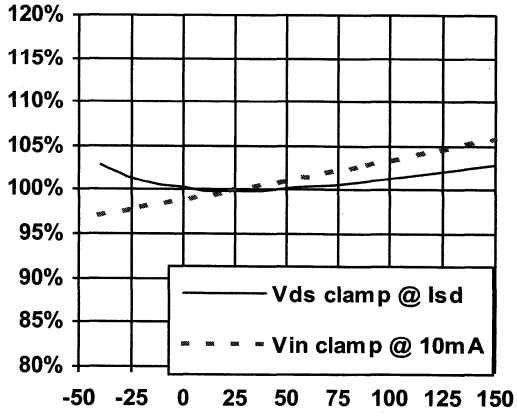


Figure 18 - Vin clamp and V clamp2 (V)
Vs Tjunction (°C)

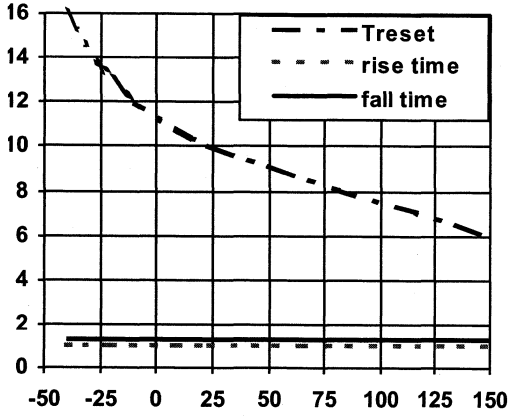
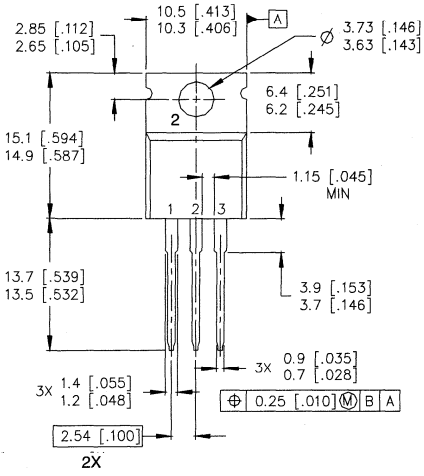
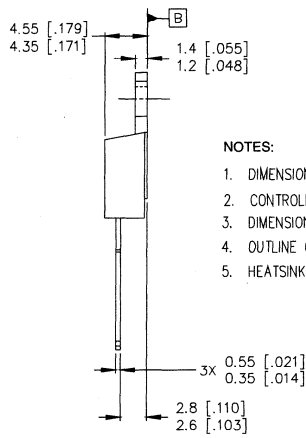


Figure 19 - Turn-on, Turn-off, and Treset (μs)
Vs Tjunction (°C)

Case Outline - TO-220



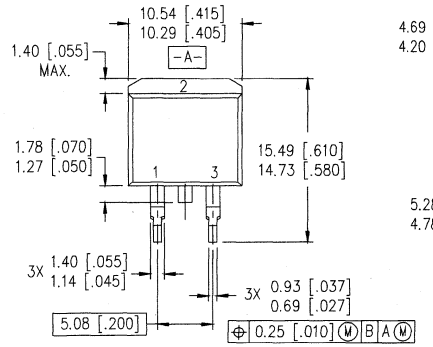


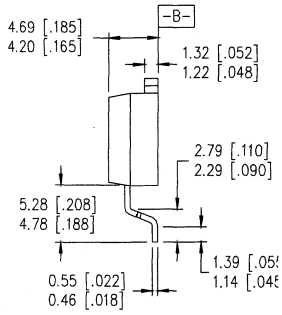
NOTES:

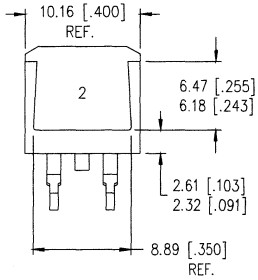
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
5. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

IRGB 01-3026 01

Case Outline - D²PAK (SMD220)



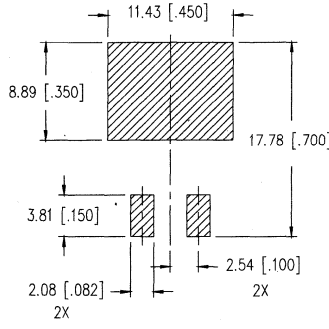




NOTES:

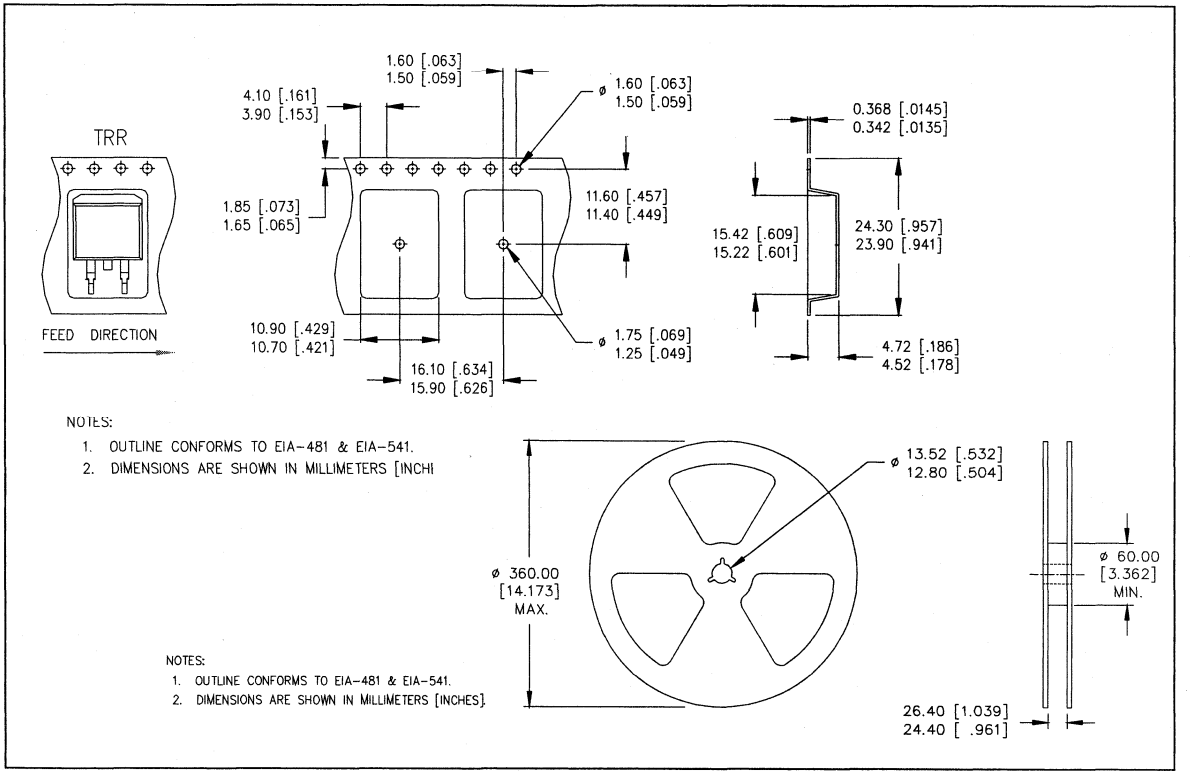
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSIONS AFTER SOLDER DIP.
5. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

MINIMUM RECOMMENDED FOOTPRINT



01-0016 05

Tape & Reel - D²PAK (SMD220)



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

Data Sheet No.PD 60148-J

IPS021/IPS021S

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

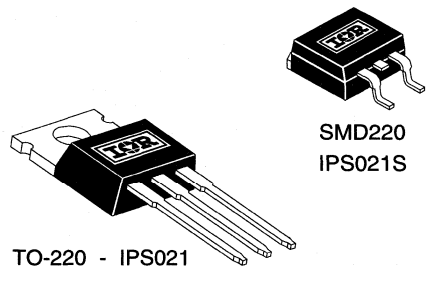
Description

The IPS021/IPS021S are fully protected three terminal SMART POWER MOSFETs that feature over-current, over-temperature, ESD protection and drain to source active clamp.These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 5A. These devices restart once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

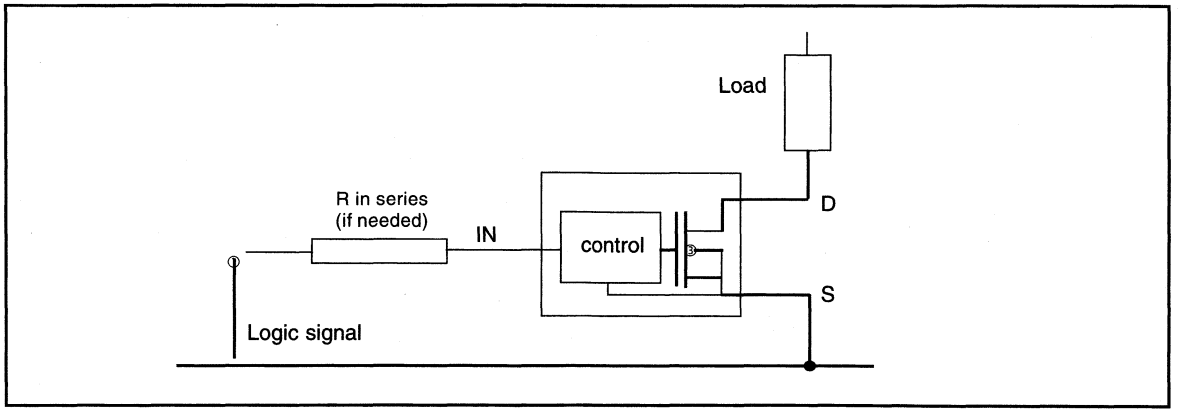
Product Summary

$R_{ds(on)}$	150mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	5A
T_{on}/T_{off}	1.5µs

Packages



Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continous current (1)			A	
	(rth=62°C/W) IPS021	—	2.8		
	(rth=10°C/W) IPS021	—	8		
	(rth=80°C/W) IPS021S	—	2.2		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10A		
P_d	Maximum power dissipation (1)			W	
	(rth=62°C/W) IPS021	—	2		
	(rth=80°C/W) IPS021S	—	1.56		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance free air	—	60	—	°C/W	TO-220
R_{th} 2	Thermal resistance junction to case	—	5	—		
R_{th} 1	Thermal resistance with standard footprint	—	80	—		D^2PAK (SMD220)
R_{th} 2	Thermal resistance with 1" square footprint	—	50	—		
R_{th} 3	Thermal resistance junction to case	—	5	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{ds} (max)	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} Tamb=85°C	Continuous drain current (TAmbient = 85°C, IN = 5V, rth = 60°C/W, Tj = 125°C)	—	1.8	A
R_{in}	Recommended resistor in series with IN pin	0.5	5	kΩ
Tr-in (max)	Max recommended rise time for IN signal (see fig. 2)	—	1	μS
Fr-Isc (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. Notes.

Static Electrical Characteristics

Standard footprint 70 μm copper thickness. T_j = 25°C (unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	100	130	150	mΩ	V_{in} = 5V, I_{ds} = 1A
	T_j = 150°C	—	220	280		
I_{dss} 1	Drain to source leakage current	0	0.01	25	μA	V_{cc} = 14V, T_j = 25°C
I_{dss} 2	Drain to source leakage current	0	0.1	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	48	54	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	56	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
V_{in} clamp	IN to source clamp voltage	7	8	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.5	2		I_d = 50mA, V_{ds} = 14V
I_{in}, -on	ON state IN positive current	25	90	200	μA	V_{in} = 5V
I_{in}, -off	ON state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 10Ω, Rinput = 50Ω, 100μs pulse, T_j = 25°C, (unless otherwise specified).

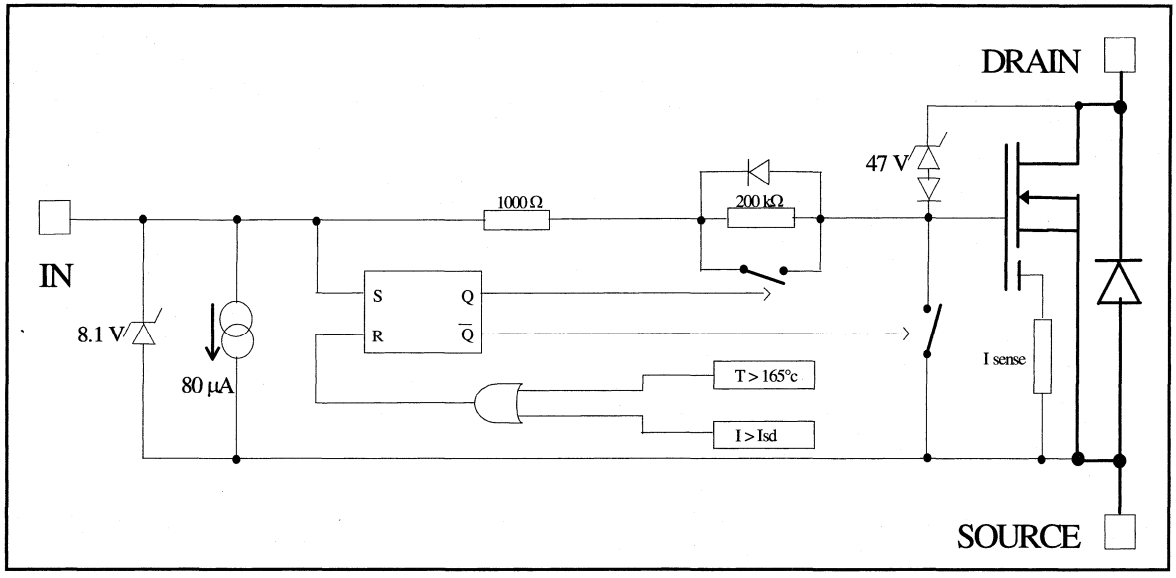
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.15	0.5	1	μs	See figure 2
T_r	Rise time	0.4	0.9	2		
T_{rf}	Time to (final $R_{ds(on)}$ 1.3)	2	6	12		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.3	2.5		
Q_{in}	Total gate charge	—	3.3	—	nC	V_{in} = 5V

Protection Characteristics

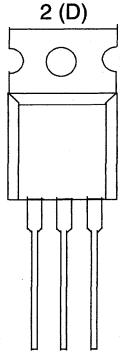
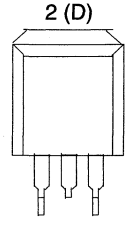
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	4	5.5	7	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	μs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	μJ	V_{cc} = 14V

Functional Block Diagram

All values are typical



Lead Assignments

 TO-220	 D²PAK (SMD220)
IPS021	**IPS021S**
Part Number	

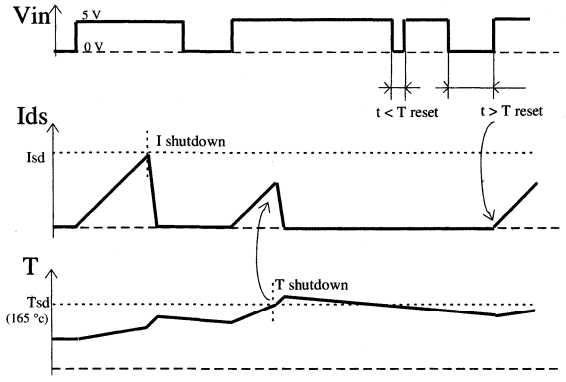


Figure 1 - Timing diagram

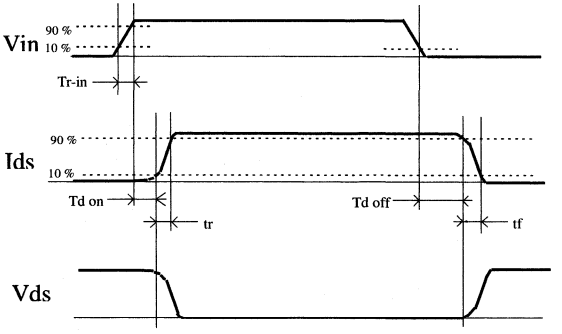


Figure 2 - IN rise time & switching time definitions

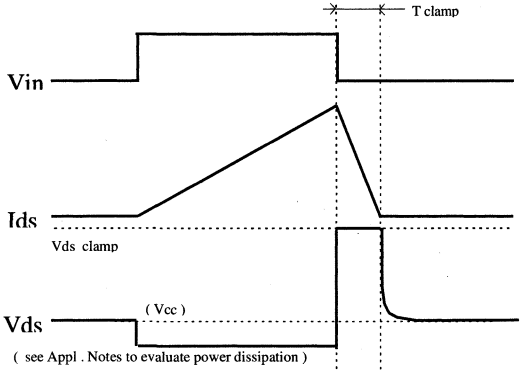


Figure 3 - Active clamp waveforms

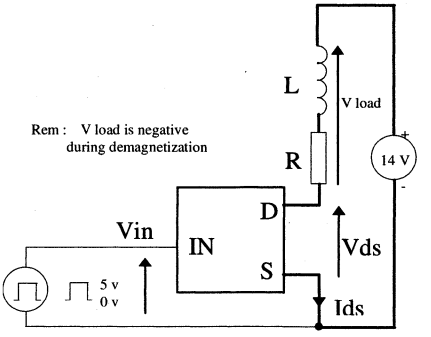


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

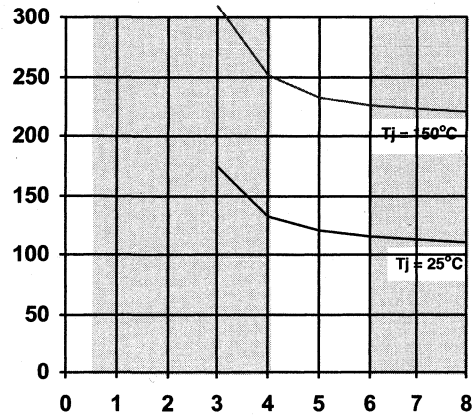


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

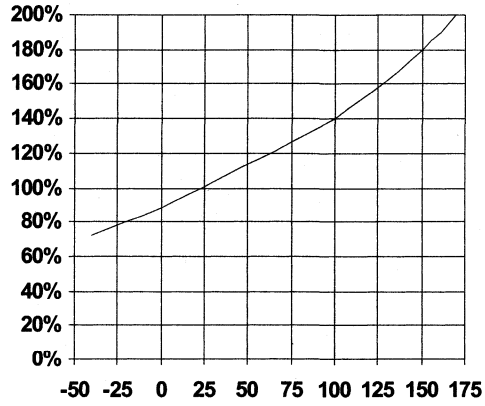


Figure 6 - Normalized Rds(on) (%) Vs Tj (°C)

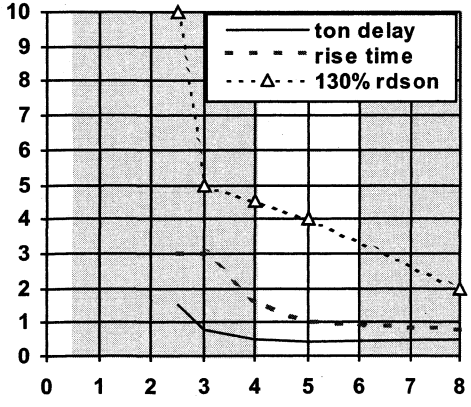


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs Input Voltage (V)

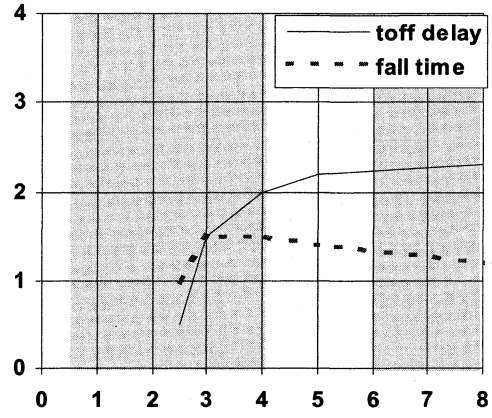


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

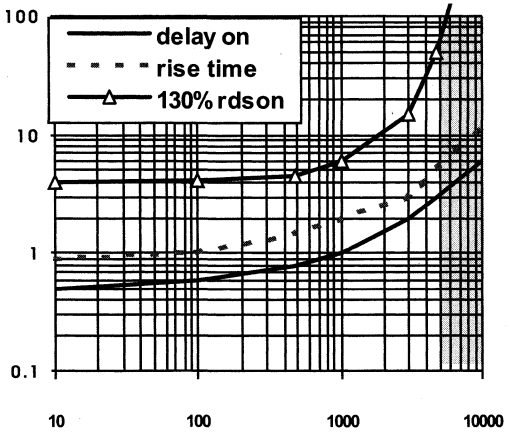


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs IN Resistor (Ω)

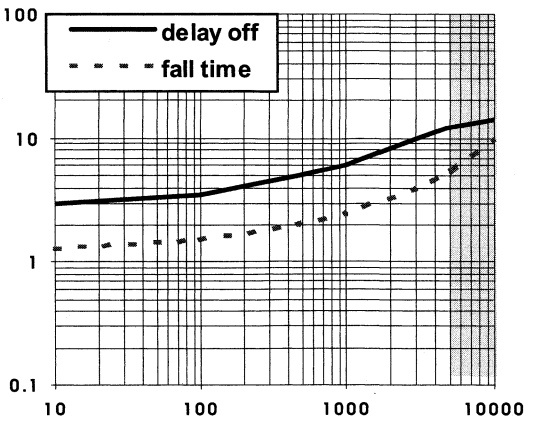


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

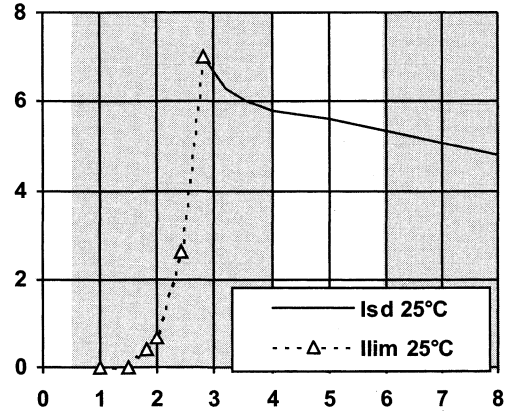


Figure 11 - Current lim. & I shutdown (A) Vs Vin (V)

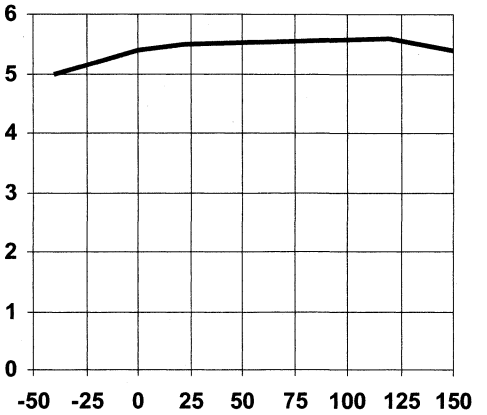


Figure 12 - I shutdown (A) Vs Temperature (°C)

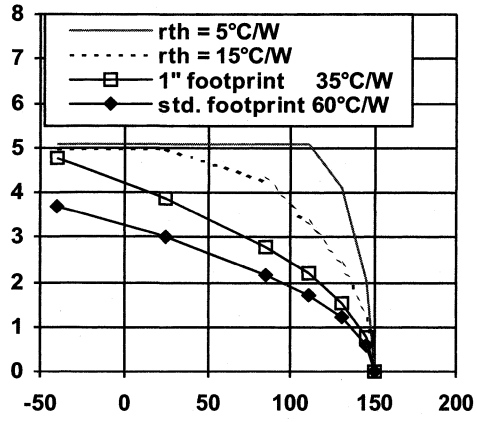


Figure 13 - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) IPS021/IPS021S

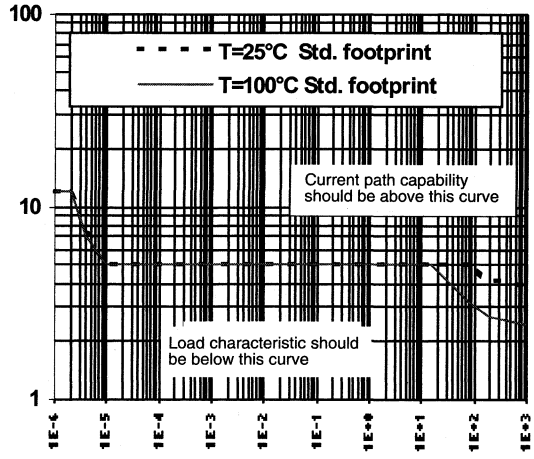


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
IPS021 & IPS021S

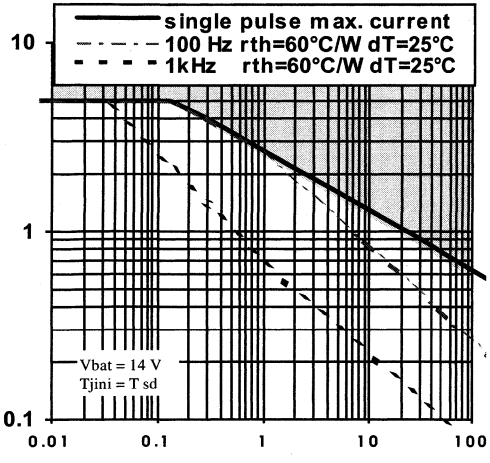


Figure 15a - Iclamp (A) Vs Inductive Load (mH)
IPS021

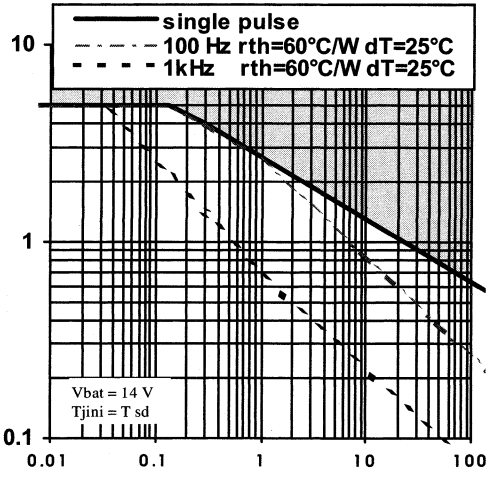


Figure 15b - Max. Iclamp (A) Vs Inductive Load
(mH) IPS021S

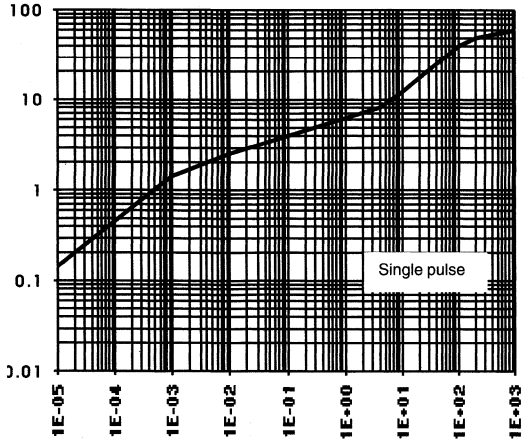


Figure 16 - Transient Thermal Imped. (°C/W) Vs Time (s)

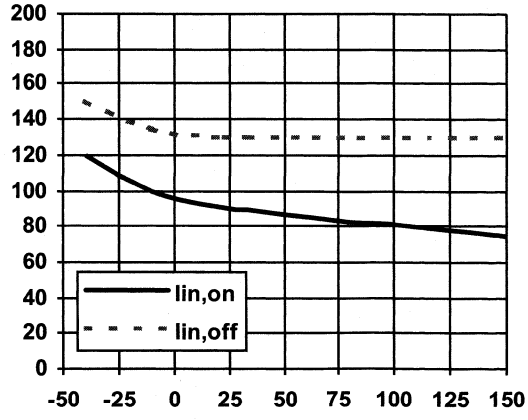


Figure 17 - Input Current (uA) Vs Junction Temperature (°C)

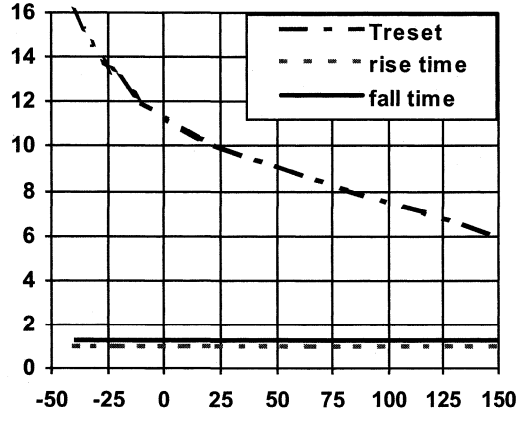


Figure 18 - Rise Time, Fall Time and Treset (µs) Vs Tj (°C)

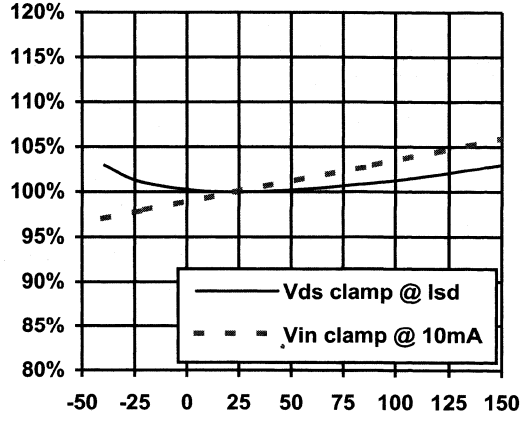
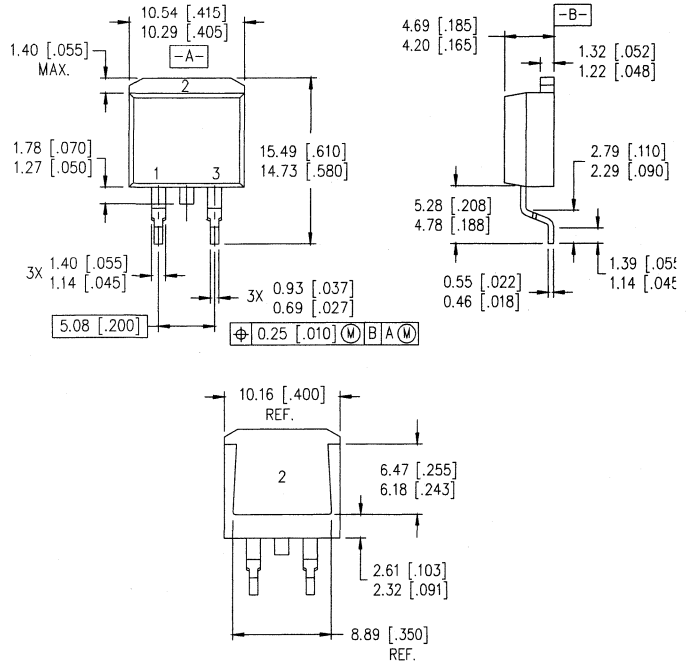


Figure 19 -Vin clamp and Vds clamp (%) Vs Tj (°C)

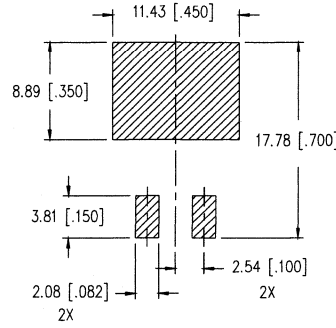
Case Outline - D²PAK (SMD220)



NOTES:

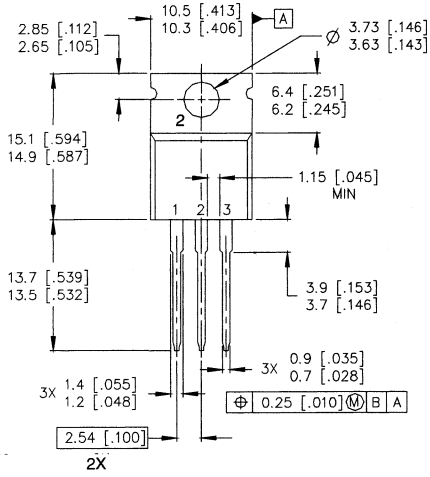
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSIONS AFTER SOLDER DIP.
5. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

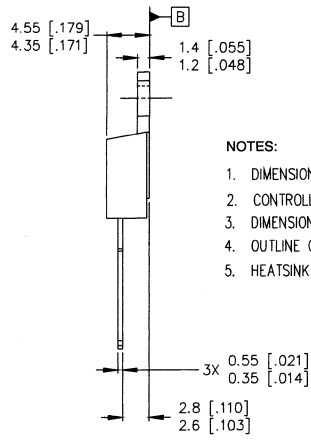
MINIMUM RECOMMENDED FOOTPRINT



01-0016 05

Case Outline - TO220



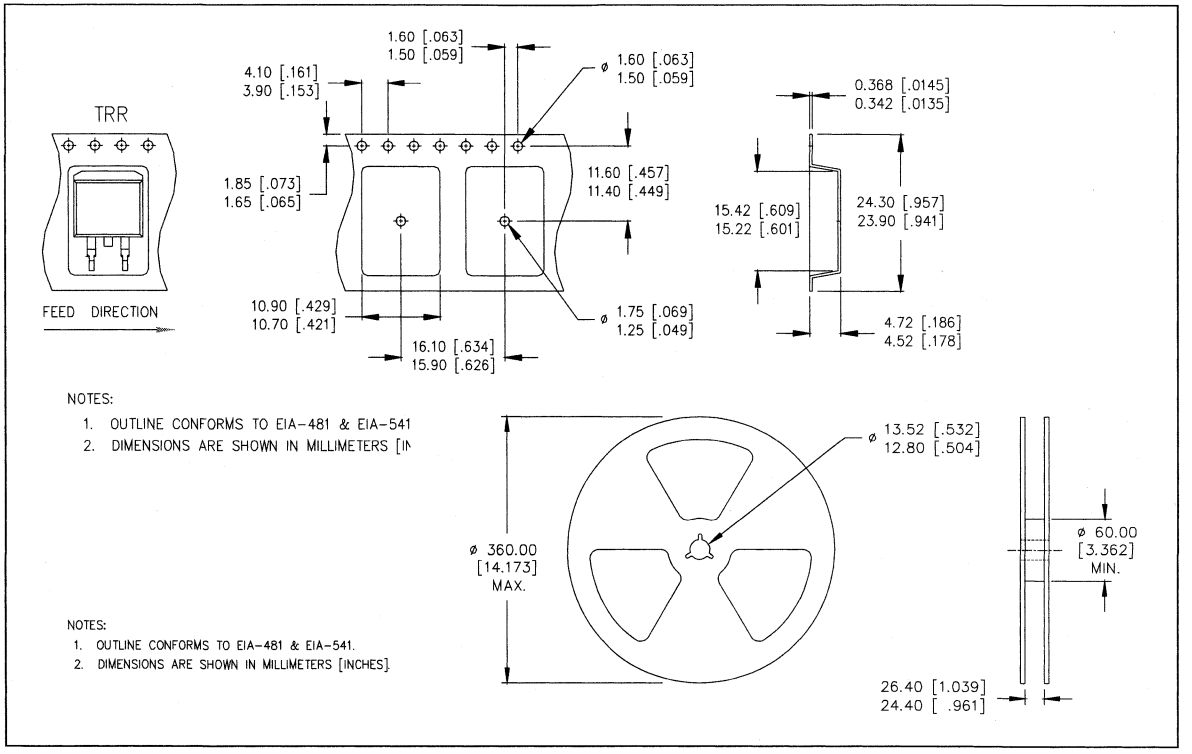


NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
5. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

IRGB 01-3026 01

Tape & Reel - D²PAK (SMD220)



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IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

IPS021L

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

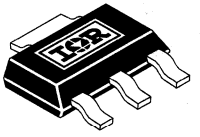
Description

The IPS021L is a fully protected three terminal SMART POWER MOSFET that features over-current, over-temperature, ESD protection and drain to source active clamp.This device combines a HEXFET® POWER MOSFET and a gate driver. It offers full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 5A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

Product Summary

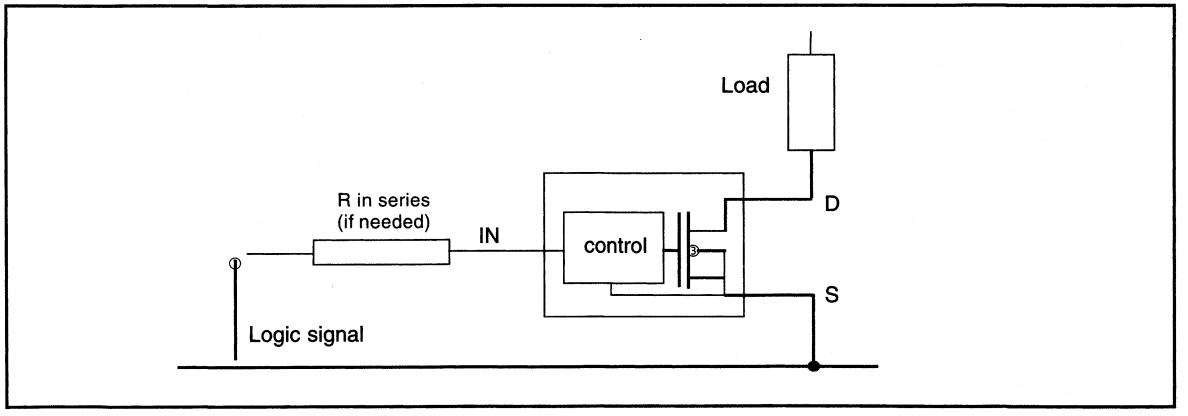
$R_{ds(on)}$	150mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	5A
T_{on}/T_{off}	1.5µs

Package



3 Lead SOT223

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 µm copper thickness..

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum Input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1) (rth=125°C/W)	—	1.4	A	
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10		
P_d	Maximum power dissipation (1) (rth=125°C/W)	—	1	W	
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10µH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint	—	100	—	°C/W	
R_{th2}	Thermal resistance with 1" square footprint	—	50	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} $T_{amb=85°C}$	Continuous drain current ($T_{Ambient}$ = 85°C, IN = 5V, rth = 100°C/W, Tj = 125°C)	—	1.4	A
R_{in}	Recommended resistor in series with IN pin	0.5	5	kΩ
$T_{r\text{-}in\ (max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. notes.

Static Electrical Characteristics

Standard footprint 70 μm copper thickness. T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	100	130	150	mΩ	V_{in} = 5V, I_{ds} = 1A
	T_j = 150°C	—	220	280		
I_{dss} 1	Drain to source leakage current	0	0.01	25	μA	V_{cc} = 14V, T_j = 25°C
I_{dss} 2	Drain to source leakage current	0	0.1	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	48	54	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	56	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
V_{in} clamp	IN to source clamp voltage	7	8	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.5	2		I_d = 50mA, V_{ds} = 14V
I_{in}, -on	ON state IN positive current	25	90	200	μA	V_{in} = 5V
I_{in}, -off	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 10Ω, Rinput = 50Ω, 100μs pulse, T_j = 25°C, (unless otherwise specified).

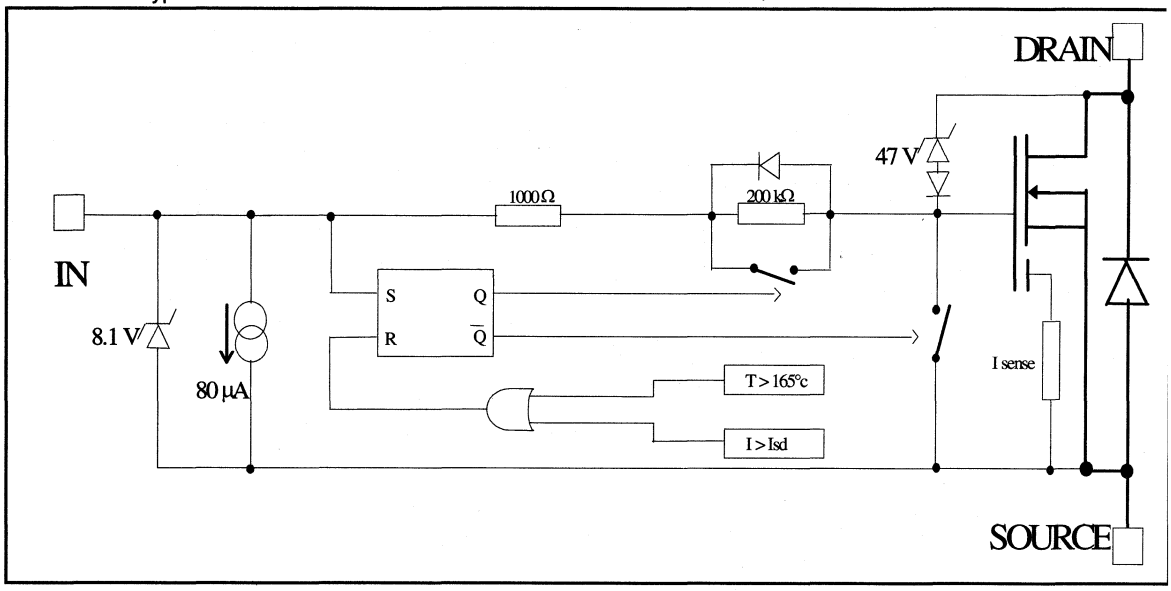
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.15	0.5	1	μs	See figure 2
T_r	Rise time	0.4	0.9	2		
T_{rf}	Time to 130% final $R_{ds(on)}$	2	6	12		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.3	2.5		
Q_{in}	Total gate charge	—	30	—	nC	V_{in} = 5V

Protection Characteristics

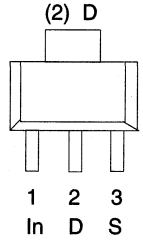
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	4	5.5	7	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	μs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	μJ	V_{cc} = 14V

Functional Block Diagram

All values are typical



Lead Assignments



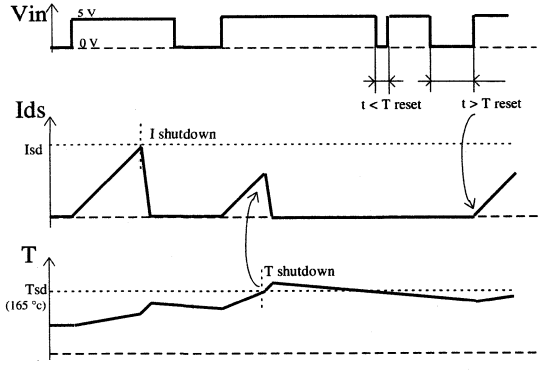


Figure 1 - Timing diagram

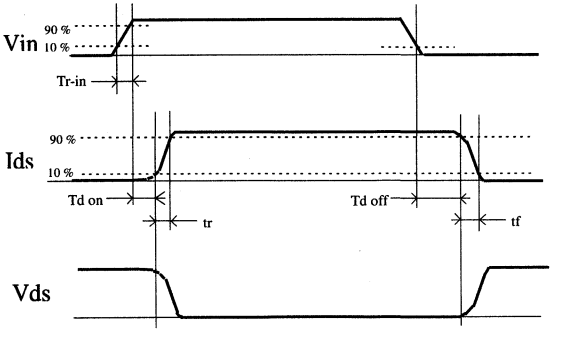


Figure 2 - IN rise time & switching time definitions

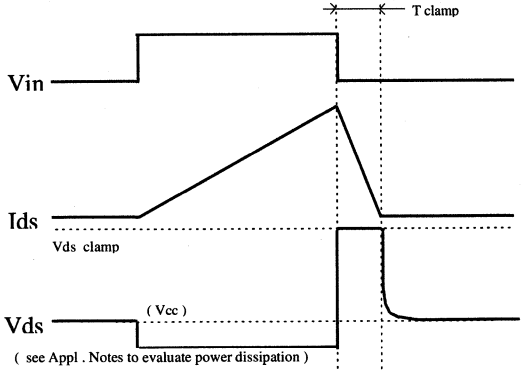


Figure 3 - Active clamp waveforms

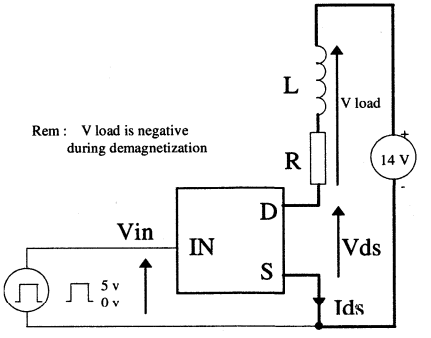


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

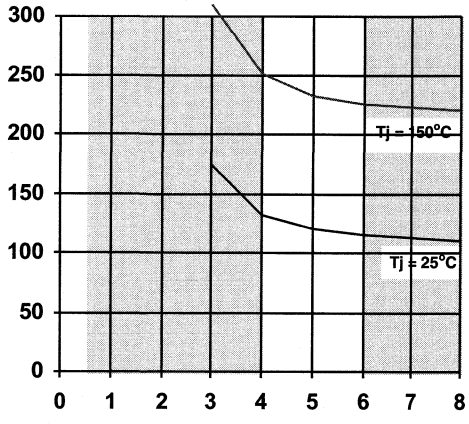


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

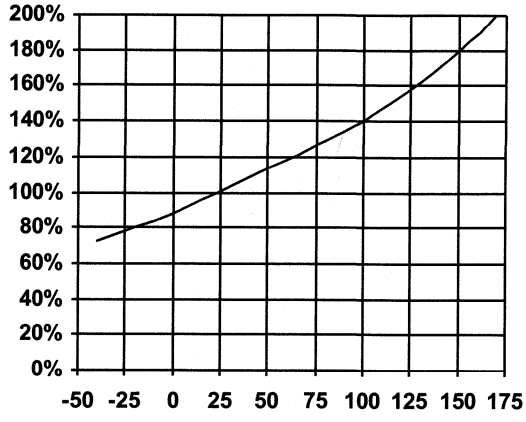


Figure 6 - Normalised Rds(on) (%) Vs Tj (°C)

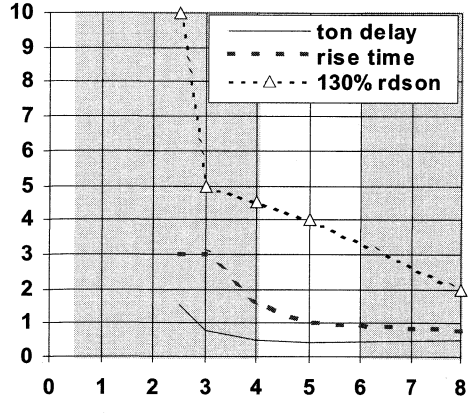


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs Input Voltage (V)

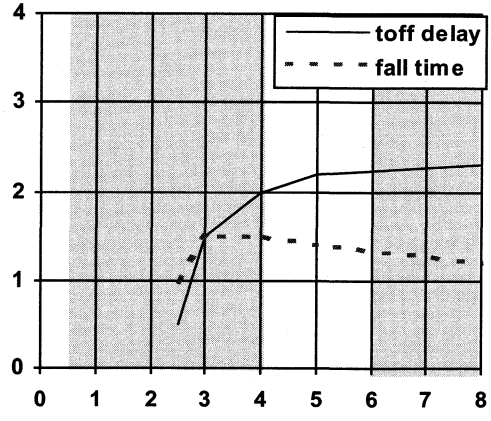


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

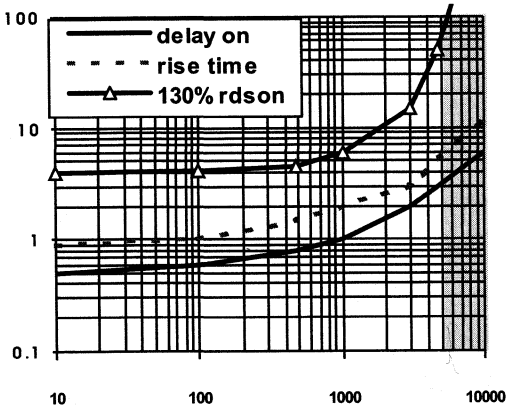


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs IN Resistor (Ω)

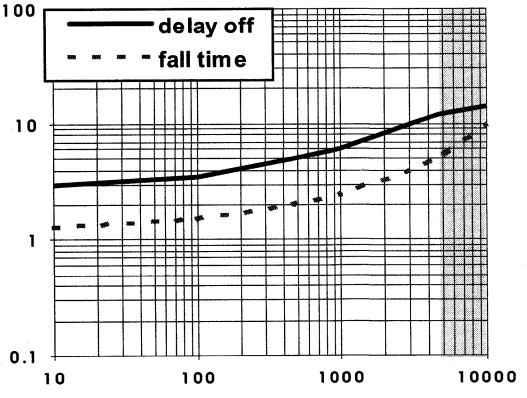


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

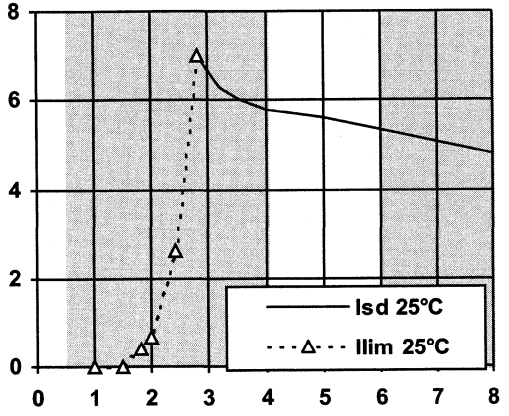


Figure 11 - Current lim. & I shutdown (A) Vs Vin (V)

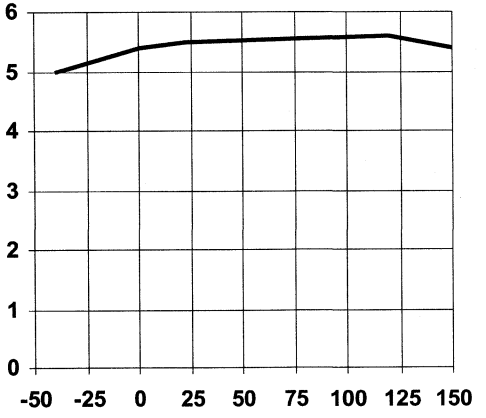


Figure 12 - I shutdown (A) Vs Temperature (°C)

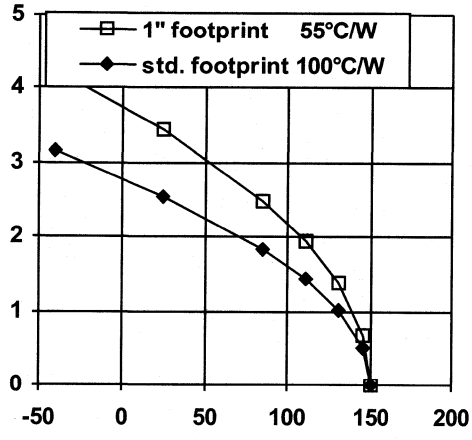


Figure 13 - Max.Cont. Ids (A) Vs Amb. Temperature (°C)

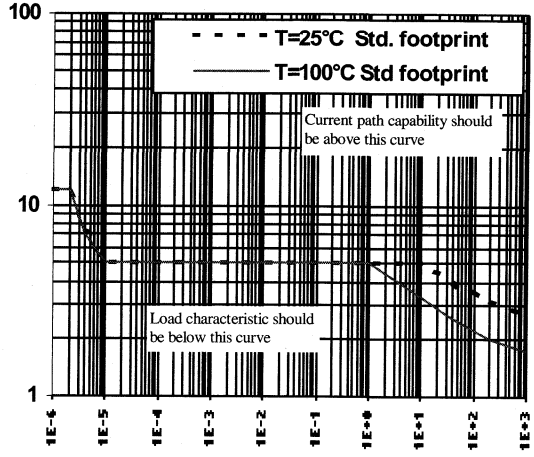


Figure 14 - Ids (A) Vs Protection Resp. Time (s)

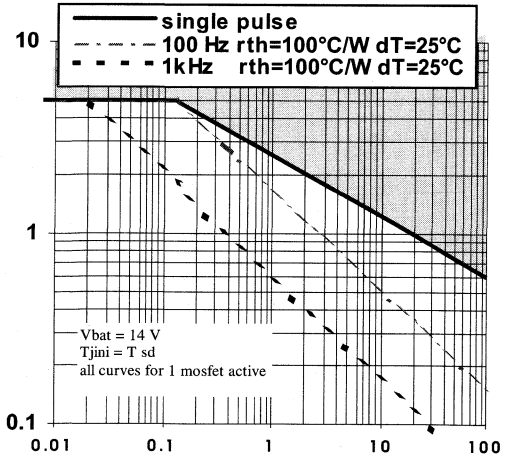


Figure 15 - I clamp (A) Vs Inductive Load (mH)

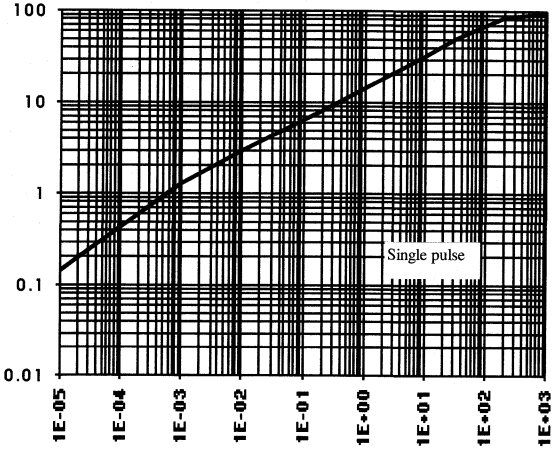


Figure 16 - Transient Thermal Imped. (°C/W) Vs Time (s)

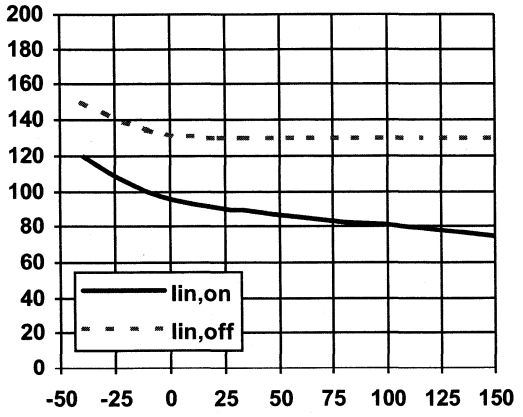


Figure 17 - Input Current (uA) Vs Junction Temperature (°C)

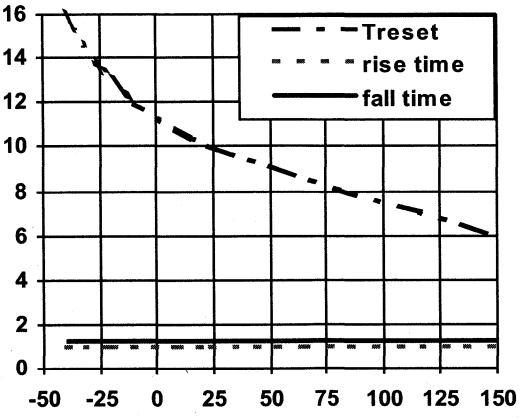


Figure 18 - Rise Time, Fall Time and Treset (μs) Vs Tj (°C)

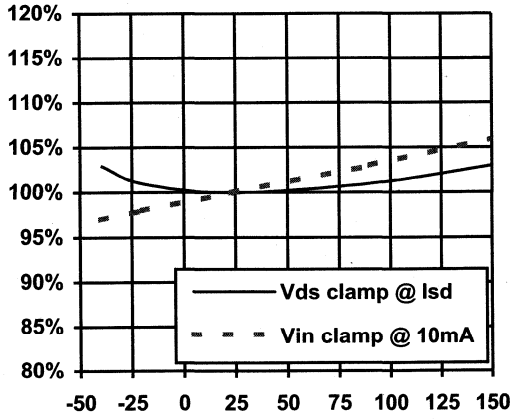
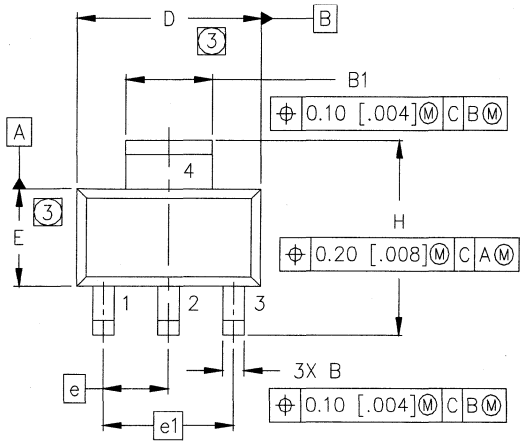
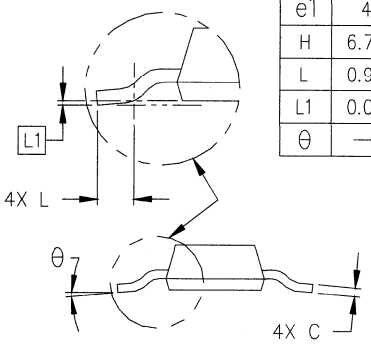


Figure 19 -Vin clamp and Vds clamp Vs Tj (°C)

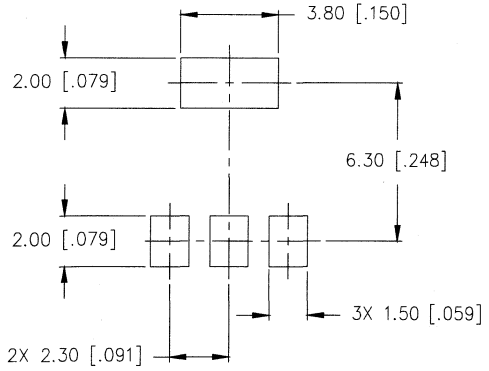
Case Outline - SOT-223





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.55	1.80	.061	.071
B	0.65	0.85	.026	.033
B1	2.95	3.15	.116	.124
C	0.25	0.35	.010	.014
D	6.30	6.70	.248	.264
E	3.30	3.70	.130	.146
e	2.30 BSC		.0905 BSC	
e1	4.60 BSC		.181 BSC	
H	6.71	7.29	.264	.287
L	0.91	—	.036	—
L1	0.061 BSC		.0024 BSC	
θ	—	10°	—	10°

MINIMUM RECOMMENDED FOOTPRINT



LEAD ASSIGNMENTS

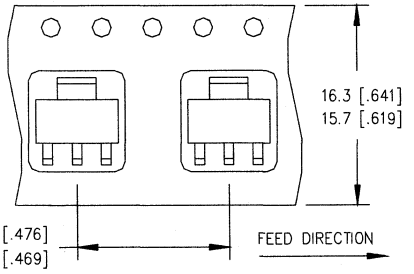
1 = GATE
2 = DRAIN
3 = SOURCE

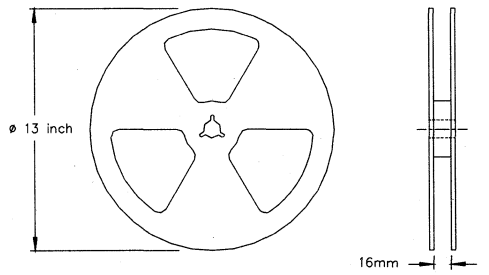
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

(TO-261AA) 01-0022 05

Tape & Reel - SOT223





NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.
4. EACH ø 330.00 [ø 13.00] REEL CONTAINS 2,500 DEVICES.

01-0028 05 / 01-0008 02

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Data and specifications subject to change without notice. 4/11/2000

International
IOR Rectifier

IPS022G/IPS024G

DUAL/QUAD FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

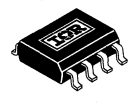
Description

The IPS022G/IPS024G are fully protected dual/quad low side SMART POWER MOSFETs respectively. They feature over-current, over-temperature, ESD protection and drain to source active clamp.These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 5A. These devices restart once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

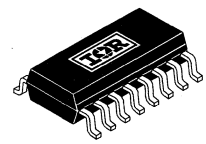
Product Summary

$R_{ds(on)}$	150mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	5A
T_{on}/T_{off}	1.5µs

Packages

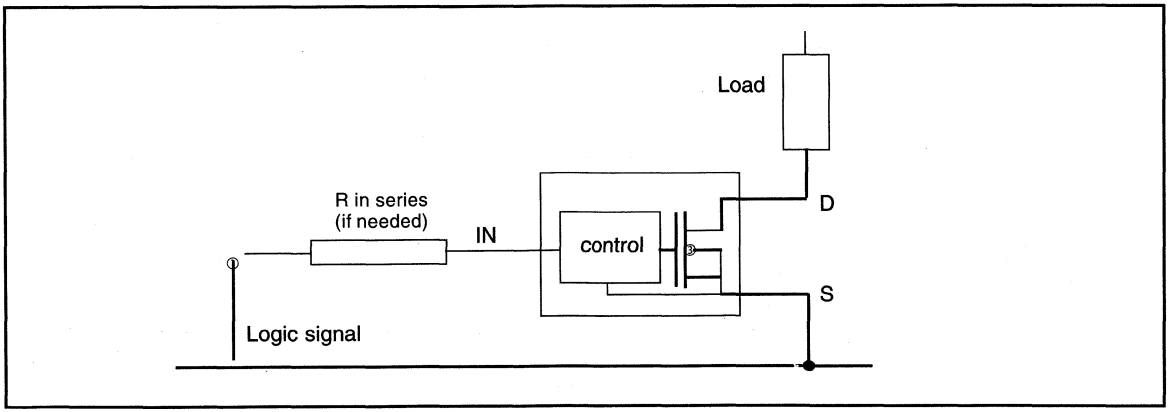


8 Lead SOIC
IPS022G
(Dual)



16 Lead SOIC
IPS024G
(Quad)

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(Σ Isd mosfets, rth=125°C/W, IPS022G)	—	1.4		
	(Σ Isd mosfets, rth=125°C/W, IPS024G)	—	2.3		
$I_{sd\ pulsed}$	Diode max. pulsed current (1) (for ea. mosfet)	—	10		
P_d	Maximum power dissipation(1)			W	
	(Σ Pd mosfets, rth=125°C/W)	—	1		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1} (2 mos on)	Thermal resistance with standard footprint (2 mosfets on)	—	100	—	°C/W	SOIC-8
R_{th2} (1 mos on)	Thermal resistance with standard footprint (1 mosfet on)	—	127	—		
R_{th3} (2 mos on)	Thermal resistance with 1" square footprint (2 mosfets on)	—	60	—		
R_{th1} (4 mos on)	Thermal resistance with standard footprint (4 mosfets on)	—	75	—		SOIC-16
R_{th2} (1mos on)	Thermal resistance with standard footprint (1 mosfet on)	—	120	—		
R_{th3} (4 mos on)	Thermal resistance with 1" square footprint (4 mosfets on)	—	60	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} Tamb=85°C	Continuous drain current (TAmbient = 85°C, IN = 5V, rth = 100°C/W, Tj = 85°C) IPS022G	—	1	A
	(TAmbient = 85°C, IN = 5V, rth = 100°C/W, Tj = 125°C) IPS024G	—	0.7	
R_{in}	Recommended resistor in series with IN pin	0.5	5	kΩ
Tr-in (max)	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
Fr-Isc (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

Static Electrical Characteristics

Standard footprint 70 µm copper thickness. (T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	100	130	150	mΩ	V_{in} = 5V, I_{ds} = 1A
	T_j = 150°C	—	220	280		
$I_{dss\ 1}$	Drain to source leakage current	0	0.01	25	µA	V_{cc} = 14V, T_j = 25°C
$I_{dss\ 2}$	Drain to source leakage current	0	0.1	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	48	54	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	56	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to source clamp voltage	7	8	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.5	2		I_d = 50mA, V_{ds} = 14V
$I_{in,\ -on}$	ON state IN positive current	25	90	200	µA	V_{in} = 5V
$I_{in,\ -off}$	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 10Ω, Rinput = 50Ω, 100µs pulse, T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.15	0.5	1	µs	See figure 2
T_r	Rise time	0.4	0.9	2		
T_{rf}	Time to 130% final $R_{ds(on)}$	2	6	12		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.3	2.5		
Q_{in}	Total gate charge	—	3.3	—	nC	V_{in} = 5V

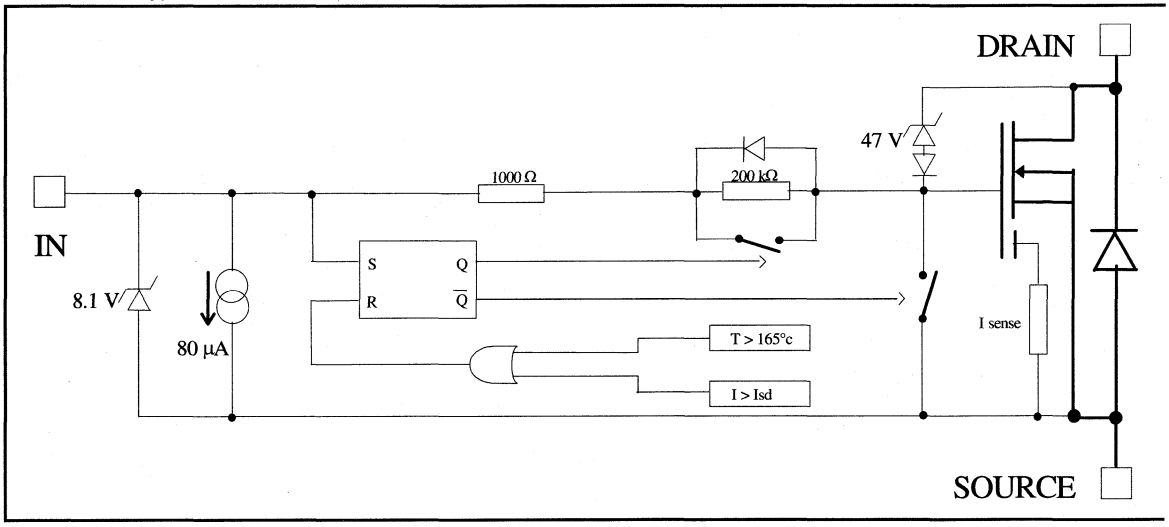
(2) Operations at higher switching frequencies is possible. See Appl. notes.

Protection Characteristics

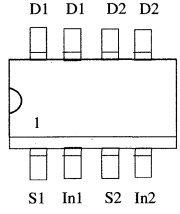
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	4	5.5	7	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{CC} = 14V

Functional Block Diagram

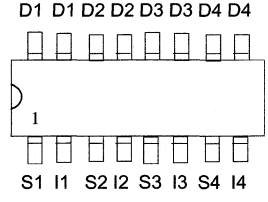
All values are typical



Lead Assignments



8 Lead SOIC
(Dual)



16 Lead SOIC
(Quad)

IPS022G	IPS024G
Part Number	

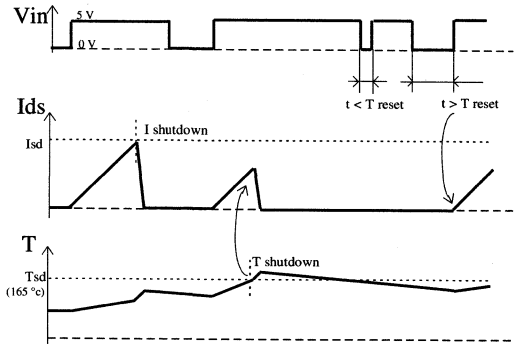


Figure 1 - Timing diagram

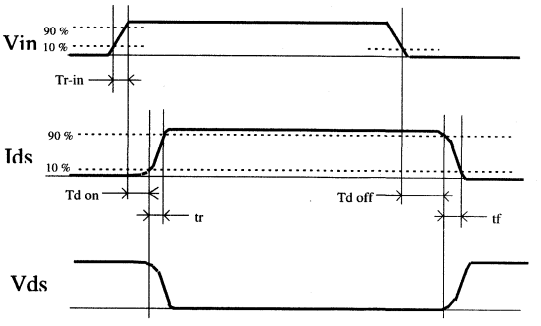


Figure 2 - IN rise time & switching time definitions

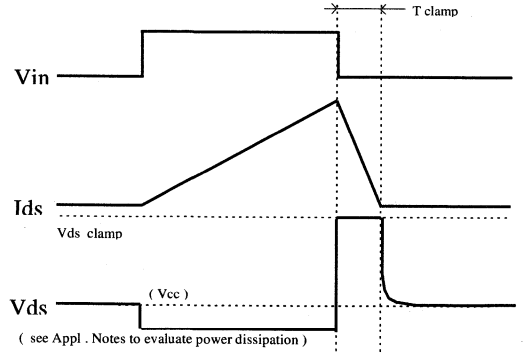


Figure 3 - Active clamp waveforms

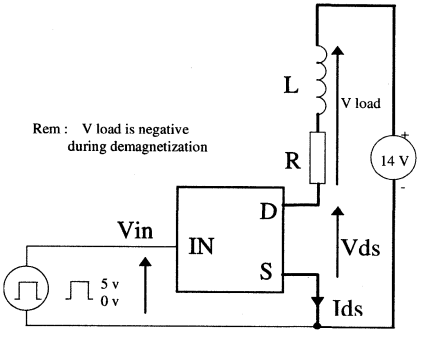


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

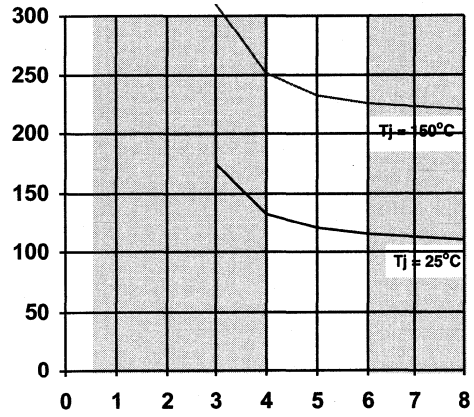


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

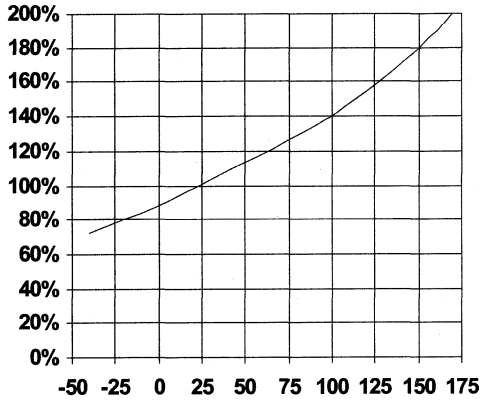


Figure 6 - Normalized Rds(on) (%) Vs Tj (°C)

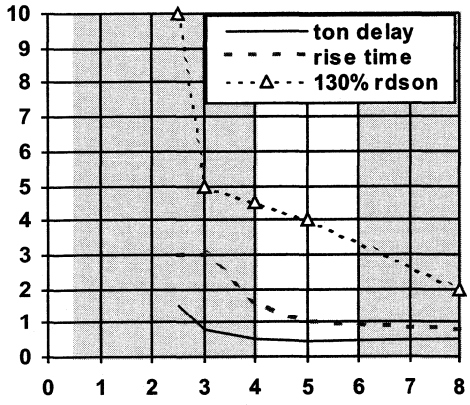


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs Input Voltage (V)

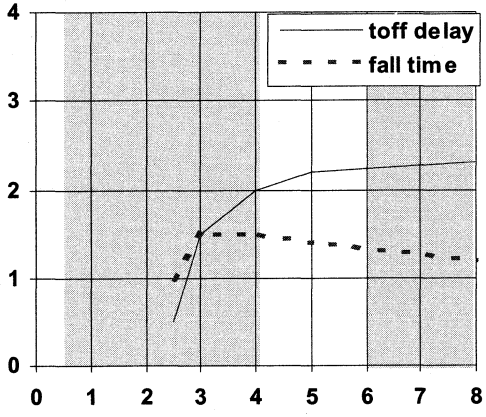


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

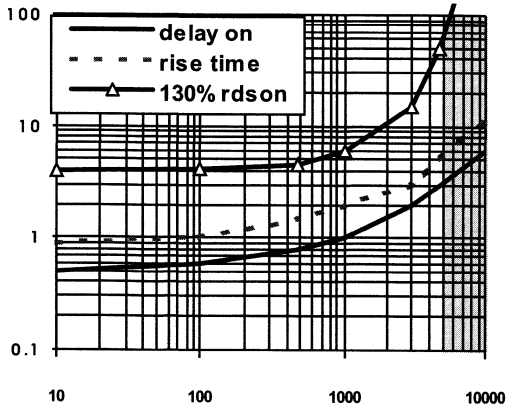


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs IN Resistor (Ω)

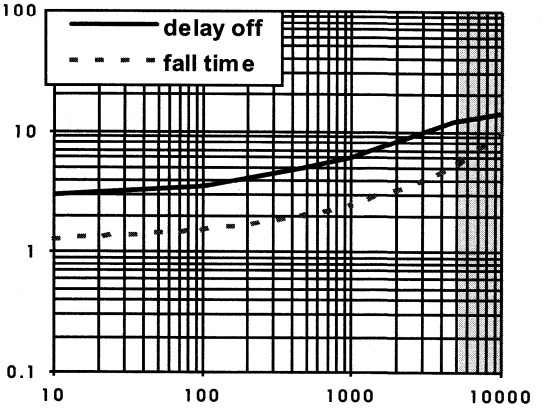


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

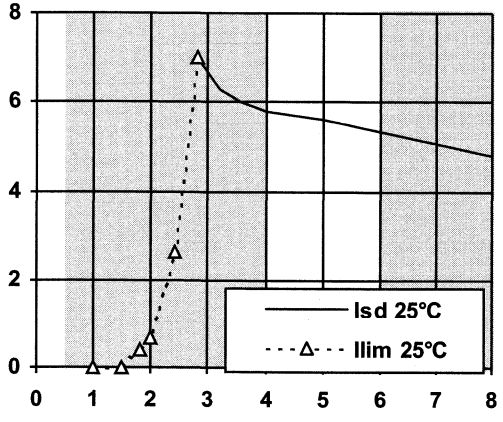


Figure 11 - Current lim. & I shutdown (A) Vs Vin (V)

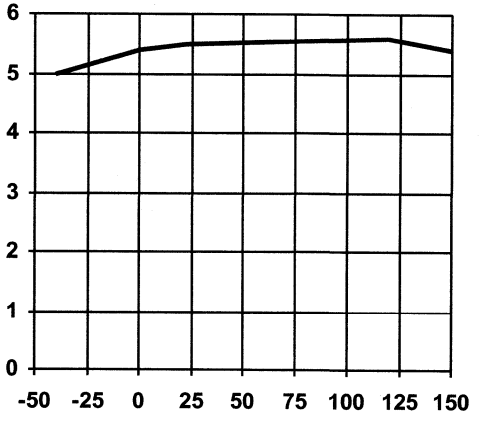


Figure 12 - I shutdown (A) Vs Temperature (°C)

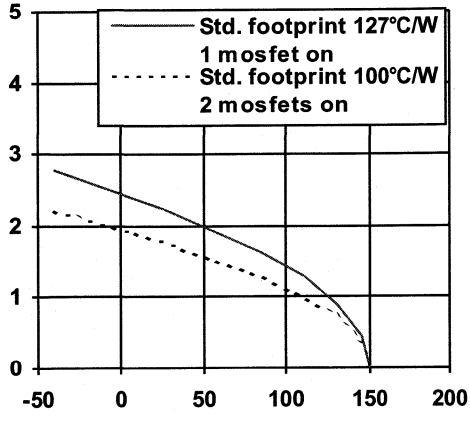


Figure 13a - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS022G

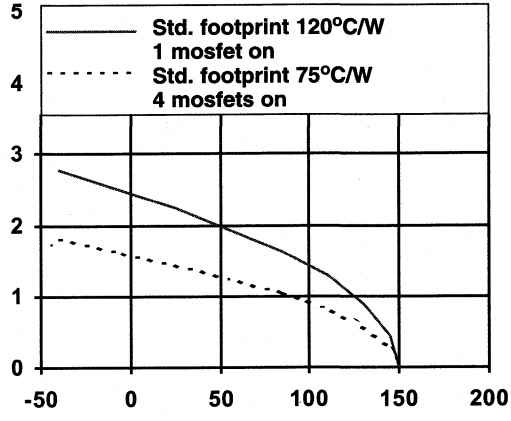


Figure 13b - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS024G

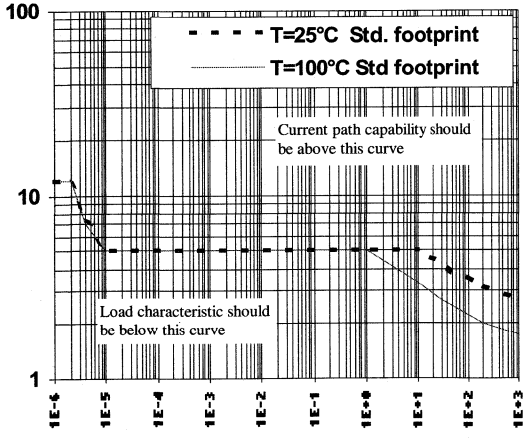


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
IPS022G/IPS024G

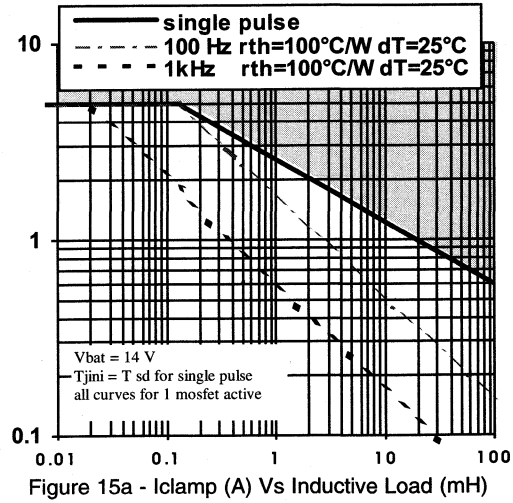


Figure 15a - Iclamp (A) Vs Inductive Load (mH)
IPS022G

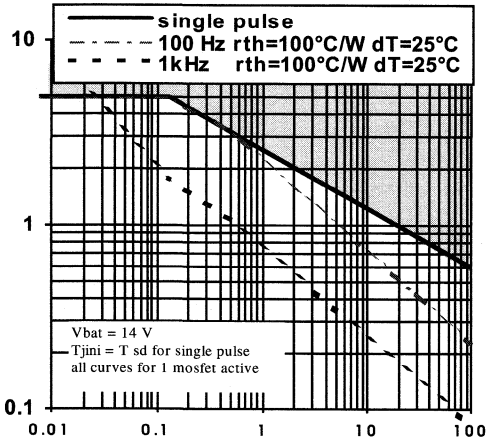


Figure 15b - Max. Iclamp (A) Vs Inductive Load (mH) - IPS024G

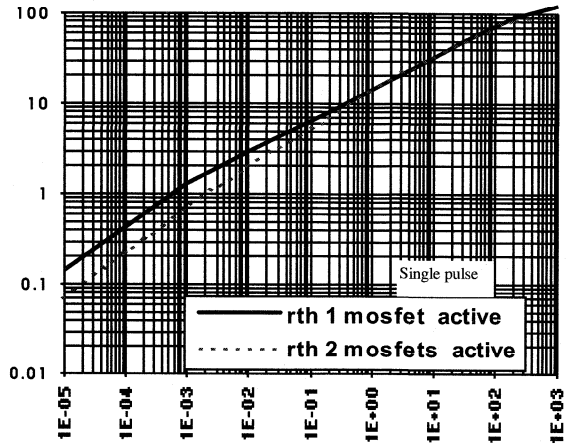


Figure 16a - Transient Thermal Imped. (°C/W) Vs Time (s) - IPS022G

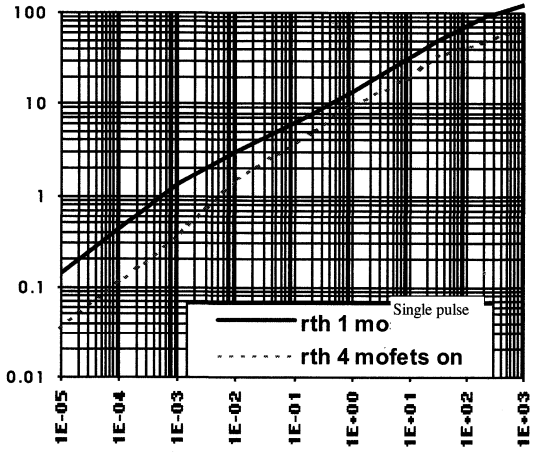


Figure 16b - Transient Thermal Imped. (°C/W) Vs Time (s) - IPS024G

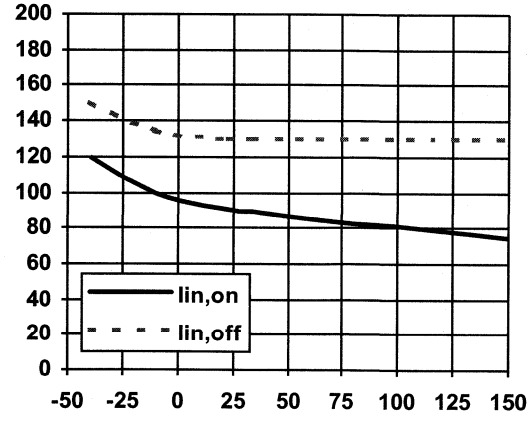


Figure 17 - Input Current (uA) Vs Junction Temperature (°C)

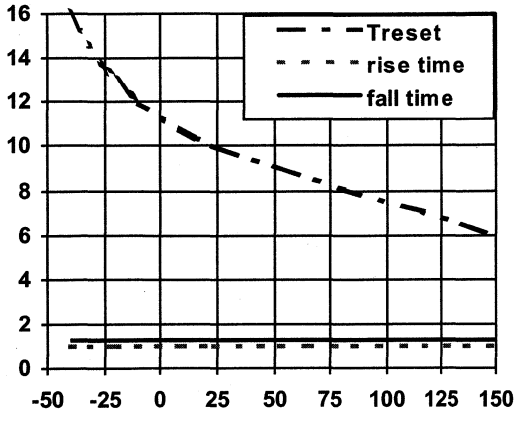


Figure 18 - Rise Time, Fall Time and Treset (µs) Vs Tj (°C)

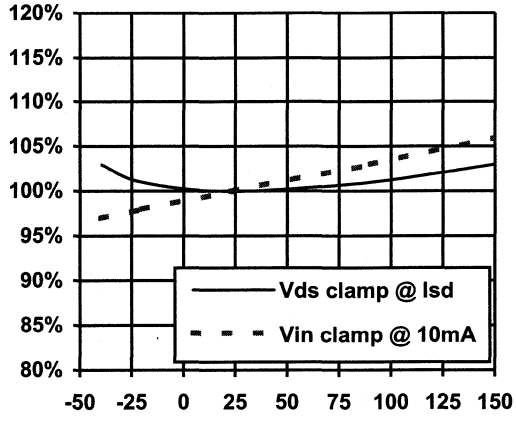
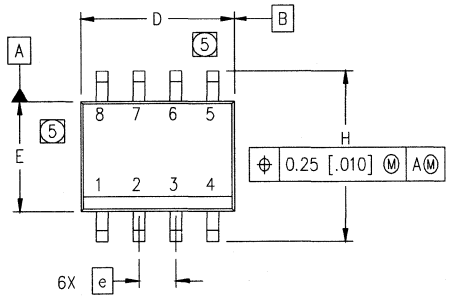
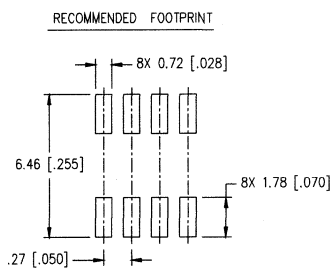


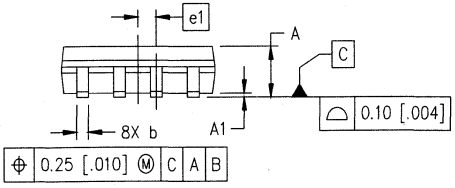
Figure 19 -Vin clamp and Vds clamp2 (%) Vs Tj (°C)

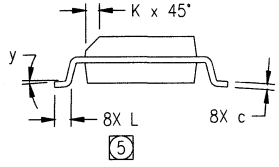
Case Outline - 8 Lead SOIC





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°





NOTES:

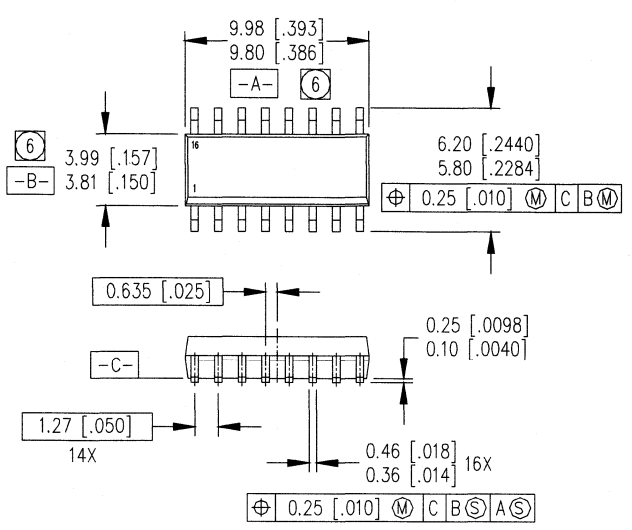
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

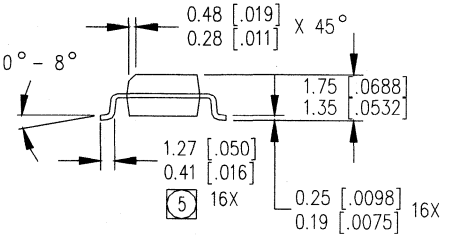
(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

Case Outline - 16 Lead SOIC (narrow body)



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



01-3064 00

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

Data Sheet No.PD 60150-I

IPS031/IPS031S

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

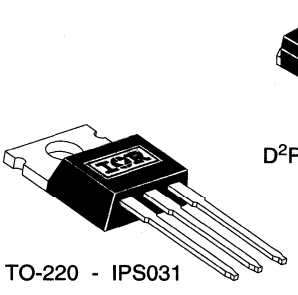
Description

The IPS031/IPS031S are fully protected three terminal SMART POWER MOSFETs that feature over-current, over-temperature, ESD protection and drain to source active clamp.These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 12A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

Product Summary

$R_{ds(on)}$	60mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	12A
T_{on}/T_{off}	1.5µs

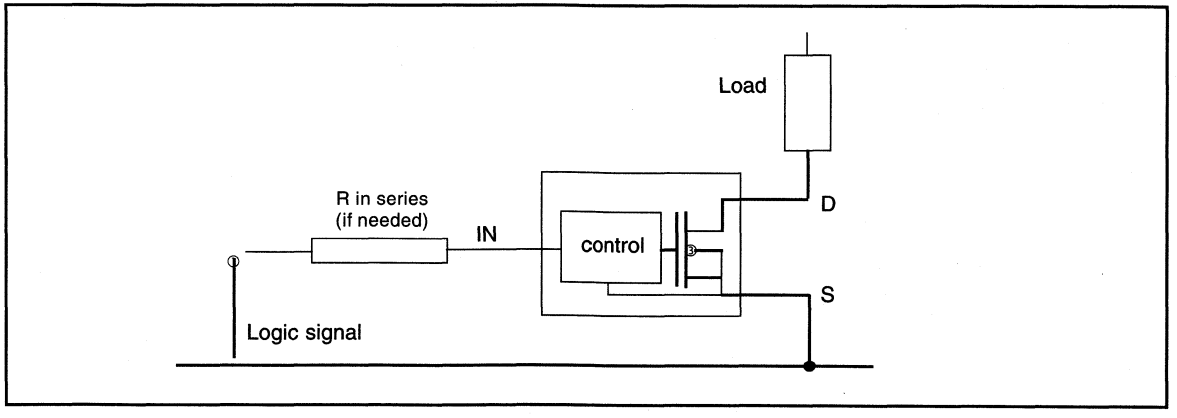
Packages



D²Pak (SMD220)
IPS031S

TO-220 - IPS031

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	rth=62°C/W IPS031	—	2.8		TO220 free air
	rth=5°C/W IPS031	—	18		TO220 with Rth=5°C/W
	rth=80°C/W IPS031S	—	2.2		SMD220 Std. footprint
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	18		
P_d	Maximum power dissipation(1)			W	
	(rth=62°C/W) IPS031	—	2		
	(rth=80°C/W) IPS031S	—	1.56		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance free air	—	60	—	°C/W	TO-220
R_{th} 2	Thermal resistance junction to case	—	3	—		
R_{th} 1	Thermal resistance with standard footprint	—	80	—		D^2PAK (SMD220)
R_{th} 2	Thermal resistance with 1" square footprint	—	60	—		
R_{th} 3	Thermal resistance junction to case	—	3	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} Tamb=85°C	Continuous drain current			A
	(TAmbient = 85°C, IN = 5V, rth = 60°C/W, Tj = 125°C) IPS031	—	3.1	
	(TAmbient = 85°C, IN = 5V, rth = 80°C/W, Tj = 125°C) IPS031S	—	2.8	
R_{in}	Recommended resistor in series with IN pin	0.2	5	kΩ
$T_{r\text{-}in(max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	μS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. Notes.

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	20	45	60	mΩ	V_{in} = 5V, I_{ds} = 1A
$R_{ds(on)}$	ON state resistance T_j = 150°C	—	75	100		
I_{dss} @Tj=25°C	Drain to source leakage current	0	0.5	25	µA	V_{cc} = 14V, T_j = 25°C
I_{dss2} @Tj=25°C	Drain to source leakage current	0	5	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	47	52	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	53	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to source clamp voltage	7	8.1	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.6	2		I_d = 50mA, Vds = 14V
$I_{in,\ -on}$	ON state IN positive current	25	90	200	µA	V_{in} = 5V
$I_{in,\ -off}$	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 5Ω , Rinput = 50Ω, 100µs pulse,T_j = 25°C, (unless otherwise specified).

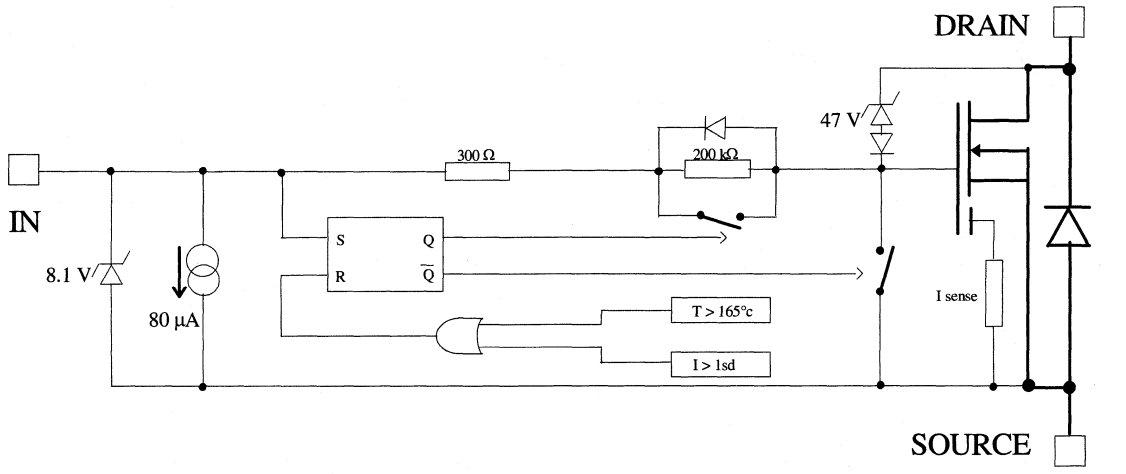
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.05	0.3	0.6	µs	See figure 2
T_r	Rise time	0.4	1	2		
T_{rf}	Time to 130% final $R_{ds(on)}$	—	8	—		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.5	2.5		
Q_{in}	Total gate charge	—	11	—	nC	V_{in} = 5V

Protection Characteristics

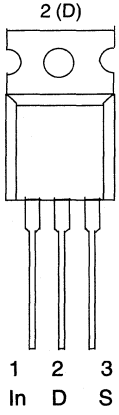
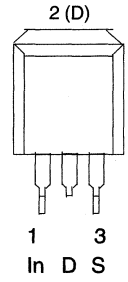
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	10	14	18	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, T_j = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{cc} = 14V

Functional Block Diagram

All values are typical



Lead Assignments

 TO-220	 D²PAK (SMD220)
IPS031	**IPS031S**
Part Number	

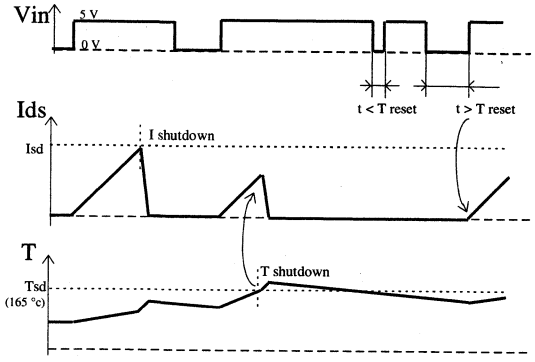


Figure 1 - Timing diagram

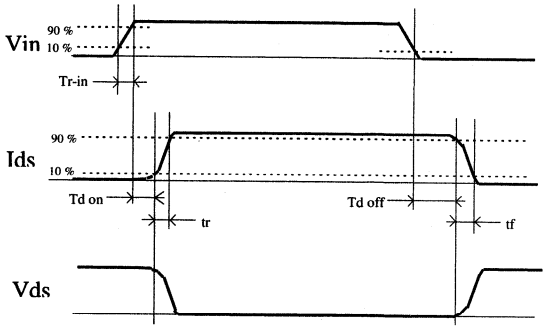


Figure 2 - IN rise time & switching time definitions

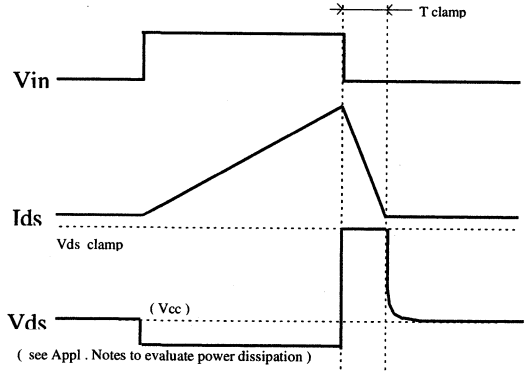


Figure 3 - Active clamp waveforms

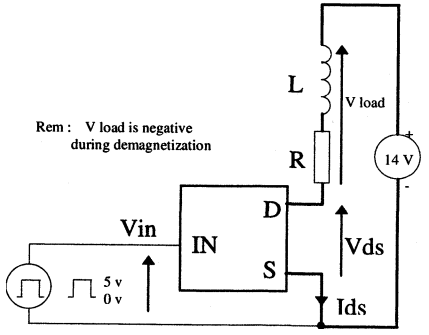


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

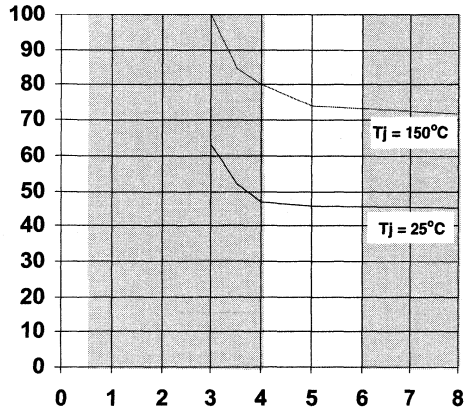


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

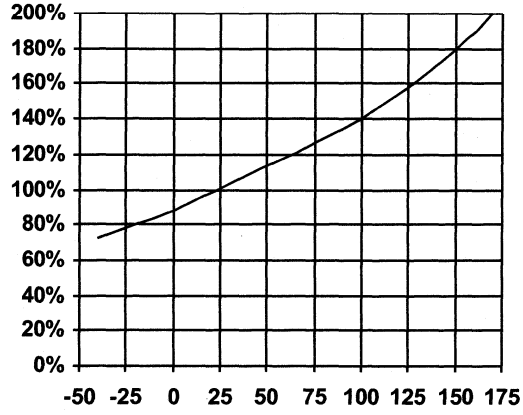


Figure 6 - Normalised Rds ON (%) Vs Tj (°C)

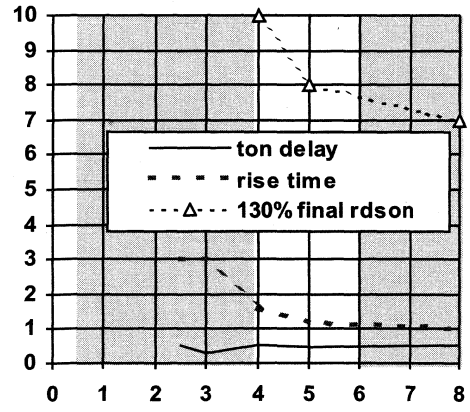


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{ds(on)}$ (us) Vs Input Voltage (V)

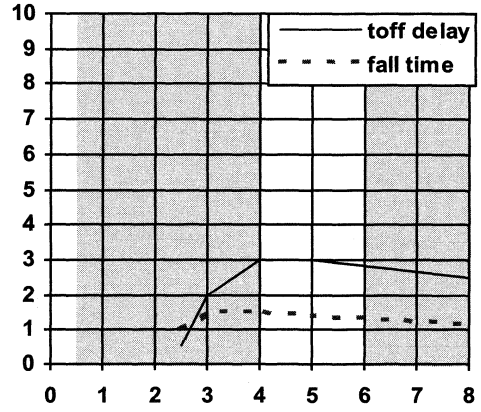


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

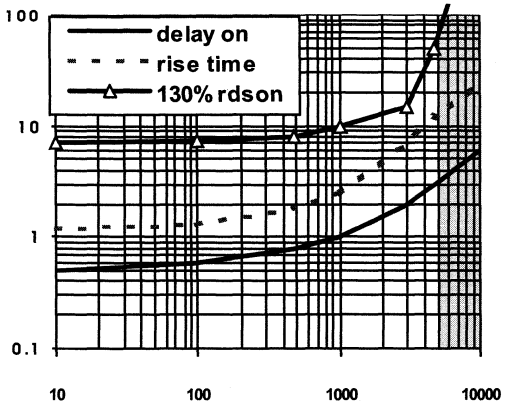


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{ds(on)}$ (us) Vs IN Resistor (Ω)

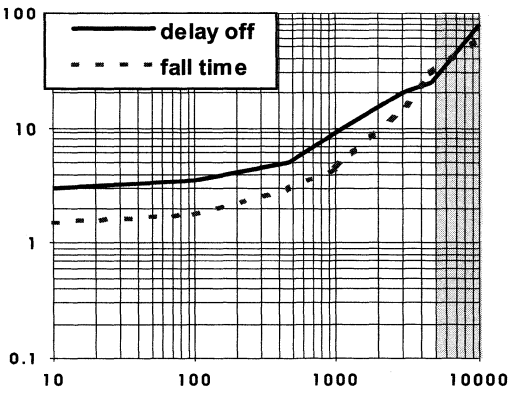


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

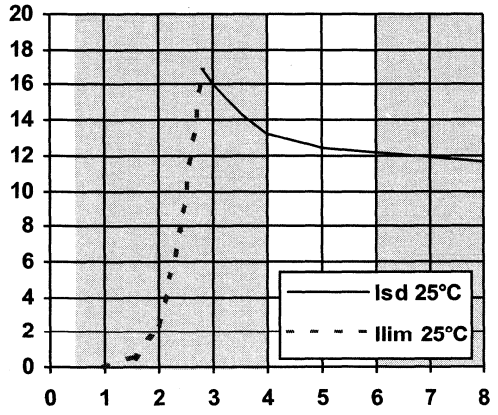


Figure 11 - Current limitation & I shutdown (A) Vs Vin (V)

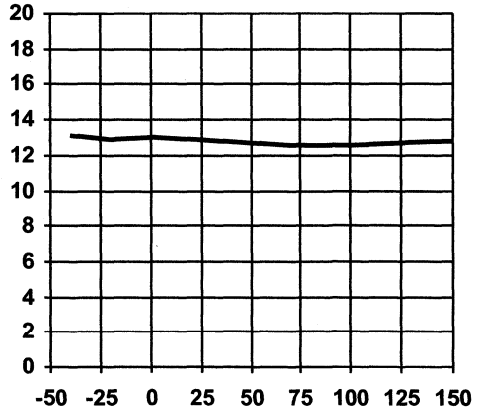


Figure 12 - I shutdown (A) Vs Temperature (°C)

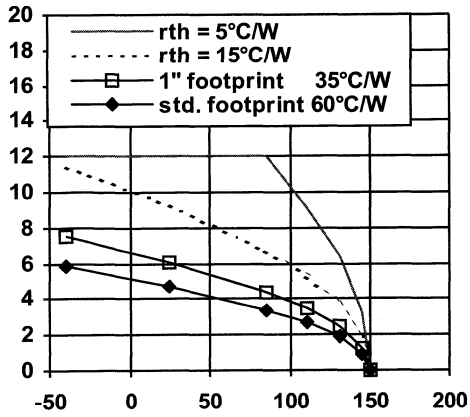


Figure 13 - Max.Cont. Ids (A) Vs Amb. Temperature (°C)

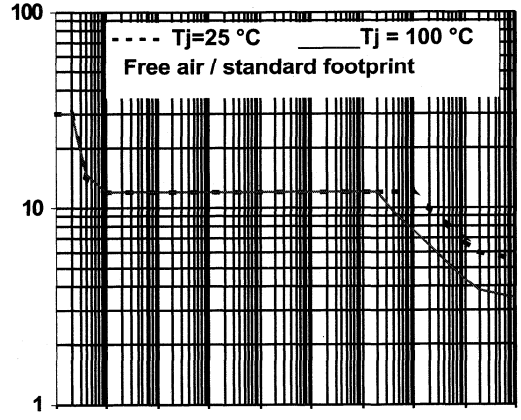


Figure 14 - Ids (A) Vs Protection Resp. Time (s) IPS031 & IPS031S

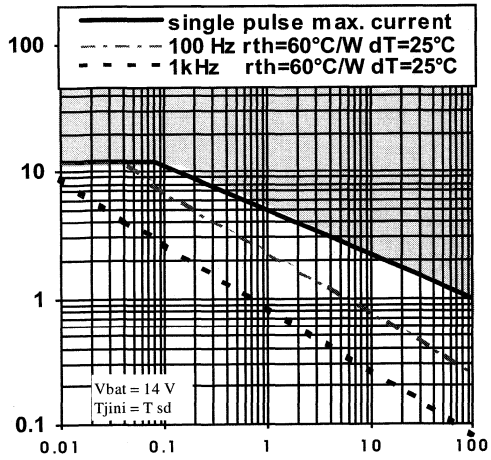


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

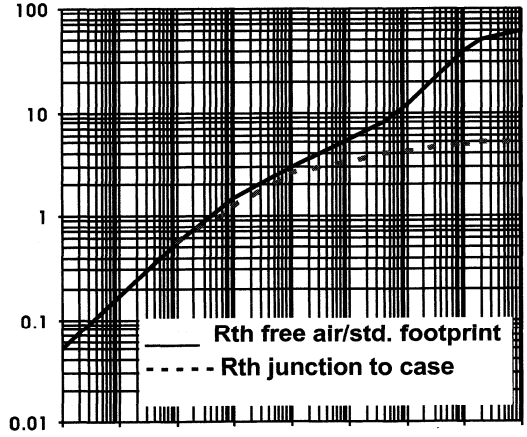


Fig.16 - Transient Thermal Impedance (°C/W) Vs Time (s) - IPS031/IPS031S

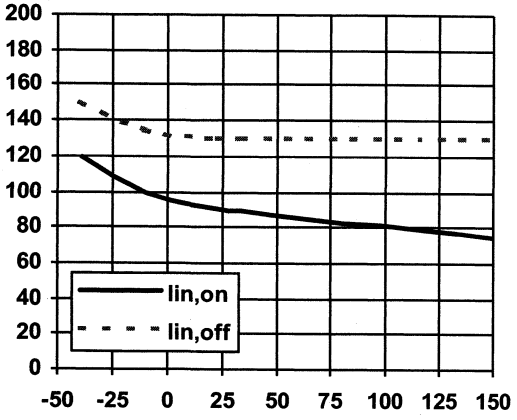


Figure 17 - Input current (μA) Vs Junction (°C)

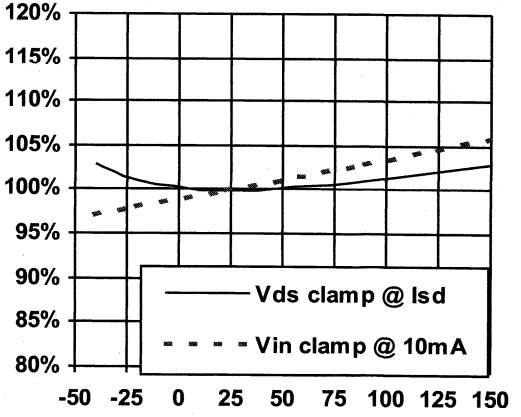


Figure 18 - Vin clamp and V clamp2 (%)
Vs Tj (°C)

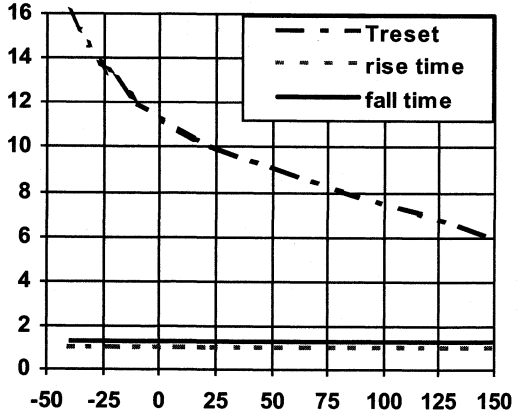
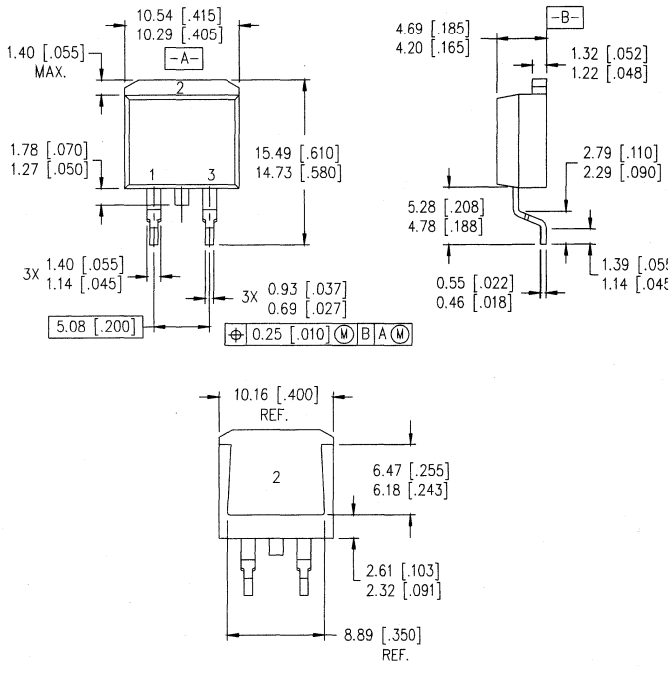


Figure 19 - Turn-on, Turn-off, and treset (μs)
Vs Tj (°C)

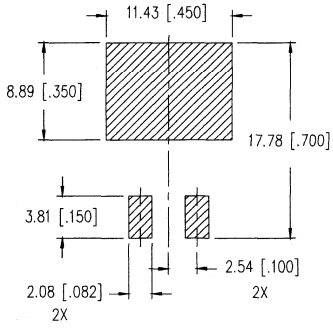
Case Outline 3 Lead - D²PAK (SMD220)



NOTES:

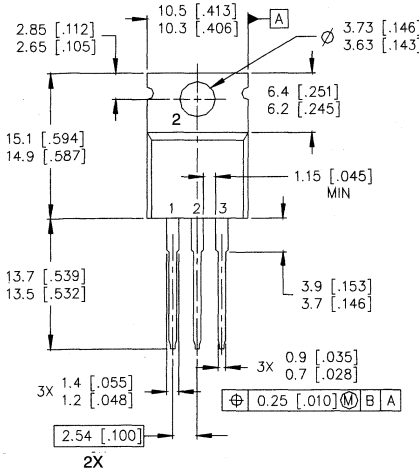
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSIONS AFTER SOLDER DIP.
5. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

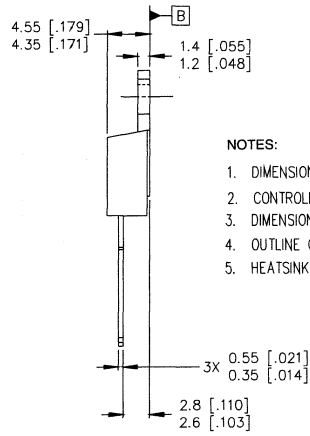
MINIMUM RECOMMENDED FOOTPRINT



01-0016 05

Case Outline 3 Lead - TO220



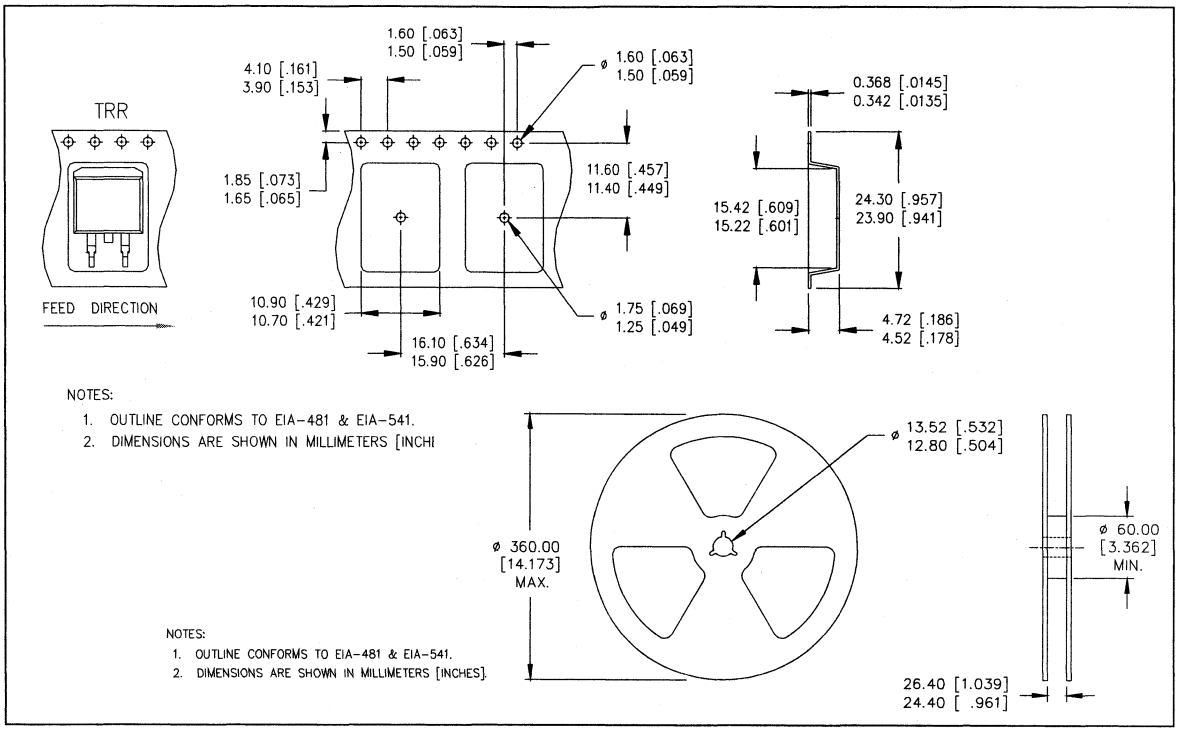


NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
5. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

IRGB 01-3026 01

Tape & Reel - D²PAK (SMD220)



International
IOR Rectifier

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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Data Sheet No.PD 60151-I

IPS031G/IPS032G

SINGLE/DUAL FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

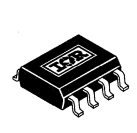
Description

The IPS031G/IPS032G are fully protected single/dual low side SMART POWER MOSFETs that feature over-current, over-temperature, ESD protection and drain to source active clamp.These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning off the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 12A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

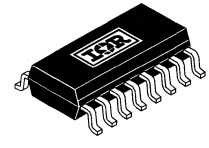
Product Summary

$R_{ds(on)}$	70mΩ (max)
V_{clamp}	50V
Ishutdown	12A
T_{on}/T_{off}	1.5µs

Packages

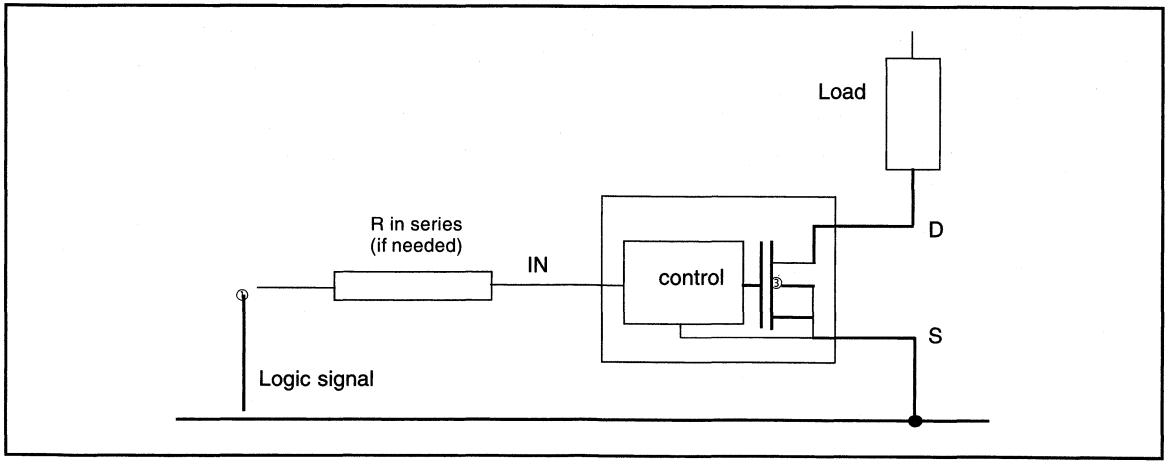


8 Lead SOIC
IPS031G



16 Lead SOIC
IPS032G
(Dual)

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness. All Sources leads of each mosfet must be connected together to get full current capability

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(rth=125°C/W) IPS031G	—	1.4		
	(for all sd mosfets, rth=85°C/W) IPS032G	—	2		
$I_{sd\ pulsed}$	Diode max. pulsed current (1) (for ea. mosfet)	—	15		
P_d	Maximum power dissipation(1)			W	
	(rth=125°C/W) IPS031G	—	1		
	(for all Pd mosfets, rth=85°C/W) IPS032G	—	1.5		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	

Thermal Chacteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint	—	100	—	°C/W	SOIC-8
R_{th2}	Thermal resistance with 1" square footprint	—	65	—		
R_{th1} (2 mos on)	Thermal resistance with standard footprint (2 mosfets on)	—	85	—		SOIC-16
R_{th2} (1 mos on)	Thermal resistance with standard footprint (1 mosfet on)	—	100	—		
R_{th3} (2 mos on)	Thermal resistance with 1" square footprint (2 mosfets on)	—	60	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous Drain to Source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} $T_{amb=85°C}$	Continuous drain current (TAmbient = 85°C, IN = 5V, rth = 100°C/W, Tj = 125°C) IPS031G	—	2.2	A
	(TAmbient = 85°C, IN = 5V, rth = 85°C/W, Tj = 125°C) IPS032G	—	1.65	
R_{in}	Recommended resistor in series with IN pin	0.2	5	kΩ
Tr-in(max)	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
Fr-Isc (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	20	45	60	mΩ	V_{in} = 5V, I_{ds} = 1A
$R_{ds(on)}$	ON state resistance T_j = 150°C	—	75	100		
I_{dss} @Tj=25°C	Drain to source leakage current	0	0.5	25	µA	V_{cc} = 14V, T_j = 25°C
I_{dss2} @Tj=25°C	Drain to source leakage current	0	5	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	47	52	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	53	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to source clamp voltage	7	8.1	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.6	2		I_d = 50mA, Vds = 14V
Iin, -on	ON state IN positive current	25	90	200	µA	V_{in} = 5V
Iin, -off	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

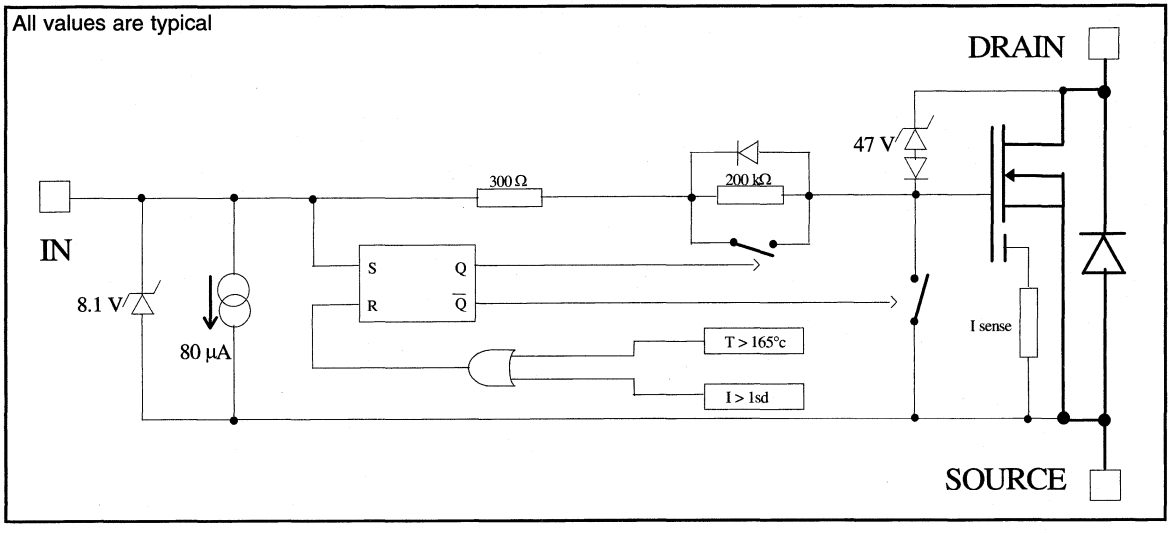
V_{cc} = 14V, Resistive Load = 5Ω (IPS031), Resistive Load = 3Ω (IPS031S), Rinput = 50Ω, 100µs pulse, T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.05	0.3	0.6	µs	See figure 2
T_r	Rise time	0.4	1	2		
T_{rf}	Time to 130% final $R_{ds(on)}$	—	8	—		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.5	2.5		
Q_{in}	Total gate charge	—	1.1	—	nC	V_{in} = 5V

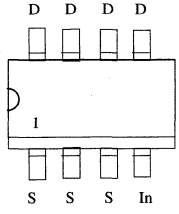
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	10	14	18	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{cc} = 14V

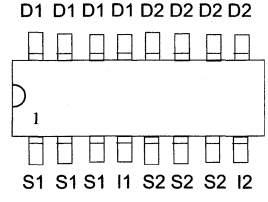
Functional Block Diagram



Lead Assignments



8 Lead SOIC



16 Lead SOIC
(Dual)

IPS031G	IPS032G
Part Number	

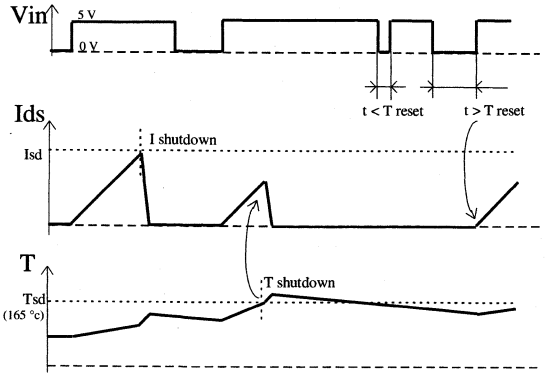


Figure 1 - Timing diagram

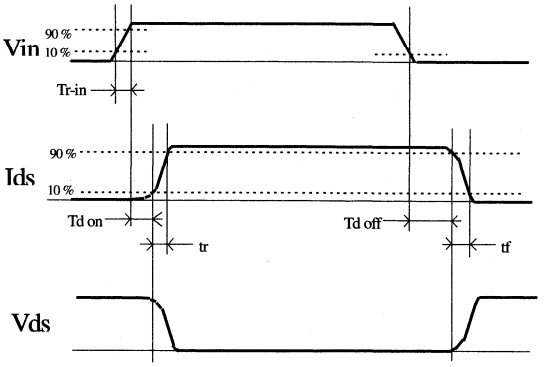


Figure 2 - IN rise time & switching time definitions

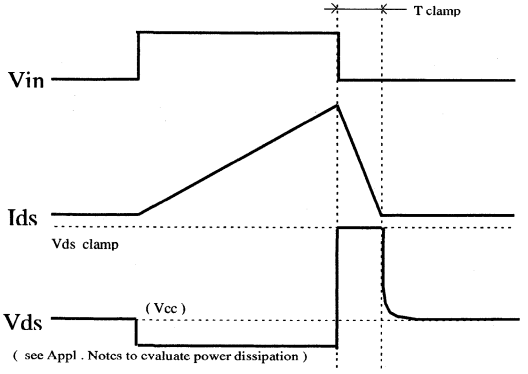


Figure 3 - Active clamp waveforms

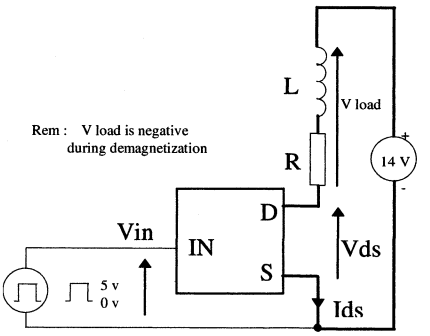


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

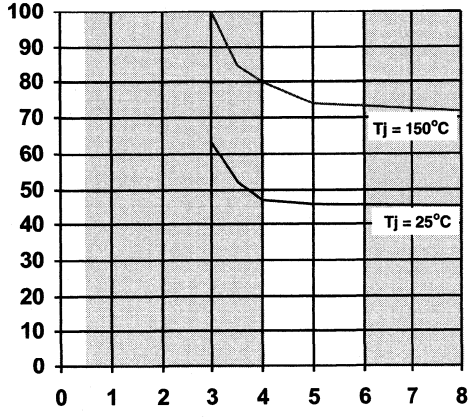


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

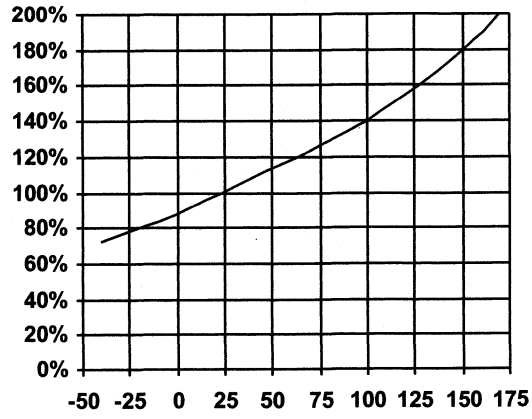


Figure 6 - Normalised Rds ON (%) Vs Tj (°C)

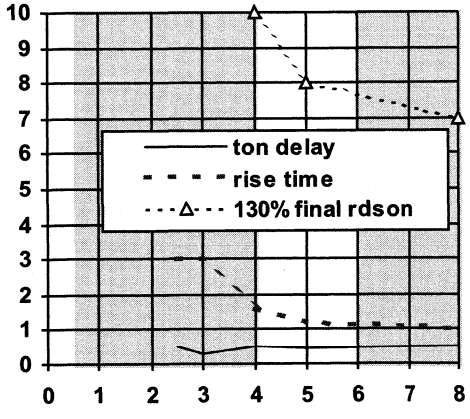


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs Input Voltage (V)

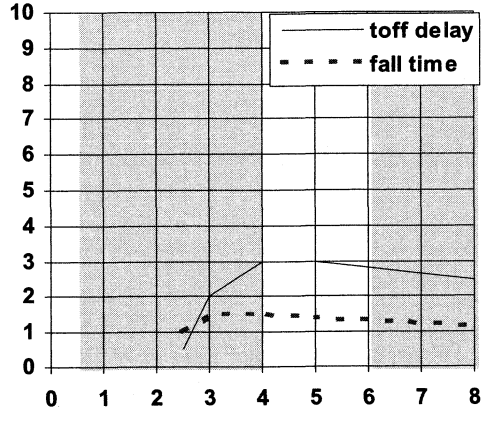


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

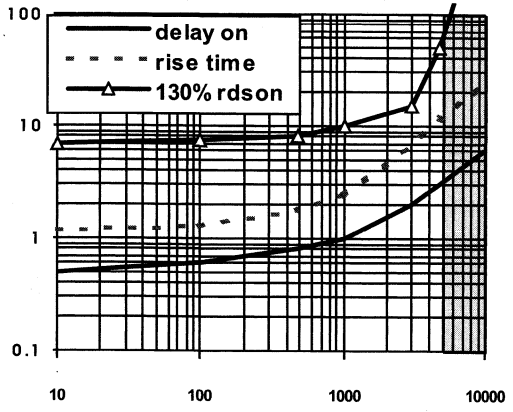


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) Vs IN Resistor (Ω)

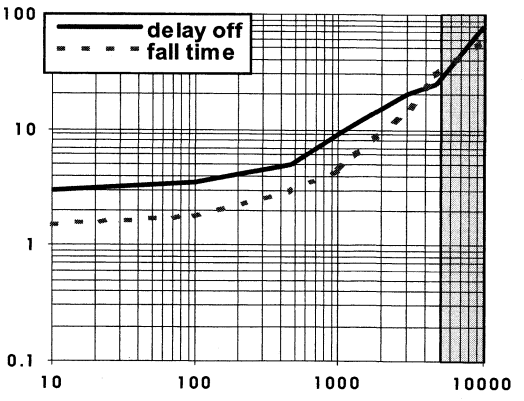


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

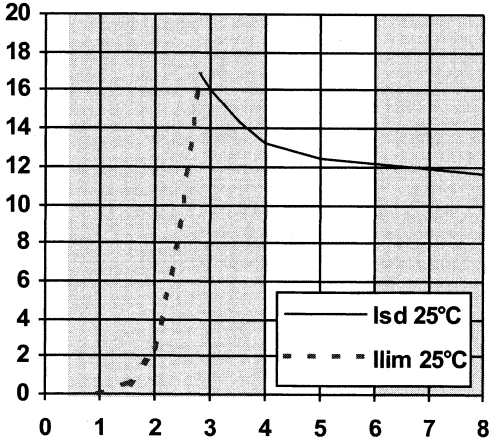


Figure 11 - Current limimitation & I shutdown (A) Vs Vin (V)

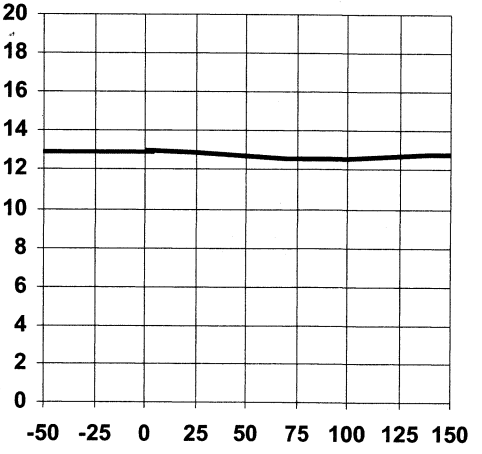


Figure 12 - I shutdown (A) Vs Temperature (°C)

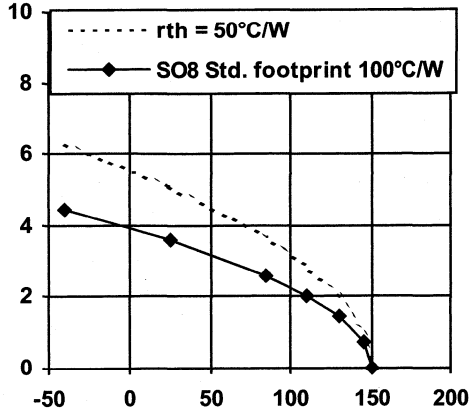


Figure 13a - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS031G

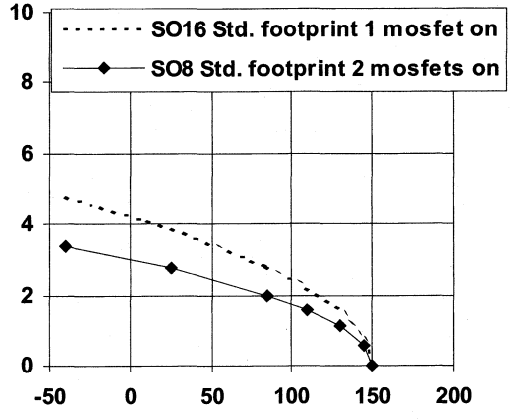


Figure 13b - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS032G

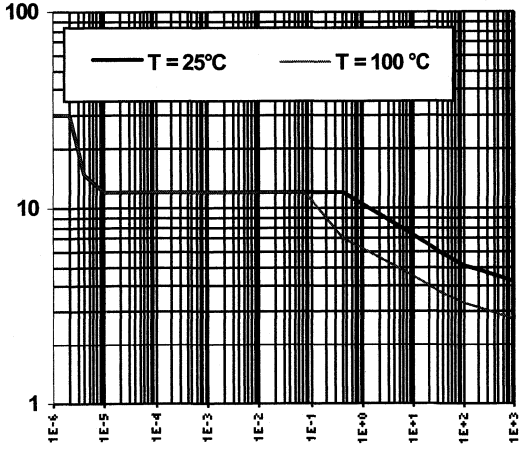


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
IPS031G/IPS032G

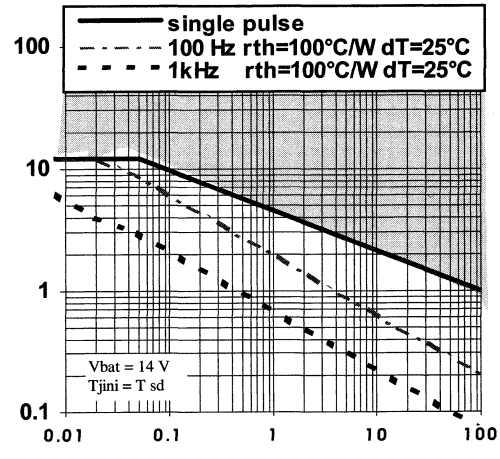


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

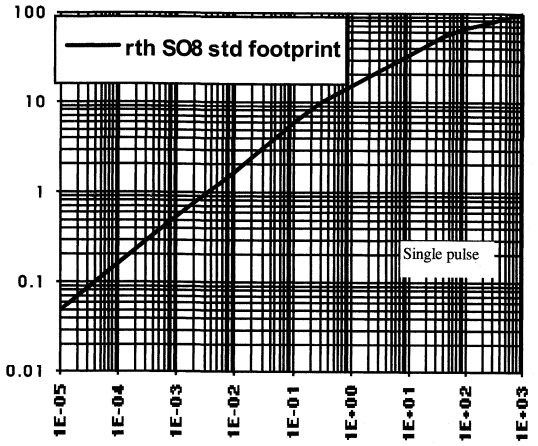


Figure 16a - Transient Thermal Imped. (°C/W) Vs Time (s) - IPS031G

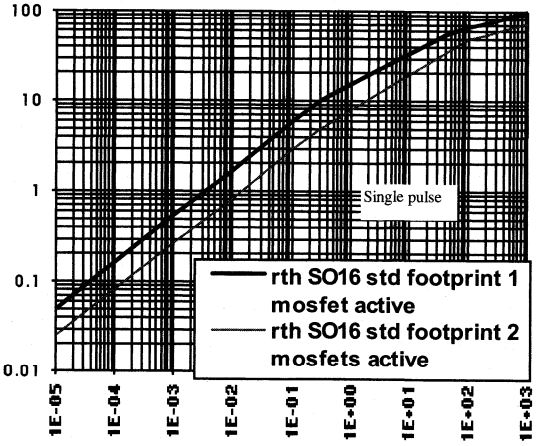


Figure 16b - Transient Thermal Imped. (°C/W) Vs Time (s) - IPS032G

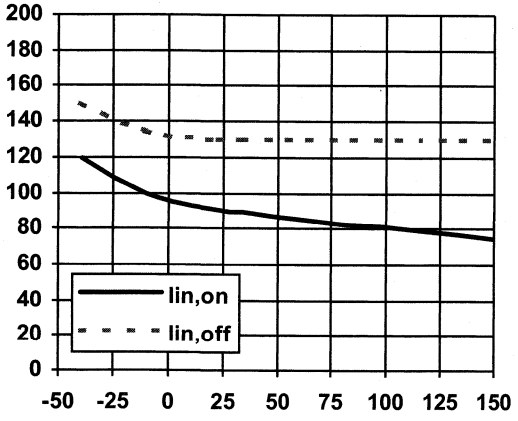


Figure 17 - Input current (μA) Vs Tj (°C)

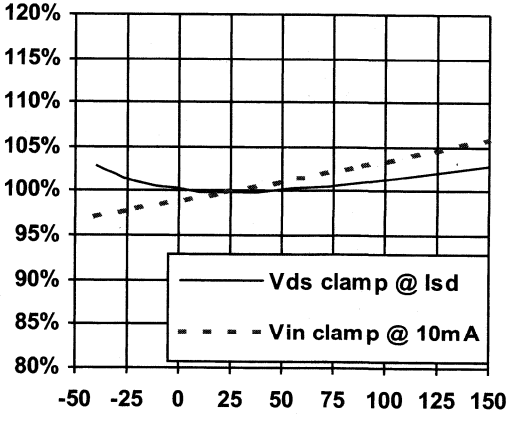


Figure 18 - Vin clamp and V clamp2 (%) Vs Tj (°C)

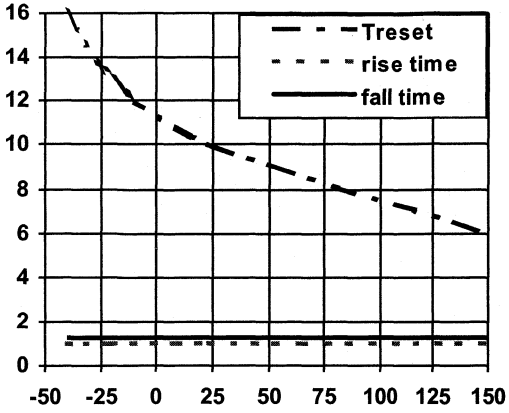
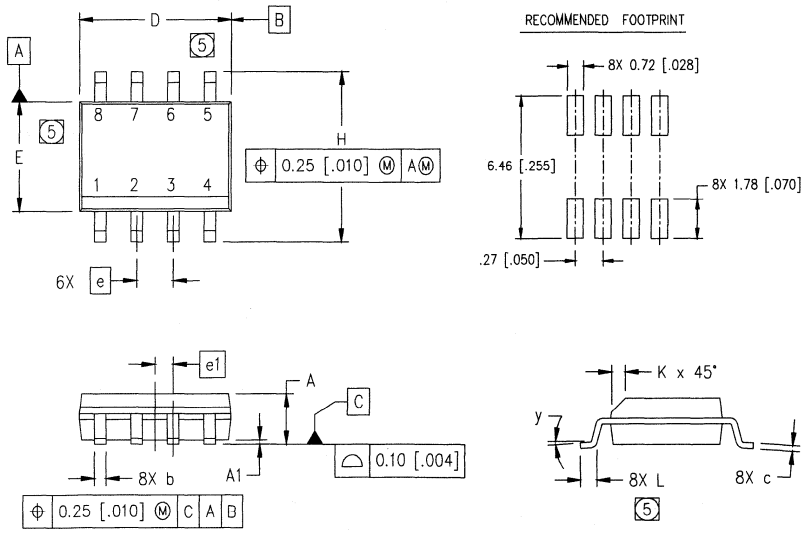


Figure 19 - Turn-on, Turn-off, and Treset (us)
Vs Tj (°C)

Case Outline - 8 Lead SOIC



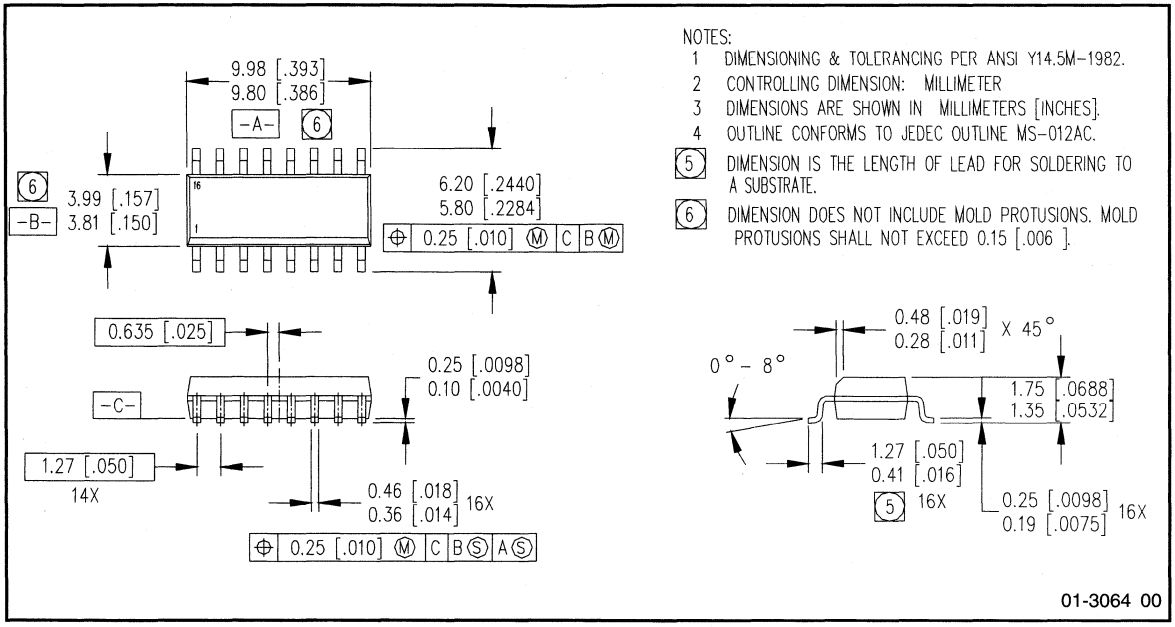
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

Case Outline - 16 Lead SOIC (narrow body)



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Data Sheet No.PD 60152-I

IPS041L

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

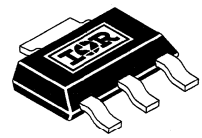
Description

The IPS041L is a fully protected three terminal SMART POWER MOSFET that features over-current, over-temperature, ESD protection and drain to source active clamp.This device combines a HEXFET® POWER MOSFET and a gate driver. It offers full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the Drain current reaches 2A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

Product Summary

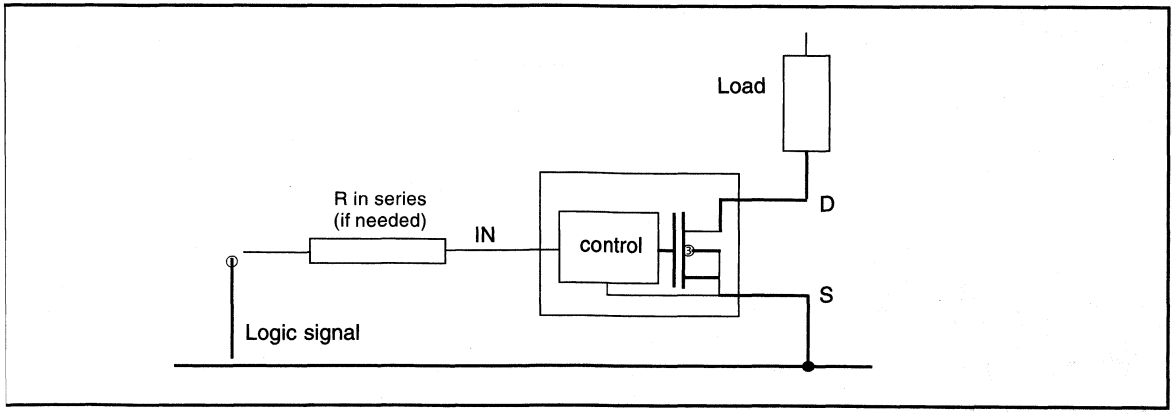
$R_{ds(on)}$	500mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	2A
T_{on}/T_{off}	1.5µs

Package



3 Lead SOT223

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicates sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 μr copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1) (rth=125°C/W)	—	1.2	A	
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	3		
P_d	Maximum power dissipation(1) (rth=125°C/W)	—	1	W	
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint	—	100	—	°C/W	
R_{th2}	Thermal resistance with 1" square footprint	—	60	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
$I_{ds\ Tamb=85°C}$	Continuous drain current (TAmbient = 85°C, IN = 5V, rth = 100°C/W, Tj = 125°C)	—	0.75	A
R_{in}	Recommended resistor in series with IN pin	1	5	kΩ
Tr-in(max)	Max recommended rise time for IN signal (see fig. 2)	—	1	μS
Fr-Isc (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. notes.

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	—	370	500	mΩ	V_{in} = 5V, I_{ds} = 1A
	T_j = 150°C	—	590	900		
I_{dss1} @Tj=25°C	Drain to source leakage current	0	0.5	25	µA	V_{cc} = 14V, T_j = 25°C
I_{dss2} @Tj=25°C	Drain to source leakage current	0	5	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to Source clamp voltage 1	47	52	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to Source clamp voltage 2	50	53	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to Source clamp voltage	7	8.1	9.5		I_{in} = 1 mA
$V_{in\ th}$	IN threshold voltage	1	1.6	2		I_d = 50mA, V_{ds} = 14V
$I_{in,\ -on}$	ON state IN positive current	25	90	200	µA	V_{in} = 5V
$I_{in,\ -off}$	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 20Ω, Rinput = 1kΩ, 100µs pulse, T_j = 25°C, (unless otherwise specified).

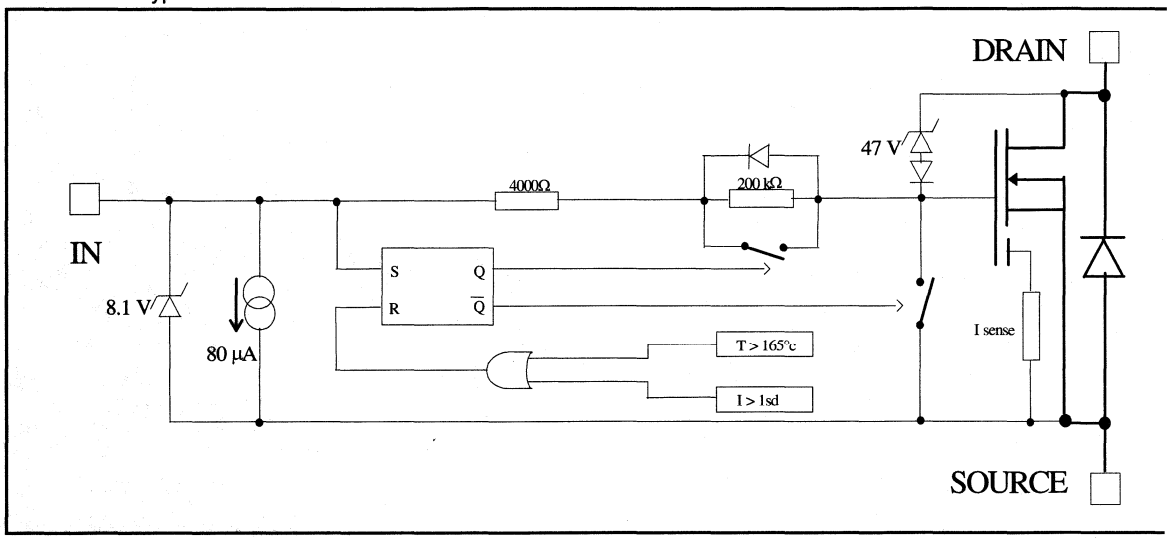
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.05	0.2	0.5	µs	See figure 2
T_r	Rise time	0.5	1.3	2.5		
T_{rf}	Time to 130% final $R_{ds(on)}$	—	5	—		
T_{off}	Turn-off delay time	0.5	1.6	2.5		See figure 2
T_f	Fall time	0.5	1.5	2.5		
Q_{in}	Total gate charge	—	1	—	nC	V_{in} = 5V

Protection Characteristics

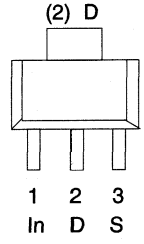
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	1.1	1.7	2.2	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{cc} = 14V

Functional Block Diagram

All values are typical



Lead Assignments



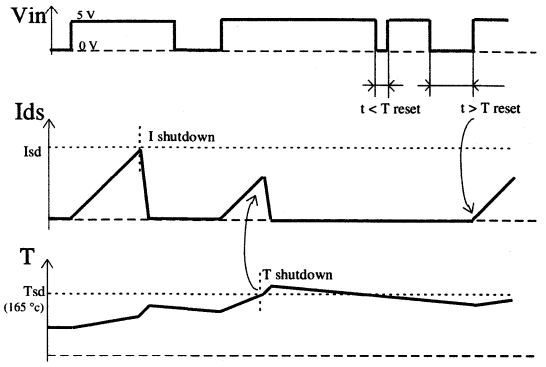


Figure 1 - Timing diagram

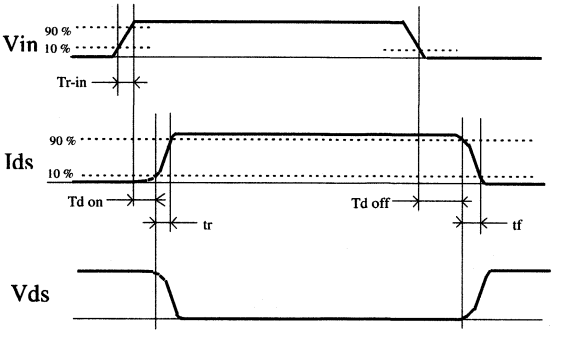


Figure 2 - IN rise time & switching time definitions

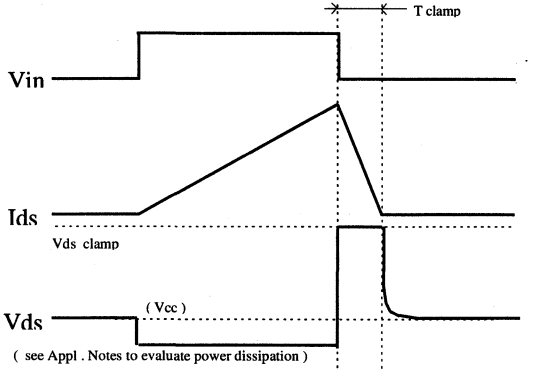


Figure 3 - Active clamp waveforms

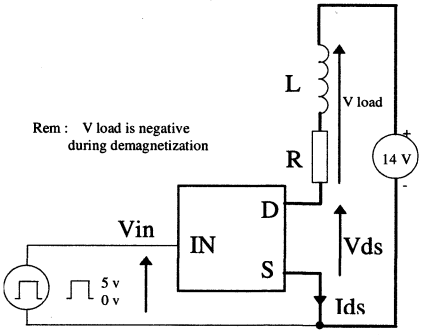


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

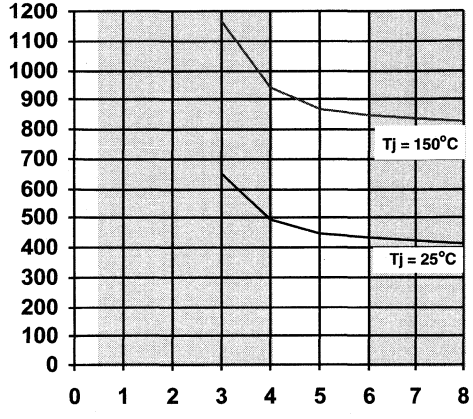


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

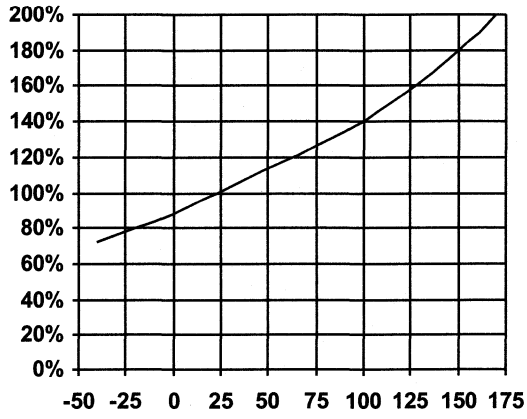


Figure 6 - Normalised Rds ON (%) Vs Tj (°C)

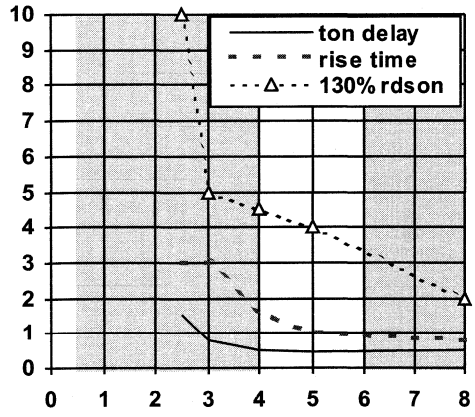


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs Input Voltage (V)

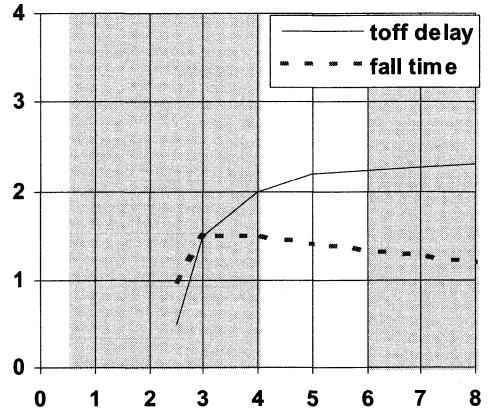


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

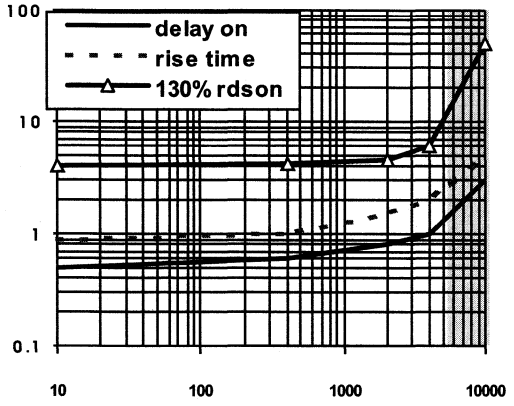


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs IN Resistor (Ω)

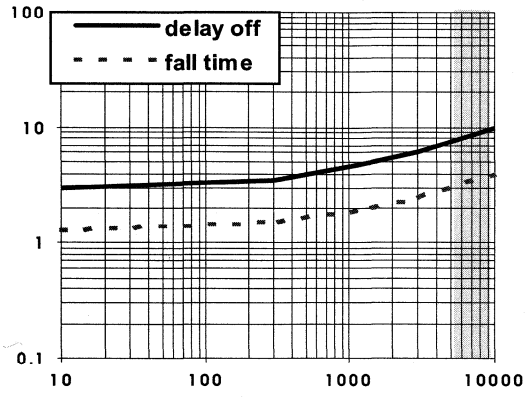


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

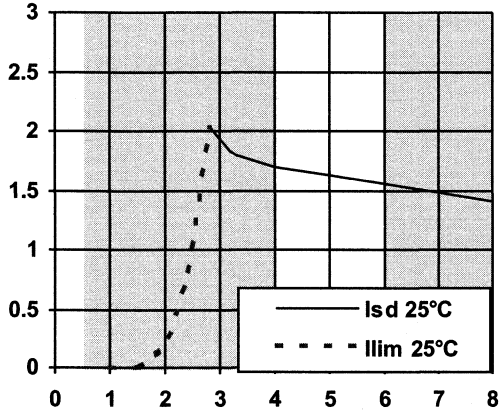


Figure 11 - Current Iim. & I shutdown (A) Vs Vin (V)

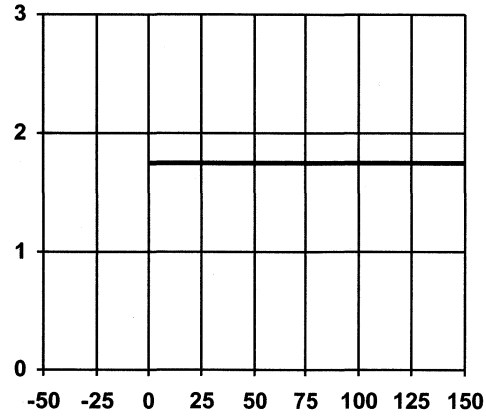


Figure 12 - I shutdown (A) Vs Temperature (°C)

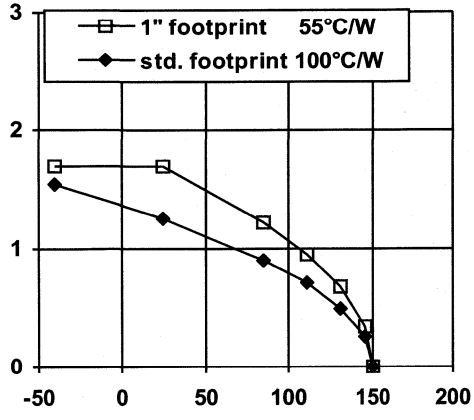


Figure 13 - Max.Cont. Ids (A) Vs Amb. Temperature (°C)

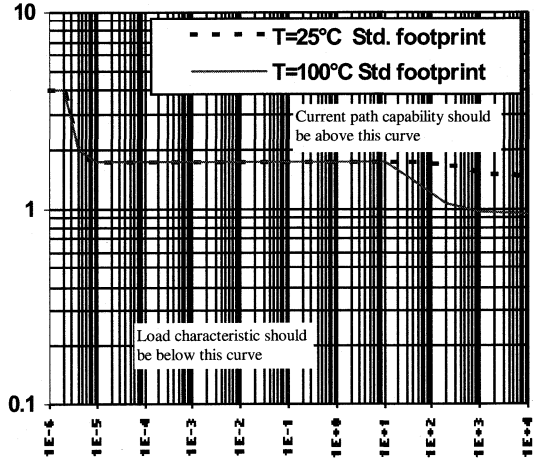


Figure 14 - Ids (A) Vs Protection Resp.Time (s)

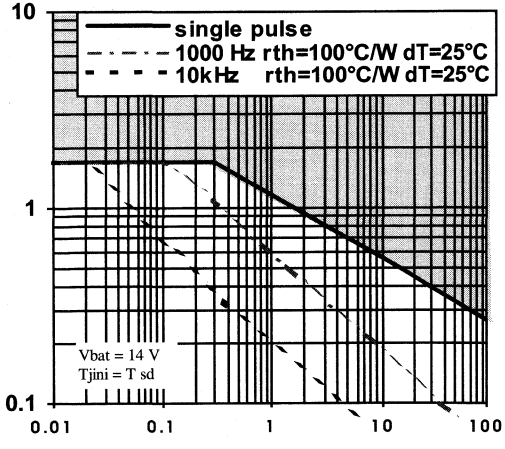


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

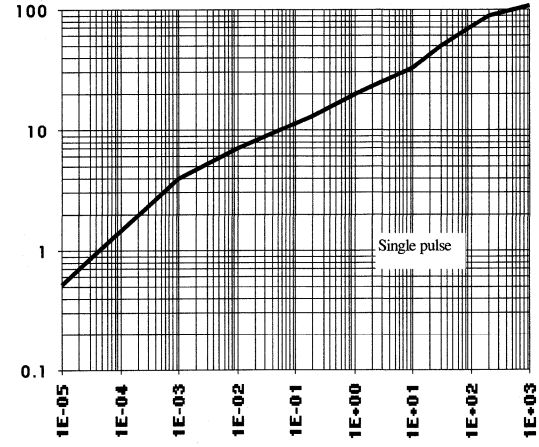


Figure 16 - Transient Thermal Imped. (°C/W) Vs Time (s)

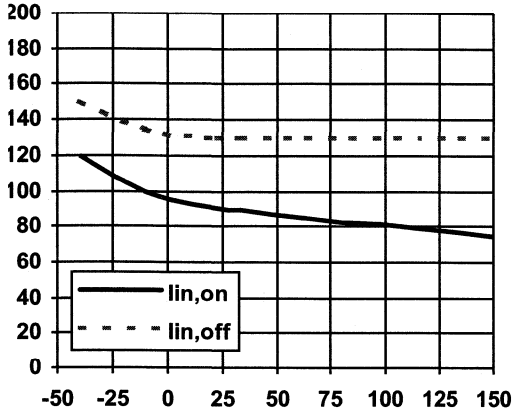


Figure 17 - Input current (μA) Vs Tj (°C)

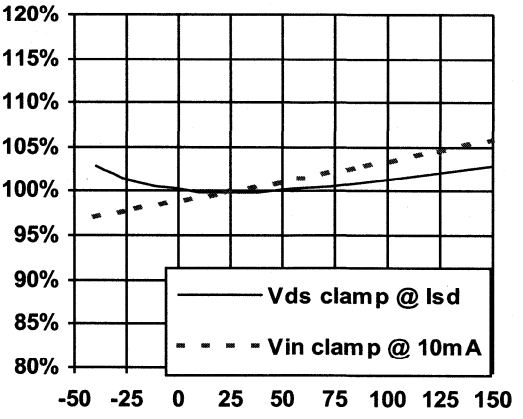


Figure 18 - Vin clamp and V clamp2 (%) Vs Tj (°C)

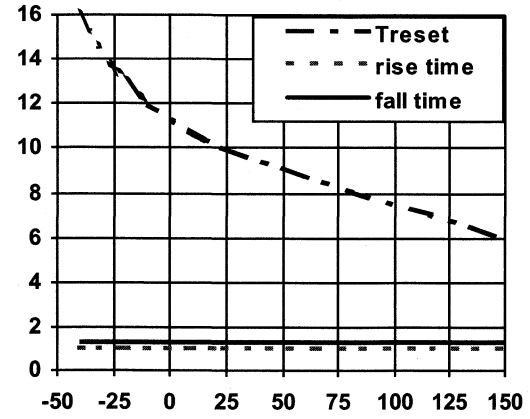
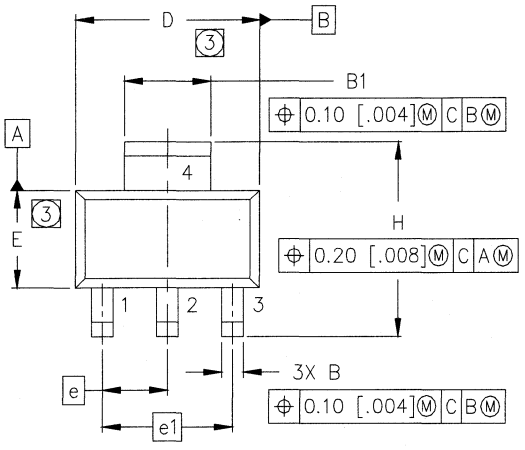
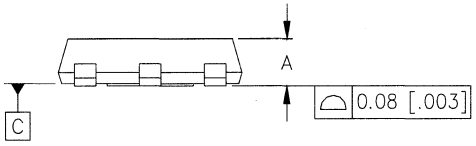
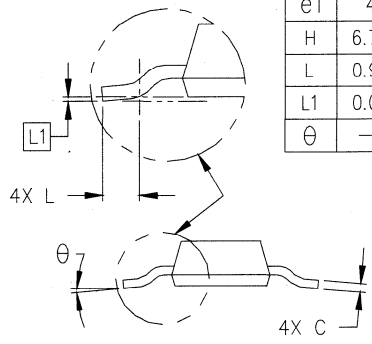


Figure 19 - Turn-on, Turn-off, and Treset (μs) Vs Tj (°C)

Case Outline - SOT-223

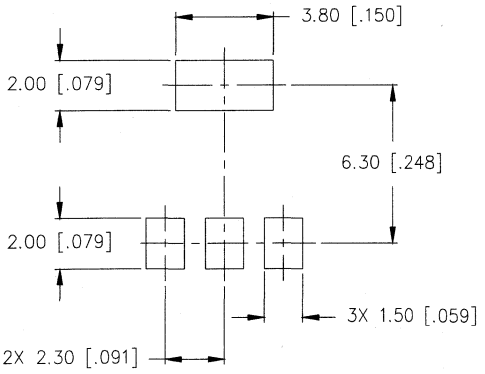






DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.55	1.80	.061	.071
B	0.65	0.85	.026	.033
B1	2.95	3.15	.116	.124
C	0.25	0.35	.010	.014
D	6.30	6.70	.248	.264
E	3.30	3.70	.130	.146
e	2.30 BSC		.0905 BSC	
e1	4.60 BSC		.181 BSC	
H	6.71	7.29	.264	.287
L	0.91	—	.036	—
L1	0.061 BSC		.0024 BSC	
θ	—	10°	—	10°

MINIMUM RECOMMENDED FOOTPRINT



LEAD ASSIGNMENTS

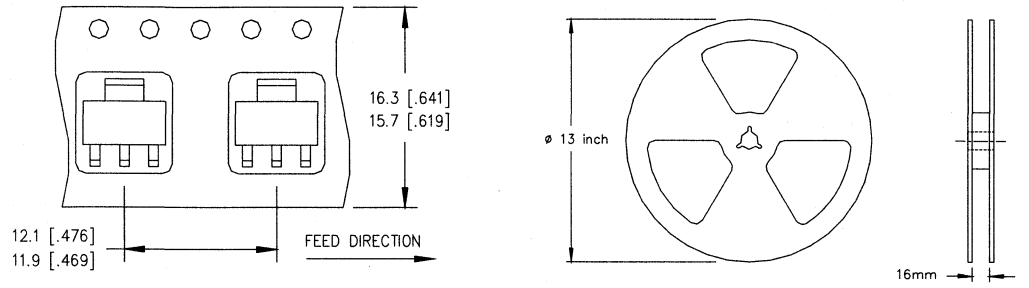
1 = GATE
2 = DRAIN
3 = SOURCE

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

(TO-261AA) 01-0022 05

Tape & Reel - SOT223



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.
4. EACH ø 330.00 [ø 13.00] REEL CONTAINS 2,500 DEVICES.

01-0028 05 / 01-0008 02

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

IPS042G

DUAL FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

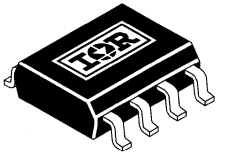
Description

The IPS042G is a fully protected dual low side SMART POWER MOSFET that features over-current, over-temperature, ESD protection and drain to source active clamp.This device combines a HEXFET® POWER MOSFET and a gate driver. It offers full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 2A. This device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

Product Summary

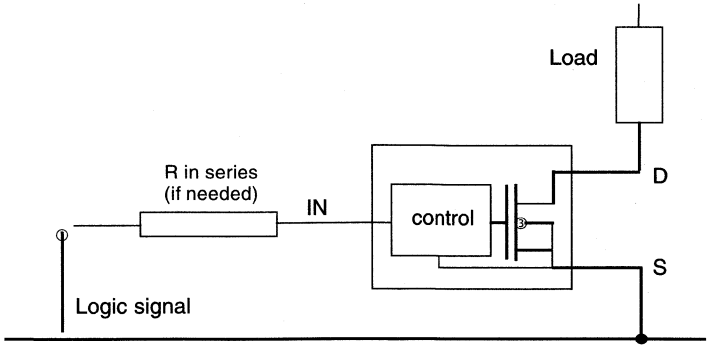
$R_{ds(on)}$	500mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	2A
T_{on}/T_{off}	1.5µs

Package



8 Lead SOIC

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 µm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(for all Isd mosfets, rth=125°C/W)	—	1.2		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	3		
P_d	Maximum power dissipation (1)			W	
	(for all Pd mosfets, rth=125°C/W)	—	1		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10µH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint (2 mosfets on)	—	100	—	°C/W	
R_{th2}	Thermal resistance with standard footprint (1 mosfet on)	—	125	—		
R_{th3}	Thermal resistance with 1" square footprint (2 mosfets on)	—	65	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous Drain to Source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} $_{Tamb=85°C}$	Continuous drain current (both mosfets at this current) TAmbient = 85°C, IN = 5V, rth = 100°C/W, Tj = 125°C	—	0.53	A
R_{in}	Recommended resistor in series with IN pin	1	5	kΩ
$T_{r\text{-}in(max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. notes.

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	—	370	500	mΩ	V_{in} = 5V, I_{ds} = 1A
	T_j = 150°C	—	590	900		
I_{dss1} @Tj=25°C	Drain to source leakage current	0	0.5	25	µA	V_{cc} = 14V, T_j = 25°C
I_{dss2} @Tj=25°C	Drain to source leakage current	0	5	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to Source clamp voltage 1	47	52	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to Source clamp voltage 2	50	53	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to Source clamp voltage	7	8.1	9.5		I_{in} = 1 mA
$V_{in\ th}$	IN threshold voltage	1	1.6	2		I_d = 50mA, V_{ds} = 14V
$I_{in,\ -on}$	ON state IN positive current	25	90	200	µA	V_{in} = 5V
$I_{in,\ -off}$	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 20Ω, Rinput = 1kΩ, 100µs pulse, T_j = 25°C, (unless otherwise specified).

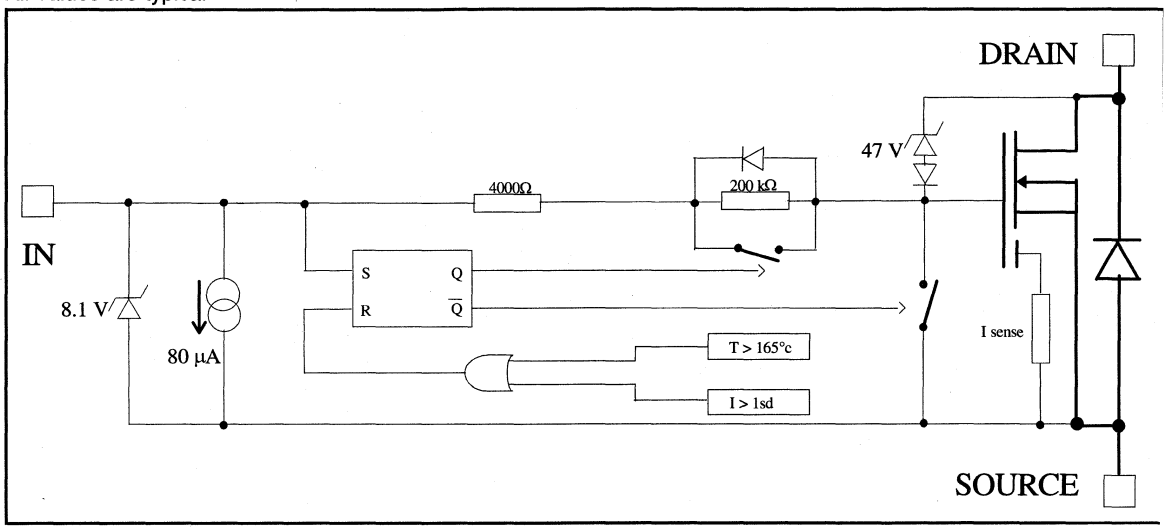
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.05	0.2	0.5	µs	See figure 2
T_r	Rise time	0.5	1.3	2.5		
T_{rf}	Time to 130% final $R_{ds(on)}$	—	5	—		
T_{off}	Turn-off delay time	0.5	1.6	2.5		See figure 2
T_f	Fall time	0.5	1.5	2.5		
Q_{in}	Total gate charge	—	1	—	nC	V_{in} = 5V

Protection Characteristics

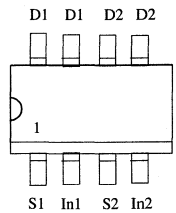
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	1.1	1.7	2.2	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, T_j = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{cc} = 14V

Functional Block Diagram

All values are typical



Lead Assignments



8 Lead SOIC

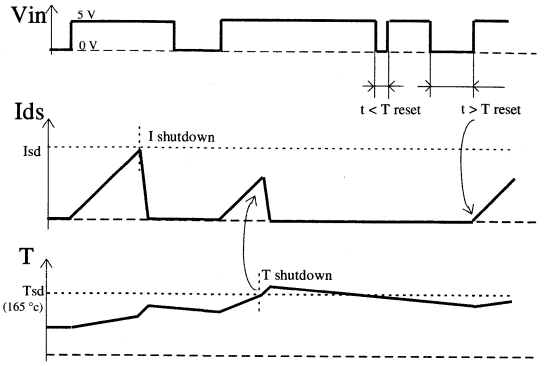


Figure 1 - Timing diagram

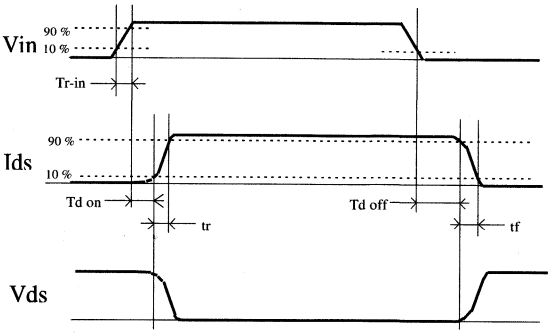


Figure 2 - IN rise time & switching time definitions

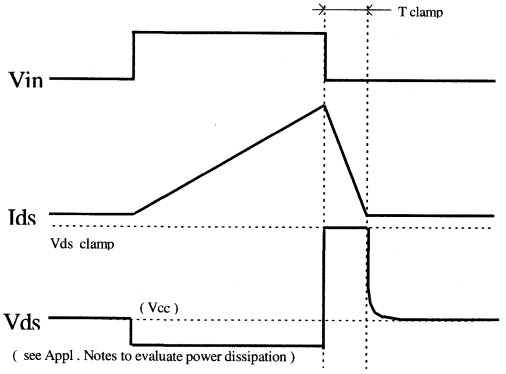


Figure 3 - Active clamp waveforms

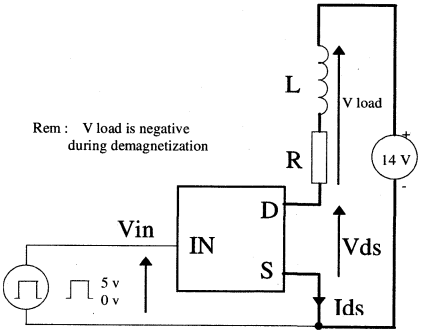


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

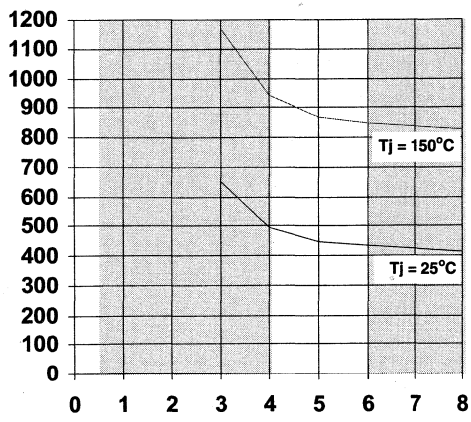


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

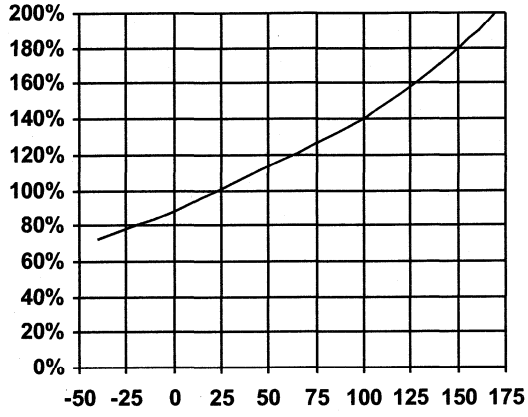


Figure 6 - Normalised Rds ON (%) Vs Tj (°C)

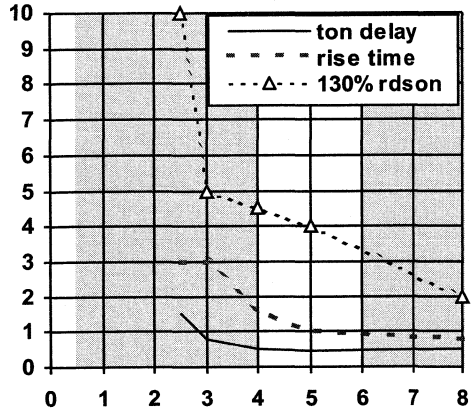


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs Input Voltage (V)

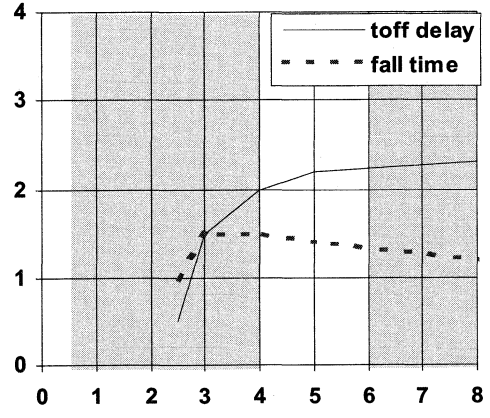


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

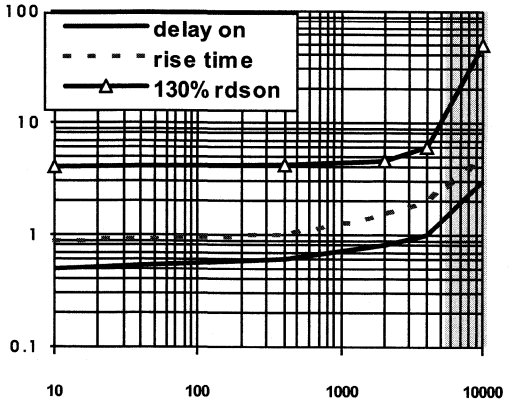


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs IN Resistor (Ω)

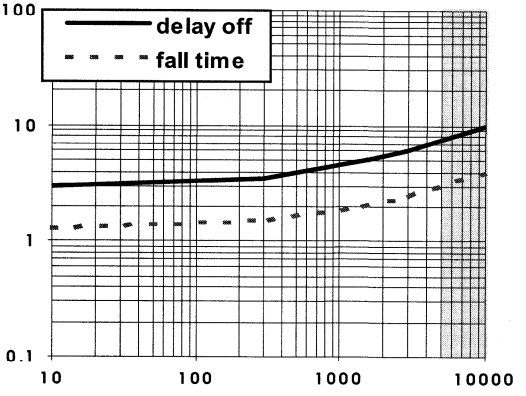


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

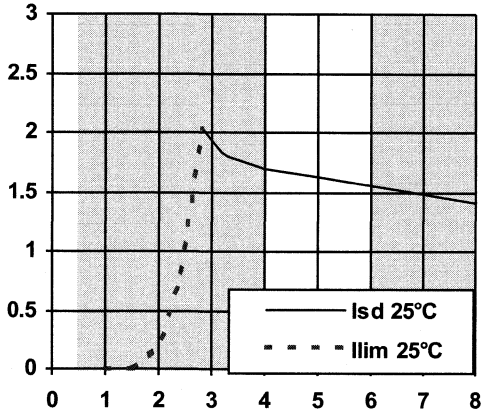


Figure 11 - Current Iim. & I shutdown (A) Vs Vin (V)

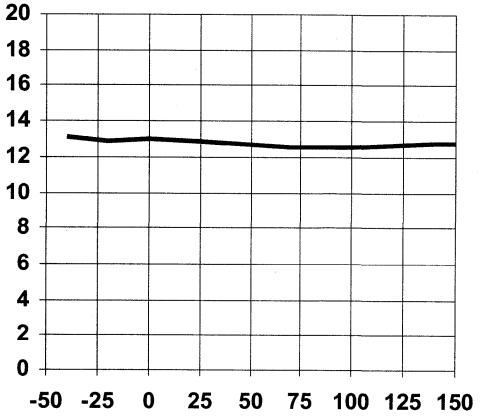


Figure 12 - I shutdown (A) Vs Temperature (°C)

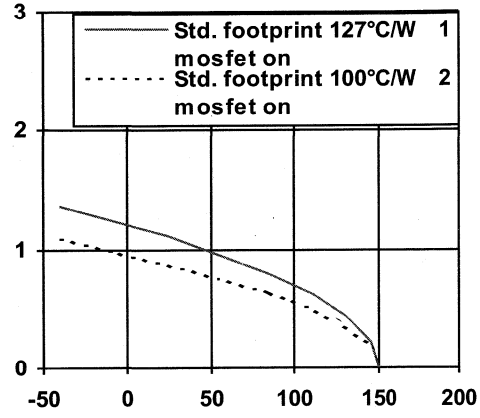


Figure 13 - Max.Cont. Ids (A) Vs Amb. Temperature (°C)

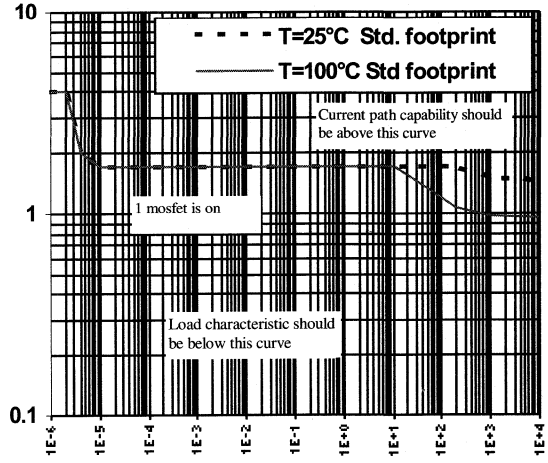


Figure 14 - Ids (A) Vs Protection Resp. Time (s)

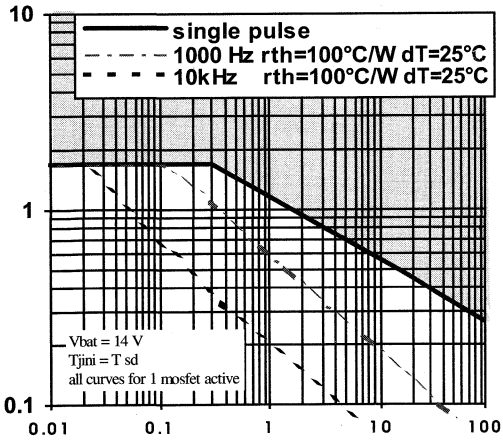


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

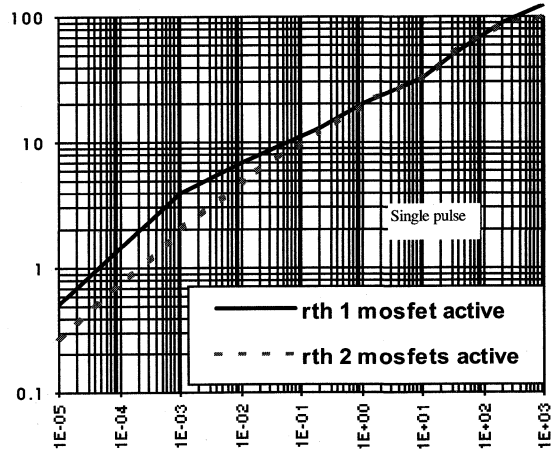


Figure 16 - Transient Thermal Imped. (°C/W) Vs Time (s)

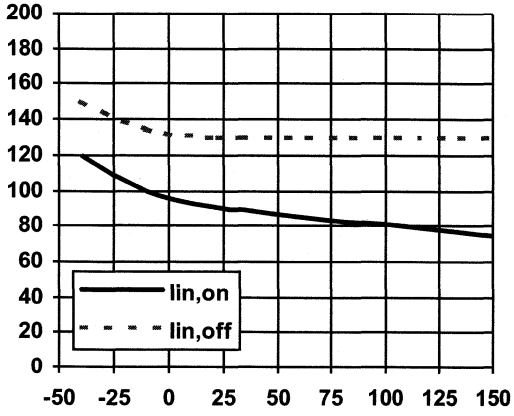


Figure 17 - Input current (μA) Vs Tj (°C)

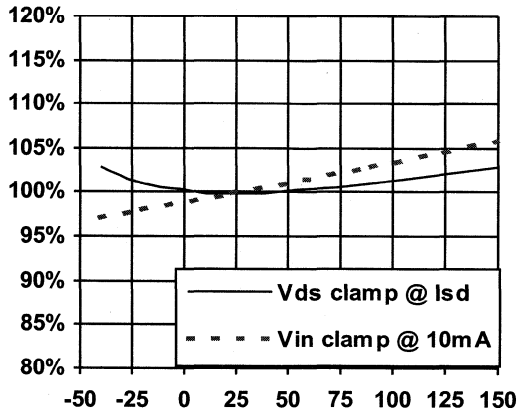


Figure 18 - Vin clamp and V clamp2 (%) Vs Tj (°C)

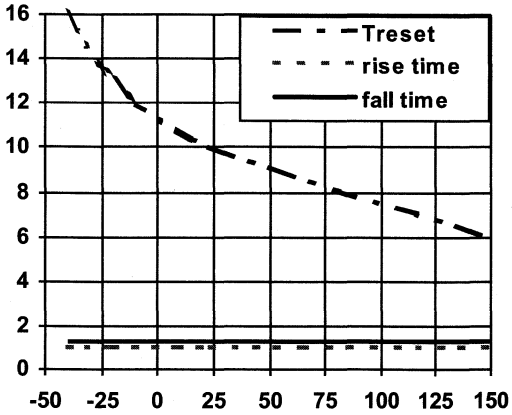
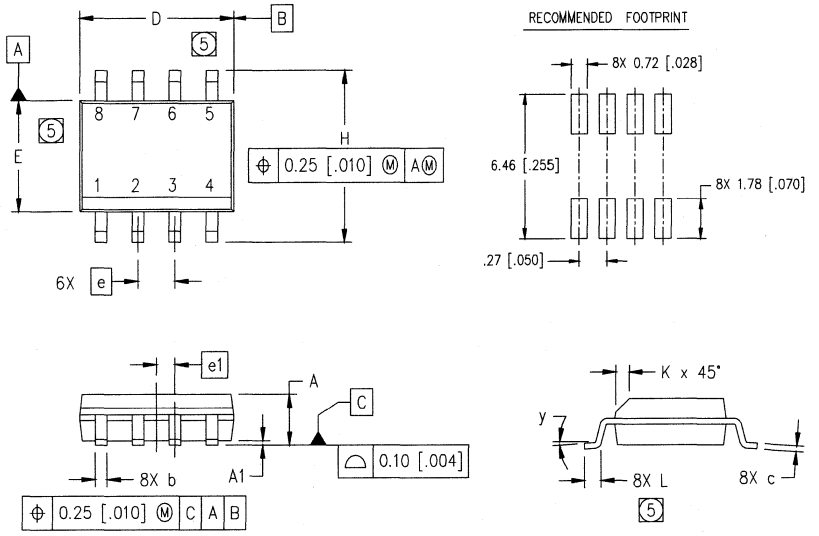


Figure 19 - Turn-on, Turn-off, and Treset (μs) Vs Tj (°C)

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

International
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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
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IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

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Data Sheet No. PD60160-A

IPS0551T

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

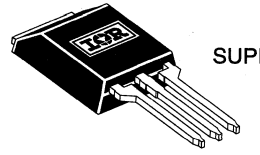
Description

The IPS0551T is a fully protected three terminal SMART POWER MOSFET that features over-current, over-temperature, ESD protection, and drain to source active clamp. This device combines a HEXFET® POWER MOSFET and a gate driver. It offers full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when temperature exceeds 165°C or when the drain current reaches 100A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

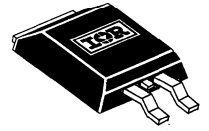
Product Summary

$R_{ds(on)}$	5.2mΩ (max)
V_{clamp}	40V
Ishutdown	100A
T_{on}/T_{off}	4μs

Package

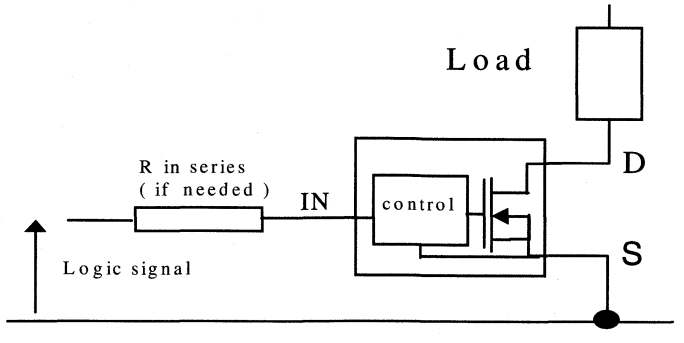


SUPER TO220



SUPER SMD220
Advance Information

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameter are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	37	V	
V_{in}	Maximum input voltage	-0.3	7		
I_{+in}	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(rth=60°C/W)	—	2.8		
	(rth=5°C/W)	—	35		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	100		
P_d	Maximum power dissipation(1)			W	
	(rth=60°C/W)	—	2		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance free air	—	60	—	°C/W	
R_{th} 2	Thermal resistance to PCB min footprint	—	60	—		
R_{th} 3	Thermal resistance to PCB 1" sq. footprint	—	35	—		
R_{th} 4	Thermal resistance junction to case	—	0.7	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	18	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} Tamb=85°C	Continuous drain current			A
	(TAmbient = 85°C, IN = 5V, rth = 80°C/W, Tj = 125°C)	—	8	
	(TAmbient = 85°C, IN = 5V, rth = 5°C/W, Tj = 125°C)	—	35	
R_{in}	Recommended resistor in series with IN pin	0.1	0.5	kΩ
$T_{r\text{-}in\ (max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	μS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. Notes.

Static Electrical Characteristics

Tj = 25°C unless otherwise specified. Standard footprint 70μm of copper thickness)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance Tj = 25°C	—	4.5	5.2	mΩ	V_{in} = 5V, I_{ds} = 10A
$R_{ds(on)}$ @Tj=150°C	ON state resistance Tj = 150°C	—	7.5	8.8		
Idss @Tj=25°C	Drain to source leakage current	0	0.01	25	μA	Vcc = 14V, Tj = 25oC
V clamp 1	Drain to source clamp voltage 1	37	40	—	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	—	43	48		I_d=$I_{shutdown}$ (see Fig.3 & 4)
V_{sd}	Body diode forward voltage	—	0.85	1		I_d = 35A, V_{in} = 0V
$V_{in\ clamp}$	IN to source clamp voltage	7	8.0	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.5	2		I_d = 50mA, Vds = 14V
$I_{in,\ on}$	Input supply current (normal operation)	25	90	300	μA	V_{in} = 5V
$I_{in,\ off}$	Input supply current (protection mode)	50	130	400		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 0.4Ω, Rinput = 50Ω, 100μs pulse, T_j = 25°C, (unless otherwise specified).

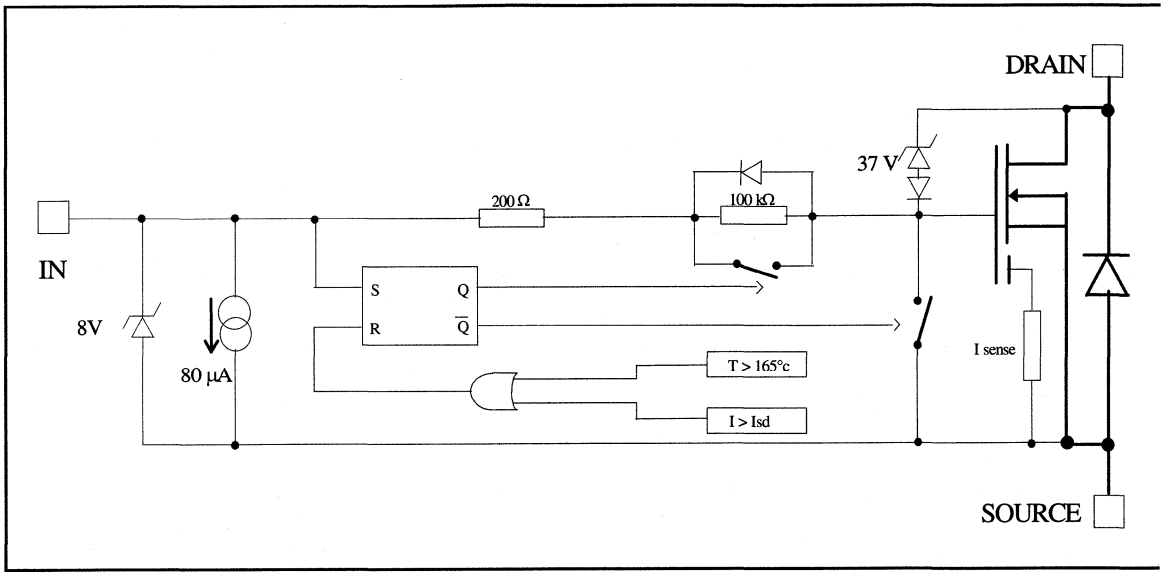
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.25	1	4	μs	See figure 2
T_r	Rise time	0.25	1	4		
T_{rf}	Time to 130% final $R_{ds(on)}$	—	15	—		
T_{off}	Turn-off delay time	1.5	4	8		See figure 2
T_f	Fall time	0.5	2	5		
Q_{in}	Total gate charge	—	200	—	nC	V_{in} = 5V

Protection Characteristics

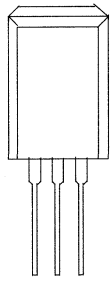
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	60	90	120	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	1.9	2.8	V	
T_{reset}	Time to reset protection	2	10	40	μs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (cf application note)	100	400	1200	μJ	V_{cc} = 14V

Functional Block Diagram

All values are typical



Lead Assignments



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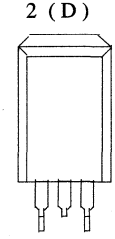

1 2 3
In D S

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(Advanced Information)

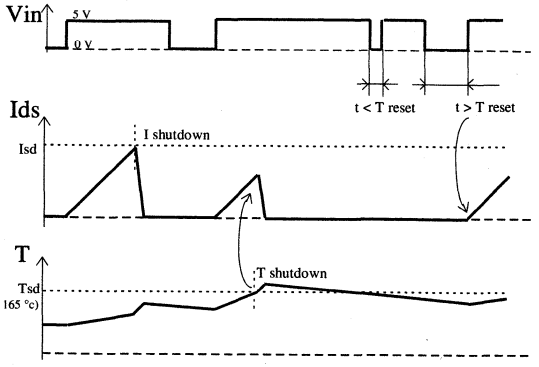


Figure 1 - Timing diagram

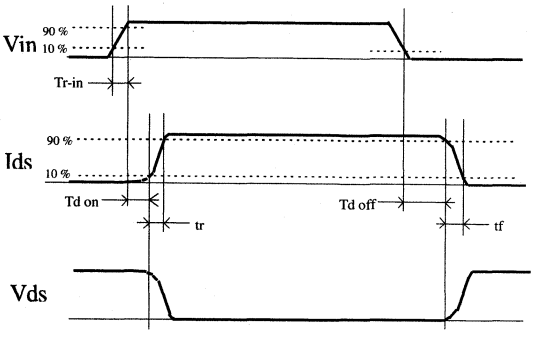


Figure 2 - IN rise time & switching time definitions

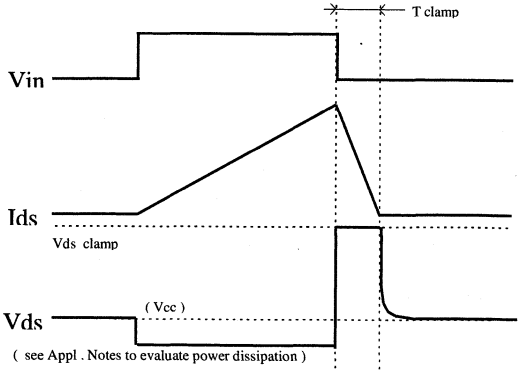


Figure 3 - Active clamp waveforms

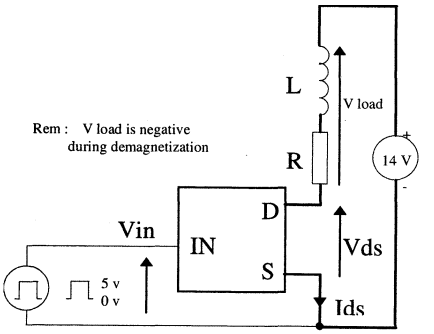


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprint. Operating in the shaded area is not recommended.

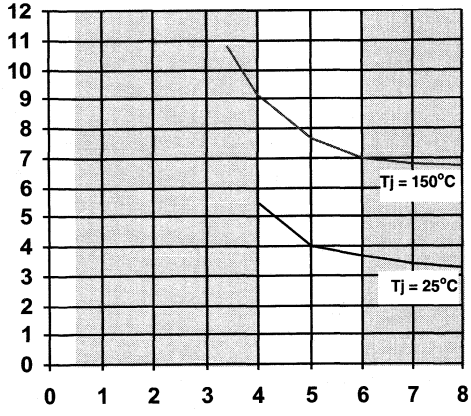


Figure 5 - $Rds_{(on)}$ (mΩ) Vs Input Voltage (V)

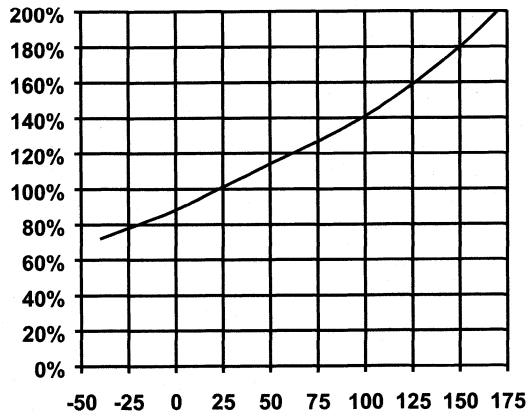


Figure 6 - Normalised $Rds_{(on)}$ (%) Vs T_j (°C)

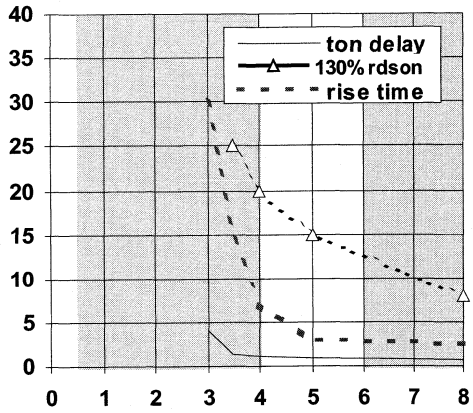


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs Input Voltage (V)

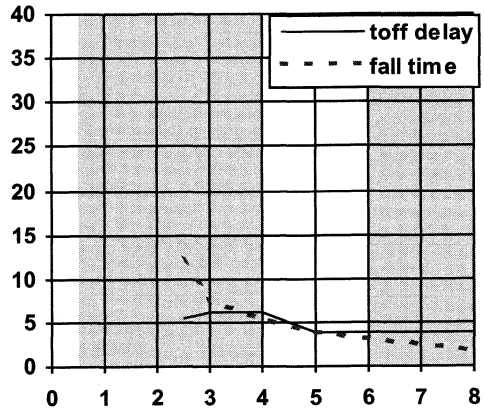


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

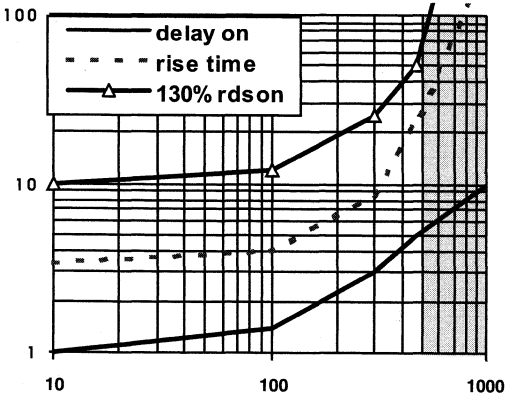


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs IN Resistor (Ω)

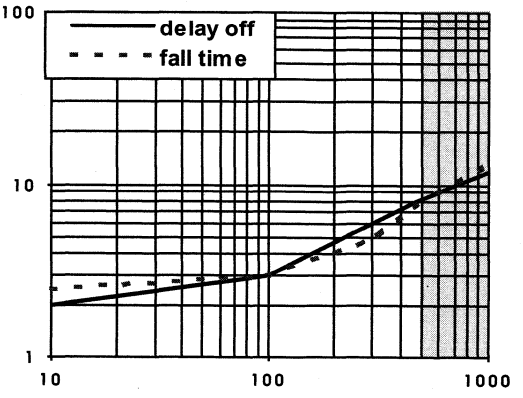


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

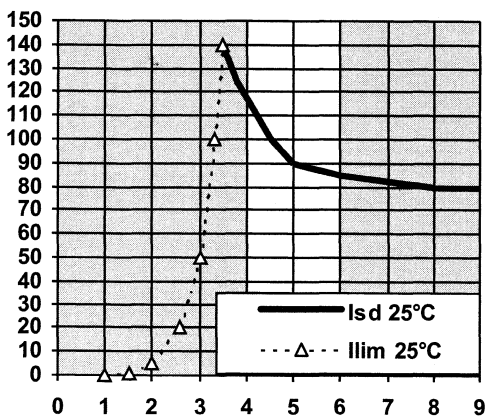


Figure 11 - Current Iim. & Ishutdown (A) Vs Vin (V)

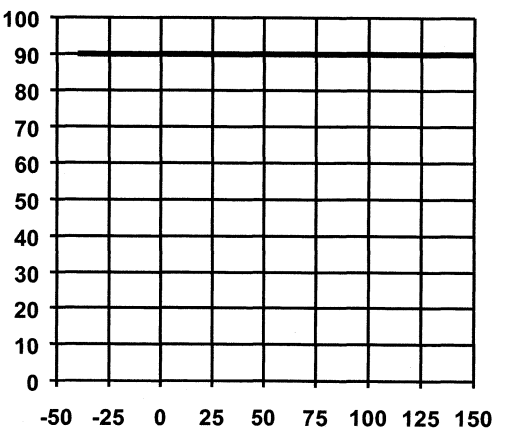


Figure 12 - Over-current (A) Vs Temperature (°C)

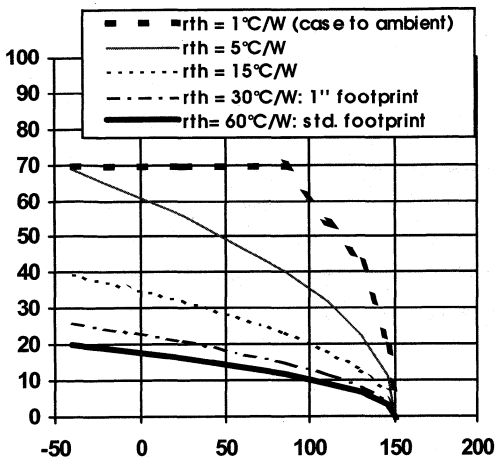


Figure 13 - Max.Cont. Ids (A) Vs Amb. Temperature (°C)

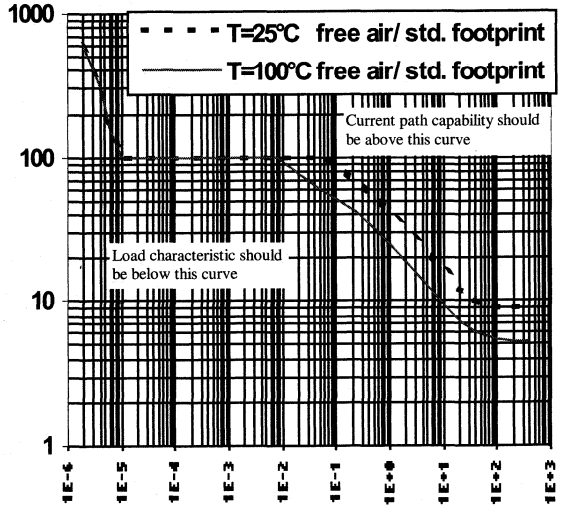


Figure 14 - Ids (A) Vs Protection Resp. Time (s)

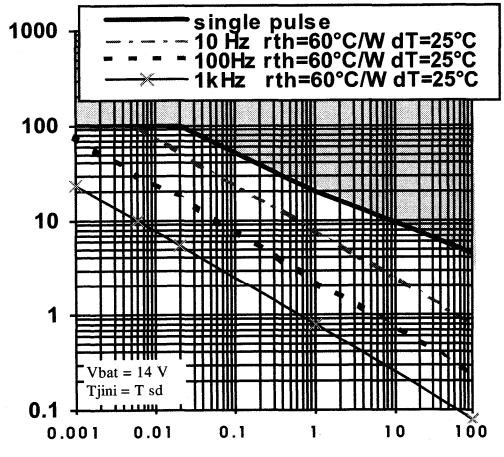


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

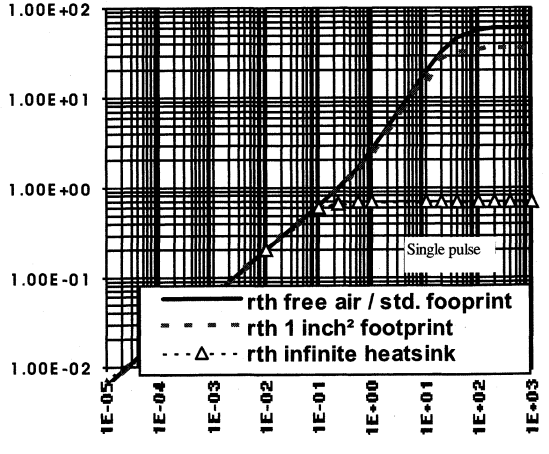


Figure 16 - Transient Thermal Imped. (°C/W) Vs Time (s)

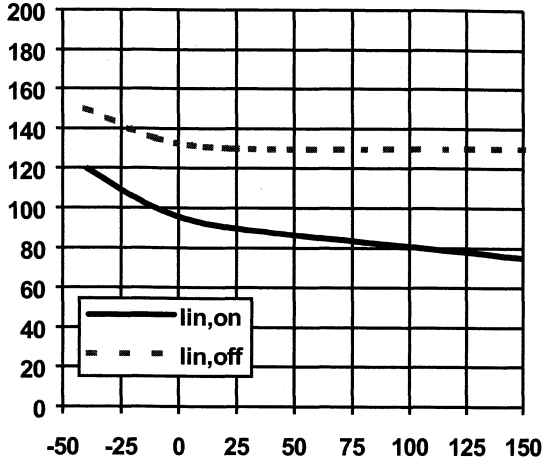


Figure 17 - Inputcurrent (μA) Vs Junction (°C)

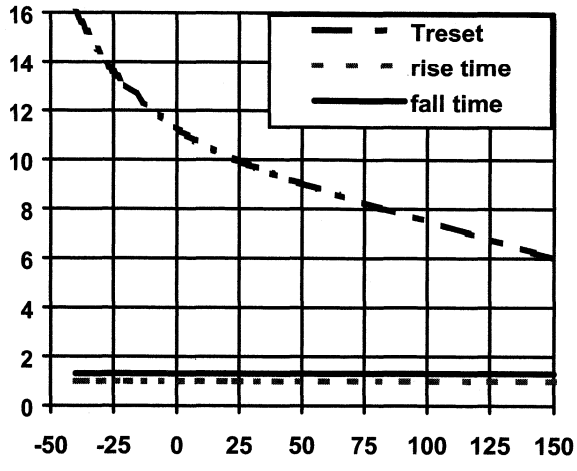


Figure 18 - Turn-on, Turn-off and Treset (μS) Vs Tj (°C)

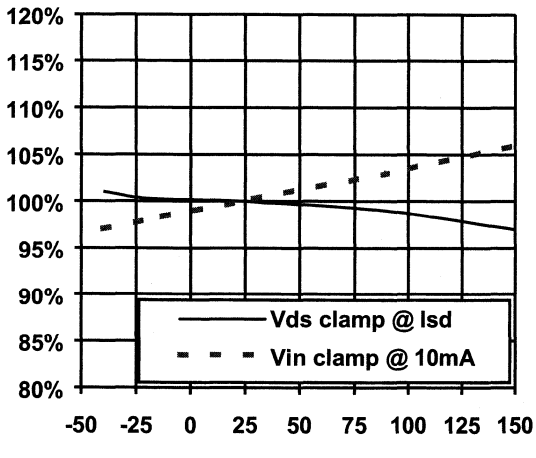
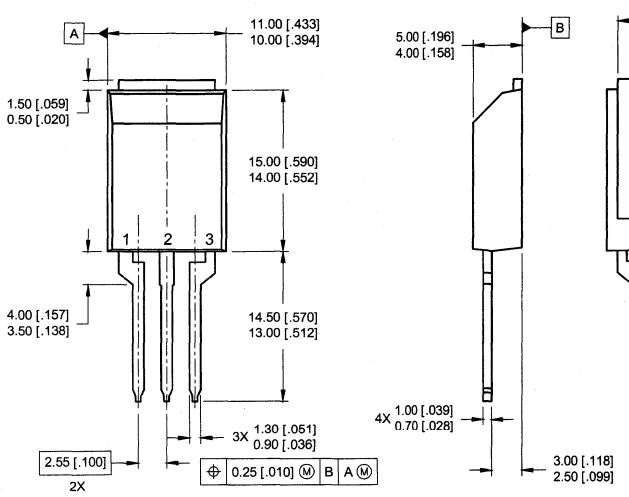


Figure 19 - Vin clamp1 & Vin clamp2 (%) Vs Tj (°C)

Case outline Super TO220



LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

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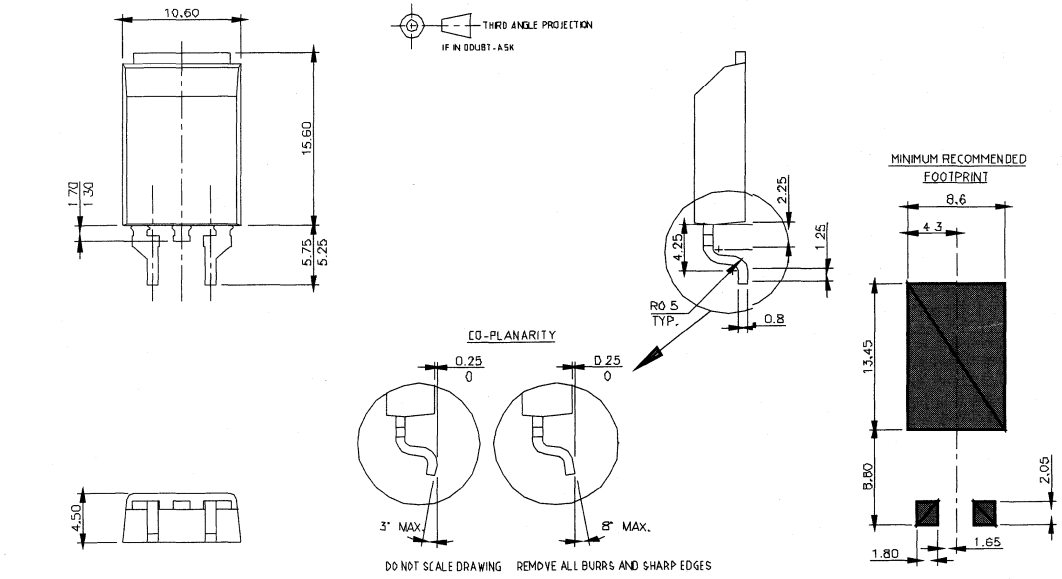
Case outline Super SMD220 (advance information)



IRGB-012-012 5

International
IOR Rectifier

Data Sheet No.PD 60155H

IPS511/IPS511S

FULLY PROTECTED HIGH SIDE POWER MOSFET SWITCH

Features

- Over temperature protection (with auto-restart)
- Short-circuit protection (current limit)
- Active clamp
- E.S.D protection
- Status feedback
- Open load detection
- Logic ground isolated from power ground

Product Summary

$R_{ds(on)}$	135mΩ (max)
V_{clamp}	50V
I_{Limit}	5A
$V_{open\ load}$	3V

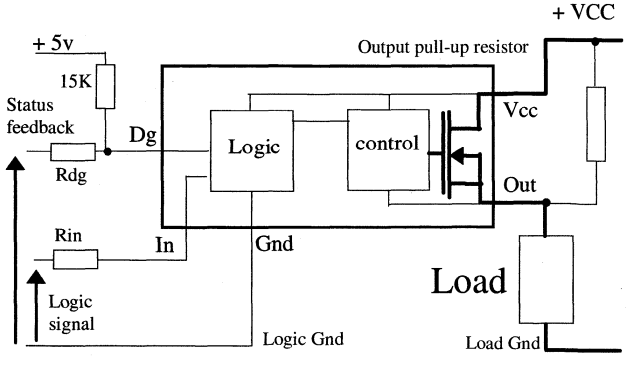
Description

The IPS511/IPS511S are fully protected five terminal high side switches with built in short circuit, over-temperature, ESD protection, inductive load capability and diagnostic feedback. The output current is controlled when it reaches I_{lim} value. The current limitation is activated until the thermal protection acts. The over-temperature protection turns off the high side switch if the junction temperature exceeds Tshutdown. It will automatically restart after the junction has cooled 7°C below Tshutdown. A diagnostic pin is provided for status feedback of short-circuit, over-temperature and open load detection. The double level shifter circuitry allows large offsets between the logic ground and the load ground.

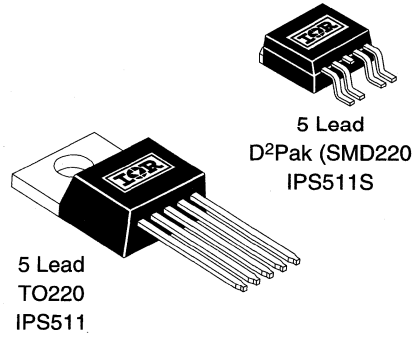
Truth Table

Op. Conditions	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Open load	H	H	H
Open load	L	H	H
Over current	H	L (limiting)	L
Over current	L	L	L
Over-temperature	H	L (cycling)	L
Over-temperature	L	L	L

Typical Connection



Packages



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to GROUND lead. (T_j = 25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{out}	Maximum output voltage	V_{CC}-50	V_{CC}+0.3	V	
V_{offset}	Maximum logic ground to load ground offset	V_{CC}-50	V_{CC}+0.3		
V_{in}	Maximum Input voltage	-0.3	5.5		
$V_{cc\ max}$	Maximum Vcc voltage	—	50		
$I_{in,\ max.}$	Maximum IN current	-5	10	mA	
V_{dg}	Maximum diagnostic output voltage	-0.3	5.5	V	
$I_{dg,\ max}$	Maximum diagnostic output current	-1	10	mA	
$I_{sd\ cont.}$	Diode max. permanent current (1)	—	2.2	A	
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
P_d	Maximum power dissipation(1)			W	
	(TC=25°C) IPS511	—	25		
	(rth=80°C/W) IPS511S	—	1.56		
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
T_{lead}	Lead temperature (soldering 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance junction to case	—	5	—	°C/W	TO-220
R_{th} 2	Thermal resistance junction to ambient	—	60	—		
R_{th} 1	Thermal resistance with standard footprint	—	60	—		D^2PAK (SMD220)
R_{th} 2	Thermal resistance with 1" square footprint	—	40	—		
R_{th} 3	Thermal resistance junction to case	—	5	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Continuous V_{CC} voltage	5.5	35	V
V_{IH}	High level input voltage	4	5.5	
V_{IL}	Low level input voltage	-0.3	0.9	
I_{out} Tamb=85°C	Continuous output current (TAmbient = 85°C, Tj = 125°C, R_{th} < 60°C/W) IPS511	—	1.7	A
	(TAmbient = 85°C, Tj = 125°C, R_{th} = 80°C/W) IPS511	—	1.5	
R_{in}	Recommended resistor in series with IN pin	4	6	kΩ
R_{dg}	Recommended resistor in series with DG pin	10	20	

Static Electrical Characteristics

(T_j = 25°C, V_{CC} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance T_j = 25°C	—	110	135	mΩ	V_{in} = 5V, I_{out} = 2.5A
$R_{ds(on)}$ (V_{CC}=6V)	ON state resistance @ V_{CC} = 6V	—	110	135		V_{in} = 5V, I_{out} = 1A
$R_{ds(on)}$ @Tj=150°C	ON state resistance Tj = 150°C	—	200	—		V_{in} = 5V, I_{out} = 2.5A
V_{CC} oper.	Operating voltage range	5.5	—	35	V	
V clamp 1	V_{CC} to OUT clamp voltage 1	50	56	—		I_d = 10mA (see Fig.1 & 2)
V clamp 2	V_{CC} to OUT clamp voltage 2	—	58	65		I_d = I_{sd} (see Fig.1 & 2)
V_f	Body diode forward voltage	—	0.9	1.2		I_d = 2.5A, V_{in} = 0V
I_{cc} off	Supply current when OFF	—	16	50	µA	V_{in} = 0V, V_{out} = 0V
I_{cc} on	Supply current when ON	—	0.7	2	mA	V_{in} = 5V
I_{cc} ac	Ripple current when ON (AC RMS)	—	20	—	µA	V_{in} = 5V
Vdgl	Low level diagnostic output voltage	—	0.15	0.4	V	I_{dg} = 1.6 mA
I_{oh}	Output leakage current	—	60	110	µA	V_{out} = 6V
I_{ol}	Output leakage current	0	—	25		V_{out} = 0V
Idg leakage	Diagnostic output leakage current	—	—	10		V_{dg} = 5.5V
V_{ih}	IN high threshold voltage	—	2.3	3	V	
V_{il}	IN low threshold voltage	1	1.95	—		
$I_{in,\ on}$	On state IN positive current	—	70	200	µA	V_{in} = 5V
In hyst.	Input hysteresis	0.1	0.25	0.5	V	

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 5.6Ω, T_j = 25°C, (unless otherwise specified).

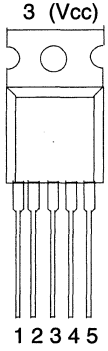
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{don}	Turn-on delay time	—	7	50	μs	See figure 3
T_{r1}	Rise time to V_{out} = V_{cc} - 5V	—	10	50		
T_{r2}	Rise time V_{cc} - 5V to V_{out} = 90% of V_{cc}	—	45	100		
dV/dt (on)	Turn ON dV/dt	—	1.3	4	V/μs	
E_{on}	Turn ON energy	—	400	—	μJ	
T_{doff}	Turn-off delay time	—	15	50	μs	See figure 4
T_f	Fall time to V_{out} = 10% of V_{cc}	—	10	50		
dV/dt (off)	Turn OFF dV/dt	—	2	6	V/μs	
E_{off}	Turn OFF energy	—	80	—	μJ	
T_{diag}	V_{out} to V_{diag} propagation delay	—	5	15	μs	See figure 6

Protection Characteristics

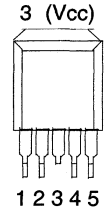
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	3	5	7	A	V_{out} = 0V
T_{sd+}	Over-temp. positive going threshold	—	165	—	°C	See fig. 2
T_{sd-}	Over-temp. negative going threshold	—	158	—	°C	See fig. 2
V_{sc}	Short-circuit detection voltage (3)	2	3	4	V	See fig. 2
$V_{open\ load}$	Open load detection threshold	2	3	4	V	

(3) Referenced to V_{cc}

Lead Assignments



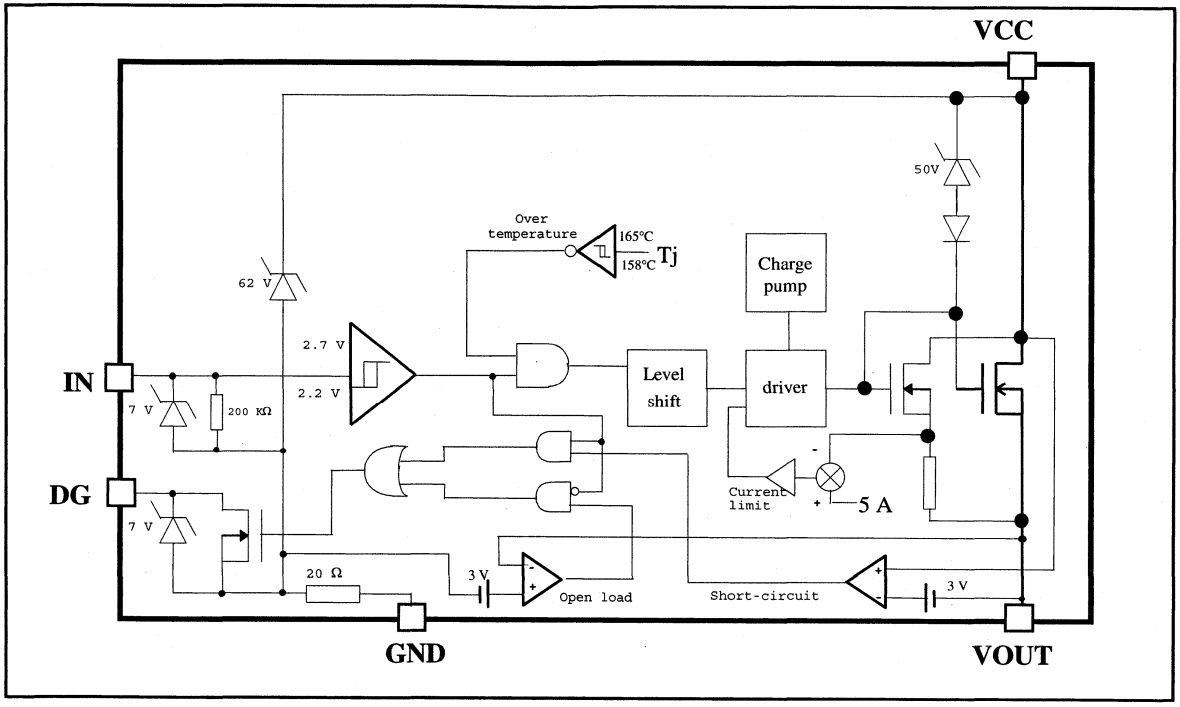
1 - Ground
2 - In
3 - Vcc
4 - DG
5 - Out



5 Lead - TO220	5 Lead - D^2PAK (SMD220)
IPS511	**IPS511S**
Part Number	

Functional Block Diagram

All values are typical



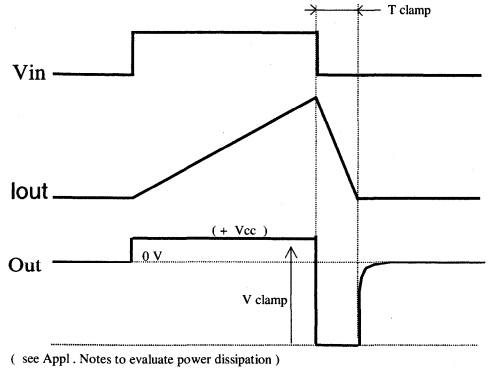


Figure 1 - Active clamp waveforms

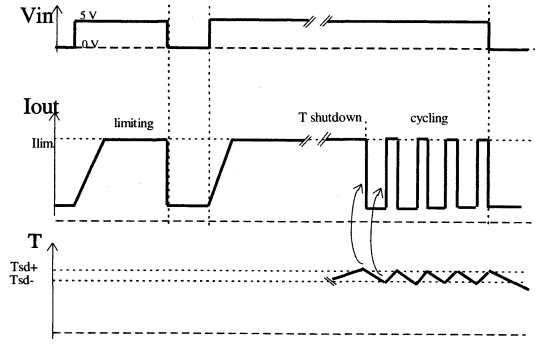


Figure 2 - Protection timing diagram

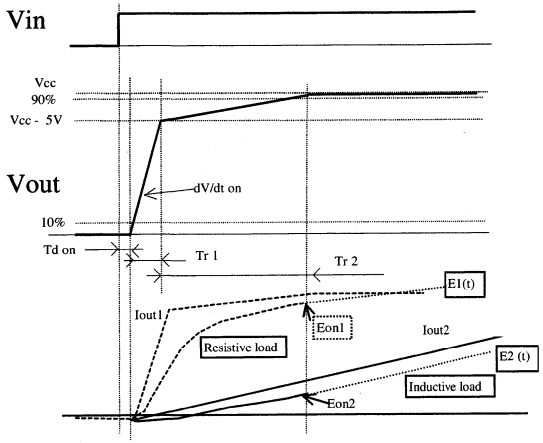


Figure 3 - Switching times definition (turn-on)
Turn on energy with a resistive or an inductive load

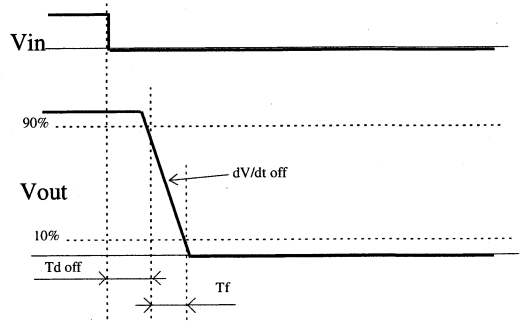


Figure 4 - Switching times definition (turn-off)

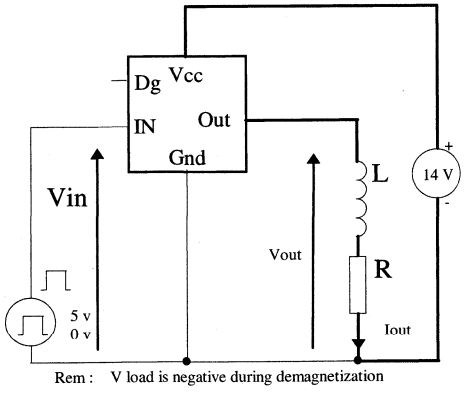


Figure 5 - Active clamp test circuit

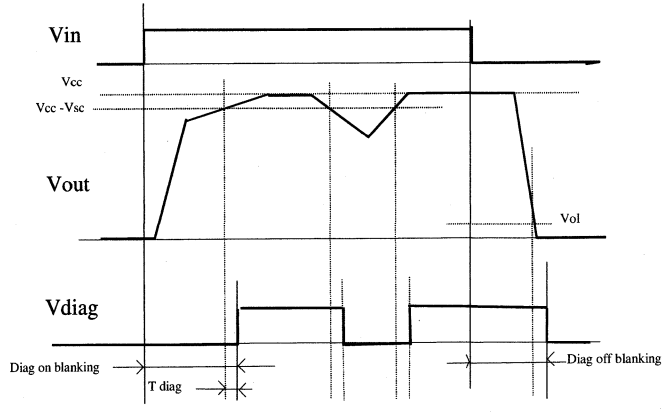


Figure 6 - Diagnostic delay definitions

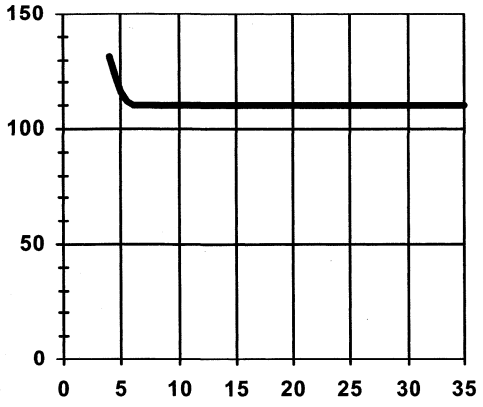


Figure 7 - $R_{ds(on)}$ (mΩ) Vs V_{cc} (V)

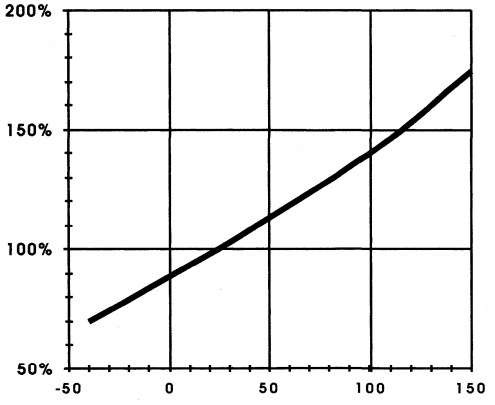


Figure 8 - Normalized $R_{ds(on)}$ (%) Vs T_j (°C)

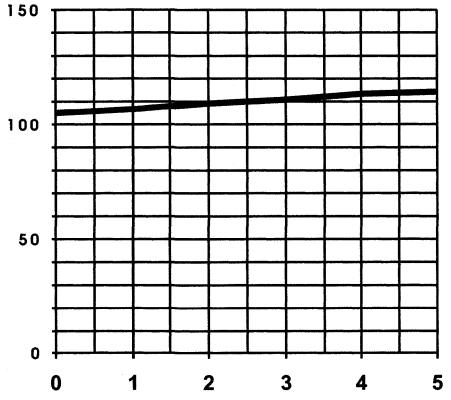


Figure 9 - Rds(on) (mΩ) Vs I_{out} (A)

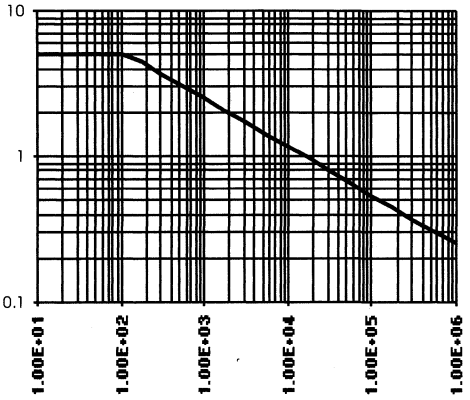


Figure 10 - Max. I_{out} (A) Vs Load Inductance (uH)

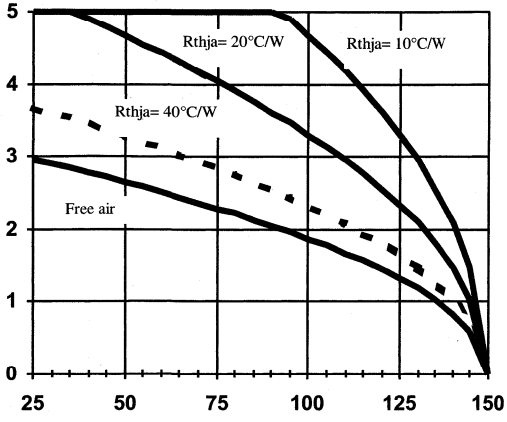


Figure 11a - Max load current (A) Vs Tamb (°C)
IPS511

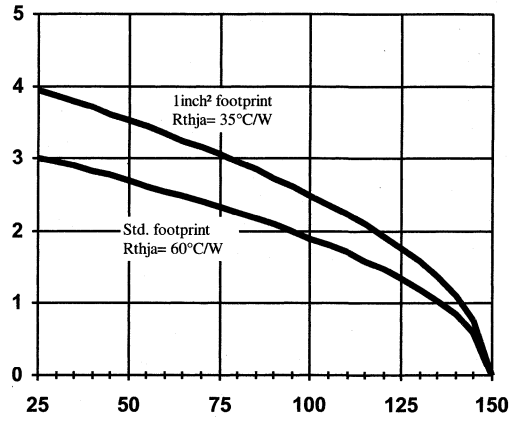


Figure 11b - Max load current (A) Vs Tamb (°C)
IPS511S

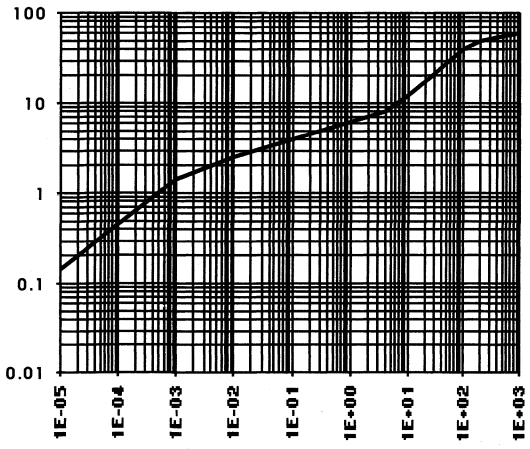


Figure 12 - Transient Thermal Impedance (°C/W)
Vs Time (S)

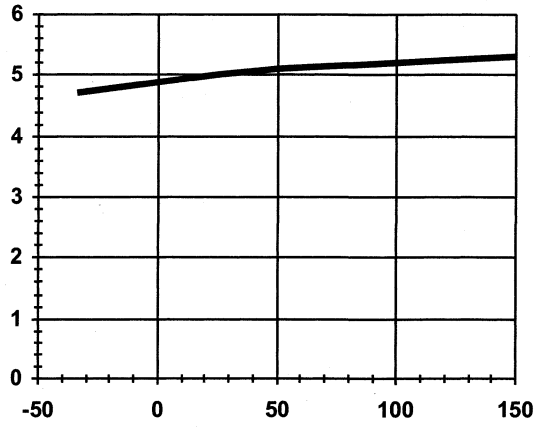


Figure 13 - I_{lim} (A) Vs T_j (°C)

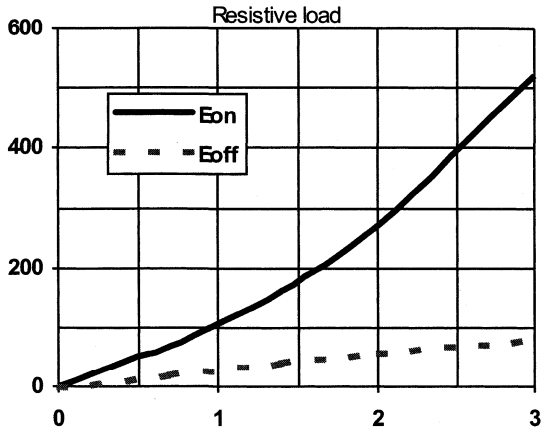


Figure 14 - E_{on}, E_{off} (μJ) (A) Vs I_{out} (A)

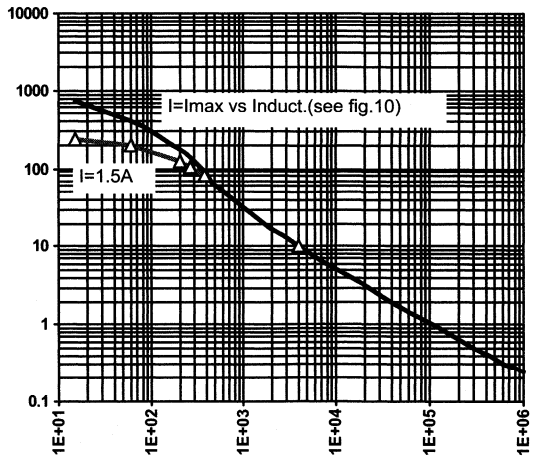


Figure 15 - E_{on} (μJ) Vs Load Inductance (μH)
(see Fig. 3)

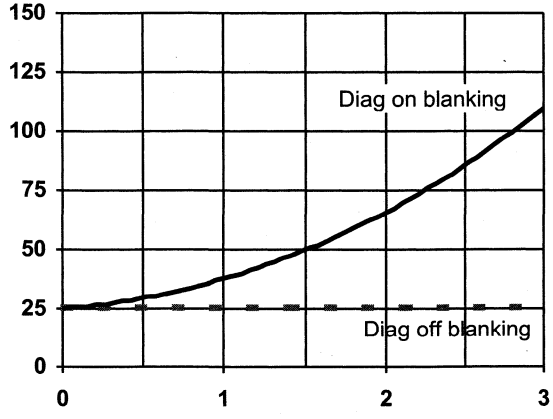


Figure 16 - Diag Blanking time (μS) Vs I_{out} (A)
(resistive load - see Fig. 6)

Figure 17 - I_{cc} (mA) Vs V_{cc} (V)

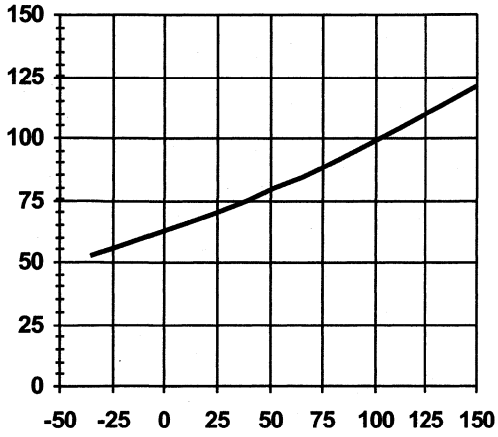
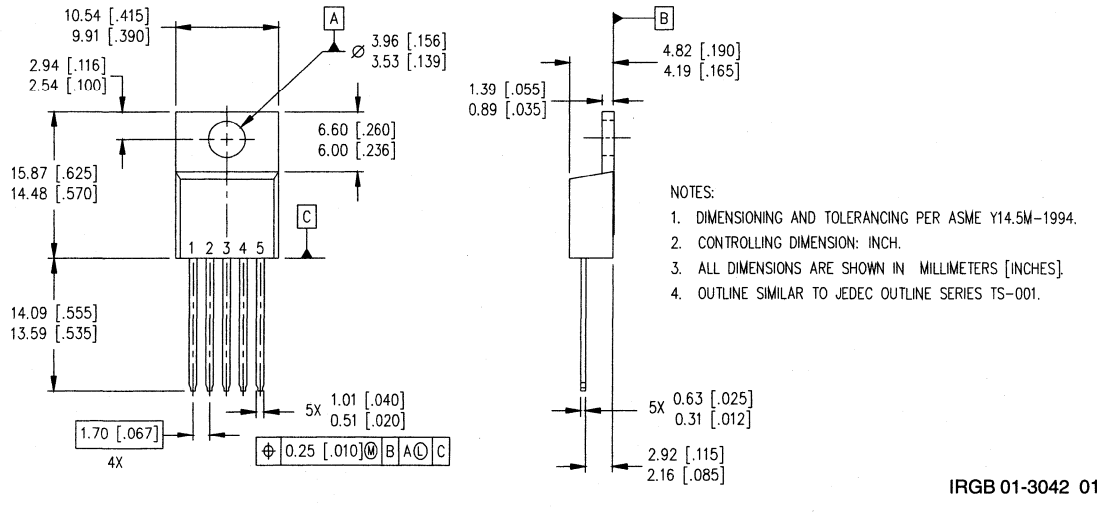
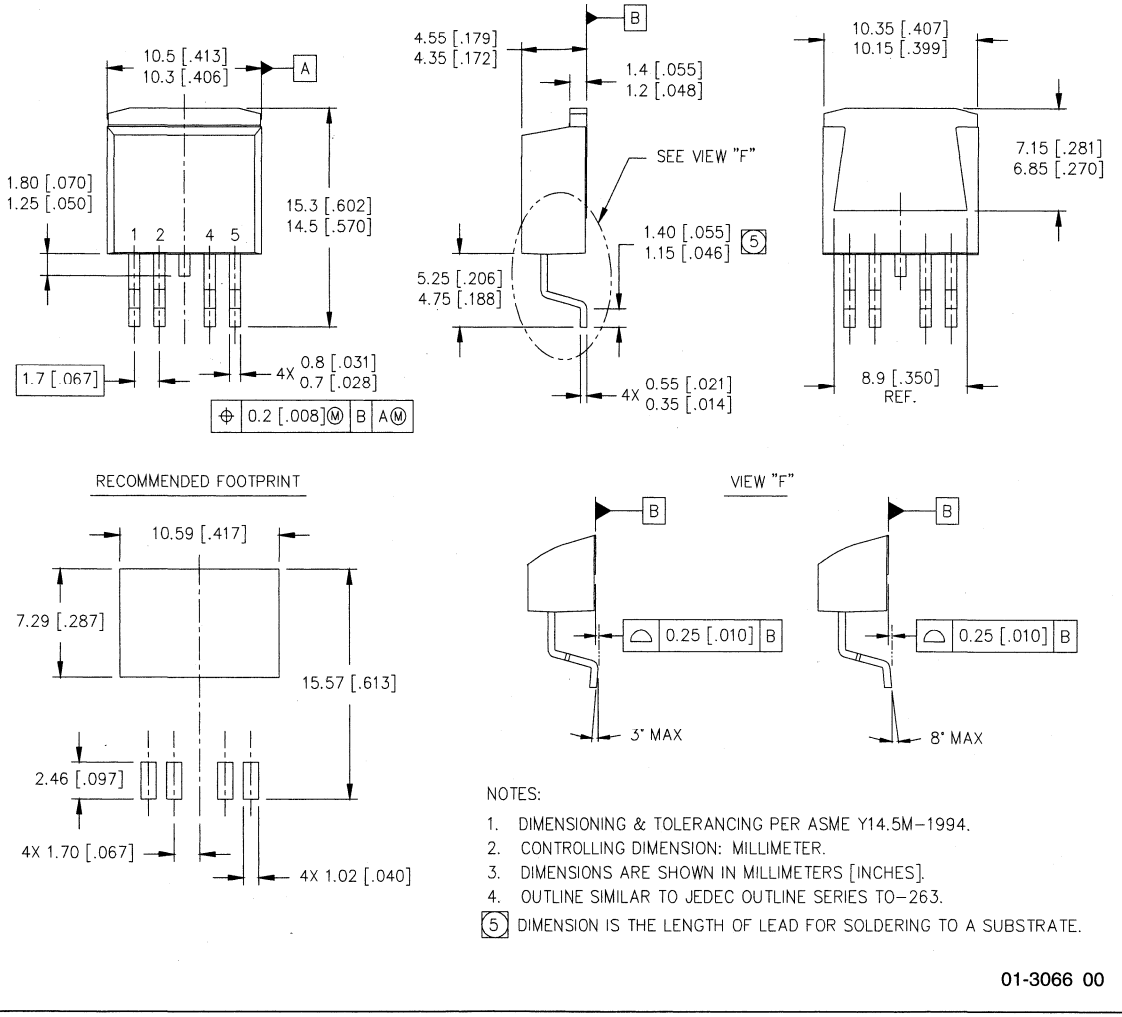


Figure 18 - I_{in} @ V_{in} = 5V (µA) Vs T_j (°C)

Case Outline 5 Lead - TO220



Case Outline 5 Lead - D²PAK (SMD220)



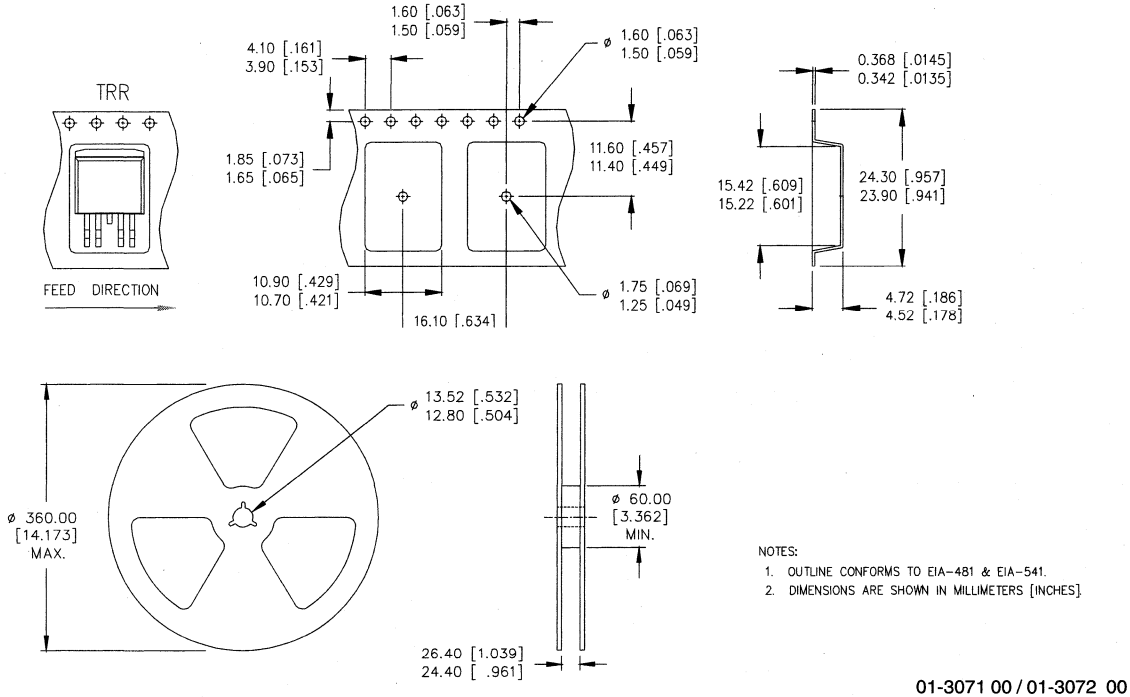
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO–263.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-3066 00

Tape & Reel 5 Lead - D²PAK (SMD220)



01-3071 00 / 01-3072 00

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

IPS511G/IPS512G

FULLY PROTECTED HIGH SIDE POWER MOSFET SWITCH

Features

- Over temperature protection (with auto-restart)
- Short-circuit protection (current limit)
- Active clamp
- E.S.D protection
- Status feedback
- Open load detection
- Logic ground isolated from power ground

Description

The IPS511G/IPS512G are fully protected five terminal high side switches with built in short-circuit, over-temperature, ESD protection, inductive load capability and diagnostic feedback. The output current is controlled when it reaches I_{lim} value. The current limitation is activated until the thermal protection acts. The over-temperature protection turns off the high side switch if the junction temperature exceeds Tshutdown. It will automatically restart after the junction has cooled 7°C below Tshutdown. A diagnostic pin is provided for status feedback of short-circuit, over-temperature and open load detection. The double level shifter circuitry allows large offsets between the logic ground and the load ground.

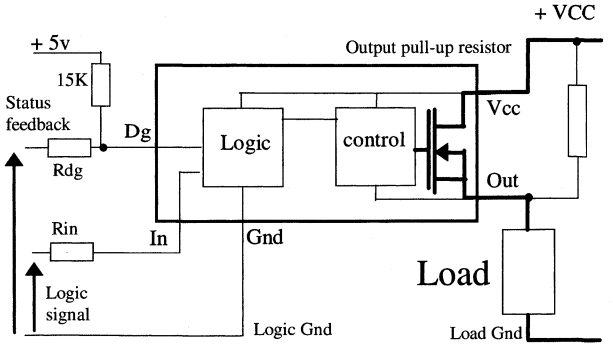
Product Summary

$R_{ds(on)}$	150mΩ (max)
V_{clamp}	50V
I_{Limit}	5A
$V_{open\ load}$	3V

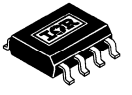
Truth Table

Op. Conditions	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Open load	H	H	H
Open load	L	H	H
Over current	H	L (limiting)	L
Over current	L	L	L
Over-temperature	H	L (cycling)	L
Over-temperature	L	L	L

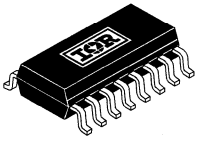
Typical Connection



Available Package



8 Lead SOIC
(Single)
IPS511G



16 Lead SOIC
(Dual)
IPS512G

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to GROUND lead. (T_j = 25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{out}	Maximum output voltage	V_{cc}-50	V_{cc}+0.3	V	
V_{offset}	Maximum logic ground to load ground offset	V_{cc}-50	V_{cc}+0.3		
V_{in}	Maximum Input voltage	-0.3	5.5		
$I_{in, max}$	Maximum IN current	-5	10	mA	
V_{dg}	Maximum diagnostic output voltage	-0.3	5.5	V	
$I_{dg, max}$	Maximum diagnostic output current	-1	10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(IPS511G)	—	1.4		
	(per leg/both legs ON - IPS512G)	—	0.8		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10		
ESD1	Electrostatic discharge voltage (Human Body)	—	4000	V	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	500		C=200pF, R=0Ω, L=10μH
P_d	Maximum power dissipation			W	
	(rth=125°C/W) IPS511G	—	1		
	(rth=85°C/W, both legs on) IPS512G	—	1.5		
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
Vvv max	Maximum Vcc voltage	—	50	V	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint	—	100	—	°C/W	8 Lead SOIC
R_{th2}	Thermal resistance with 1" square footprint	—	80	—		
R_{th1} (2 mos on)	Thermal resistance with standard footprint (2 mosfets on)	—	85	—		16 Lead SOIC
Rth2 (1) (1 mos on)	Thermal resistance with standard footprint (1 mosfet on)	—	100	—		
Rth2 (2 mos on)	Thermal resistance with 1" square footprint (2 mosfets on)	—	50	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{cc}	Continuous V_{cc} voltage	5.5	35	V
V_{IH}	High level input voltage	4	5.5	
V_{IL}	Low level input voltage	-0.3	0.9	
I_{out} Tamb=85°C	Continuous output current (TAmbient = 85°C, Tj = 125°C, rth = 100°C/W) IPS511G	—	1.4	A
I_{out} Tamb=85°C	Continuous output current per leg (TAmbient = 85°C, Tj = 125°C R_{th} = 85°C/W both legs on) IPS512G	—	1.0	
R_{in}	Recommended resistor in series with IN pin	4	6	kΩ
R_{dg}	Recommended resistor in series with DG pin	10	20	

Static Electrical Characteristics

(T_j = 25°C, V_{cc} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance T_j = 25°C	—	130	150	mΩ	V_{in} = 5V, I_{out} = 2.5A
$R_{ds(on)}$ (V_{cc}=6V)	ON state resistance @ V_{cc} = 6V	—	130	150		V_{in} = 5V, I_{out} = 1A
$R_{ds(on)}$ @Tj=150°C	ON state resistance Tj = 150°C	—	220	—		V_{in} = 5V, I_{out} = 2.5A
V_{cc} oper.	Operating voltage range	5.5	—	35	V	
V clamp 1	V_{cc} to OUT clamp voltage 1	50	56	—		I_d = 10mA (see Fig.1 & 2)
V clamp 2	V_{cc} to OUT clamp voltage 2	—	58	65		I_d = I_{sd} (see Fig.1 & 2)
V_f	Body diode forward voltage	—	0.9	1.2		I_d = 2.5A, V_{in} = 0V
$I_{cc\ off}$	Supply current when OFF	—	16	50	µA	V_{in} = 0V, V_{out} = 0V
$I_{cc\ on}$	Supply current when ON	—	0.7	2	mA	V_{in} = 5V
$I_{cc\ ac}$	Ripple current when ON (AC RMS)	—	20	—	µA	V_{in} = 5V
V_{dgl}	Low level diagnostic output voltage	—	0.15	0.4	V	I_{dg} = 1.6 mA
I_{ol}	Output leakage current	—	60	120	µA	V_{out} = 6V
I_{ol}	Output leakage current	0	—	25		V_{out} = 0V
$I_{dg\ leakage}$	Diagnostic output leakage current	—	—	10		V_{dg} = 5.5V
V_{ih}	IN high threshold voltage	—	2.3	2.5	V	
V_{il}	IN low threshold voltage	1	2	—		
$I_{in,\ on}$	On state IN positive current	—	70	200	µA	V_{in} = 5V
In, hyst.	Input hysteresis	0.1	0.25	0.5	V	

Switching Electrical Characteristics

V_{CC} = 14V, Resistive Load = 5.6Ω, T_j = 25°C, (unless otherwise specified).

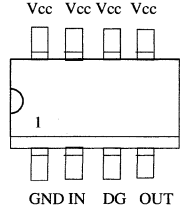
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{don}	Turn-on delay time	—	7	50	µs	See figure 3
T_{r1}	Rise time to V_{out} = V_{CC} - 5V	—	10	50		
T_{r2}	Rise time from the end of TR1 to V_{out} = 90% of V_{CC}	—	45	95		
dV/dt (on)	Turn ON dV/dt	—	1.3	4	V/µs	
E_{on}	Turn ON energy	—	400	—	µs	See figure 4
T_{doff}	Turn-off delay time	—	15	50		
T_f	Fall time to V_{out} = 10% of V_{CC}	—	10	50		
dV/dt (off)	Turn OFF dV/dt	—	2	6	V/µs	
E_{off}	Turn OFF energy	—	80	—	µJ	
T_{diag}	Vout to Vdiag propagation delay	—	5	15	µs	

Protection Characteristics

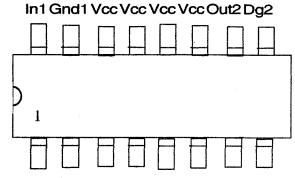
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	3	5	7	A	V_{out} = 0V
T_{sd+}	Over-temp. positive going threshold	—	165	—	°C	See fig. 2
T_{sd-}	Over-temp. negative going threshold	—	158	—	°C	See fig. 2
V_{sc}	Short-circuit detection voltage (3)	2	3	4	V	See fig. 2
$V_{open\ load}$	Open load detection threshold	2	3	4	V	

(3) Referenced to V_{CC}

Lead Assignments



8 Lead SOIC



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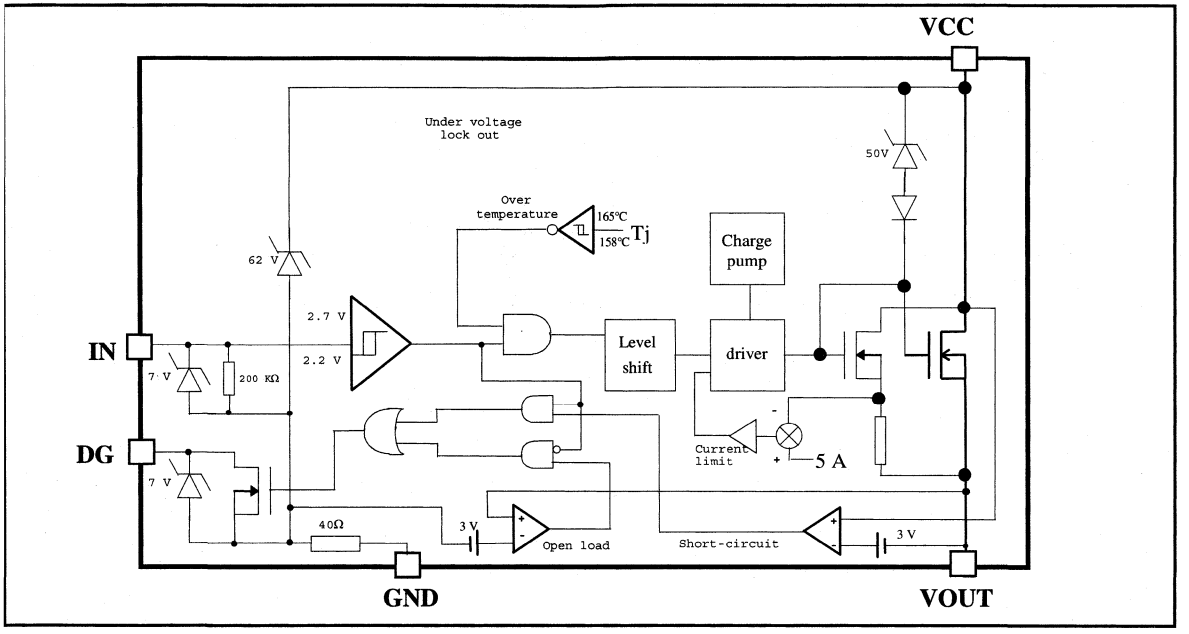
IPS511G	IPS512G
Part Number	

Functional Block Diagram

All values are typical



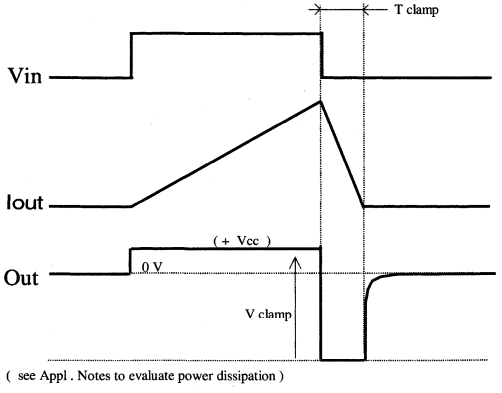


Figure 1 - Active clamp waveforms

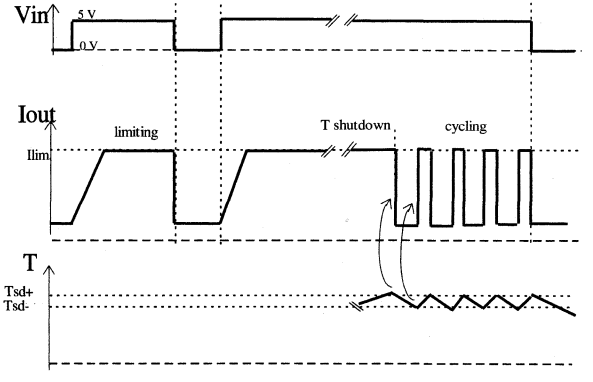


Figure 2 - Protection timing diagram

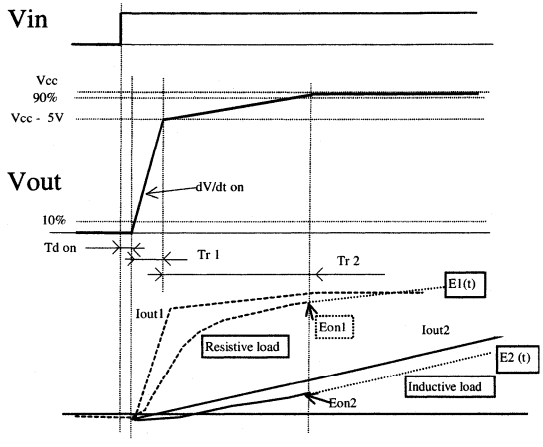


Figure 3 - Switching times definition (turn-on)
Turn on energy with a resistive or an inductive load

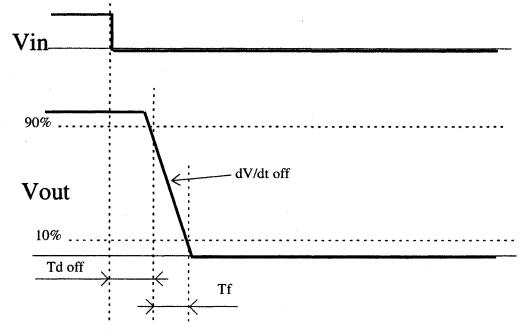


Figure 4 - Switching times definition (turn-off)

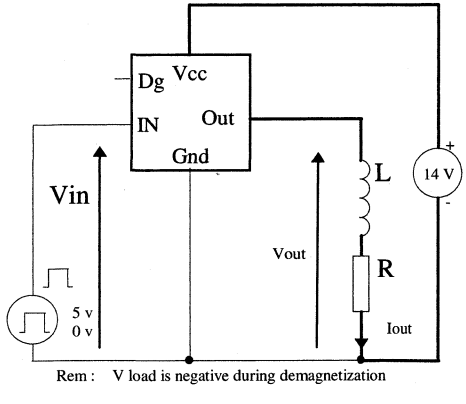


Figure 5 - Active clamp test circuit

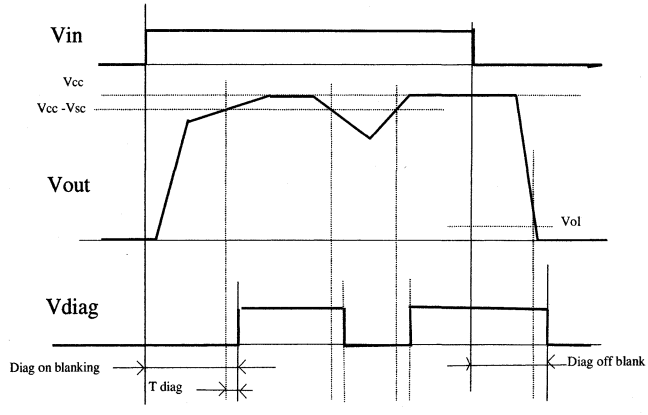


Figure 6 - Diagnostic delay definitions

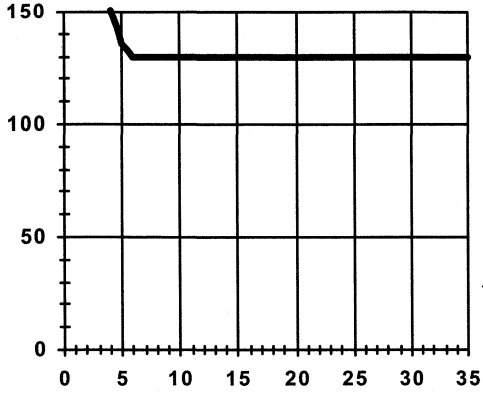


Figure 7 - $R_{ds(on)}$ (mΩ) Vs V_{cc} (V)

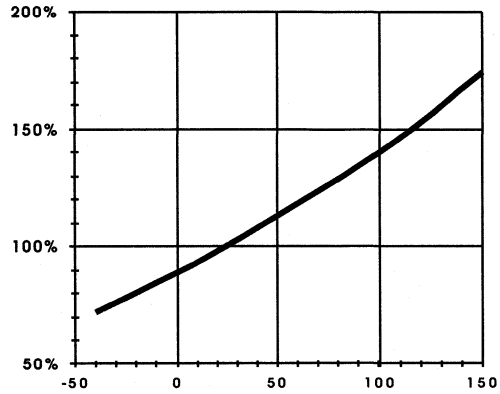


Figure 8 - Normalized $R_{ds(on)}$ Vs T_j (°C)

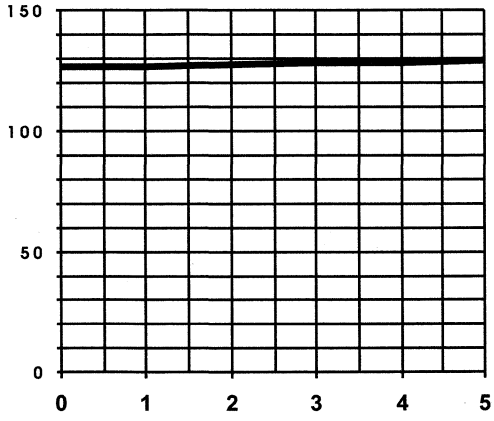


Figure 9 - Rds(on) (mΩ) Vs I_{out} (A)

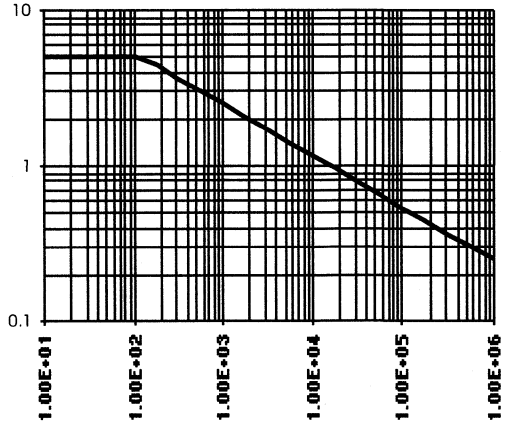


Figure 10 - Max. I_{out} (A) Vs Load Inductance (uH)

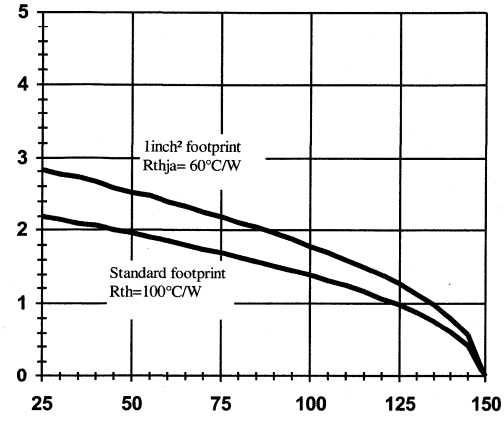


Figure 11a - Max load current (A) Vs Tamb (°C)
IPS511G

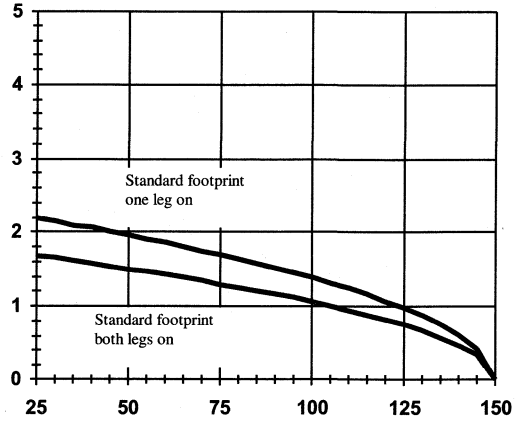


Figure 11b - Max load current (A) Vs Tamb (°C)
IPS512G

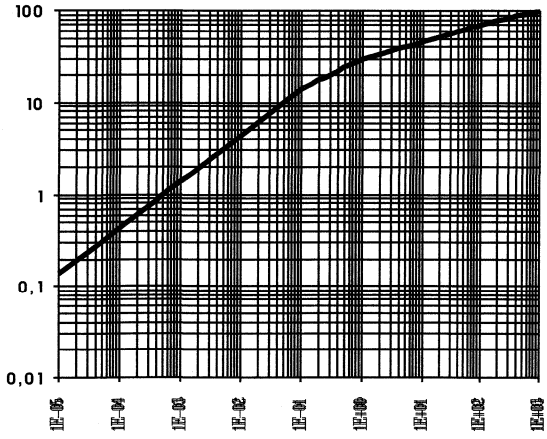


Figure 12 - Transient Thermal Impedance (°C/W)
Vs Time (S) - IPS511G/IPS512G

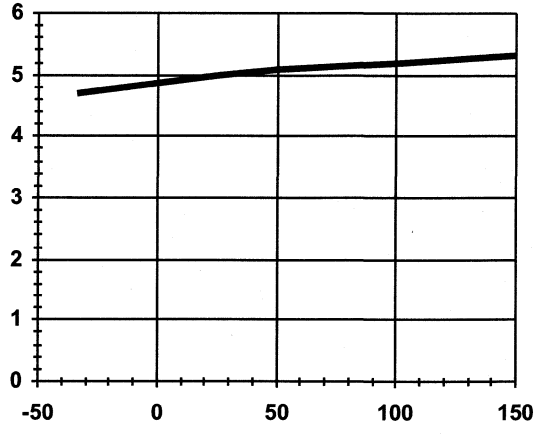


Figure 13 - I_{lim} (A) Vs T_j (°C)

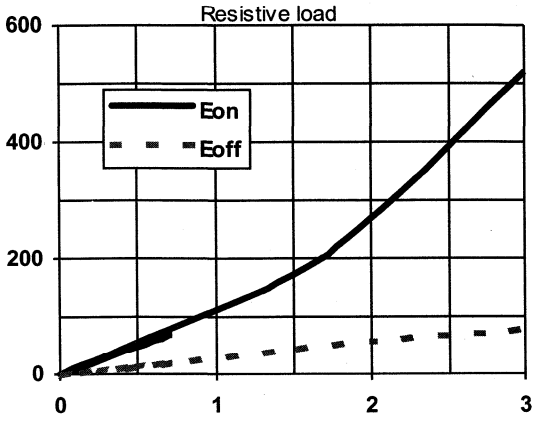


Figure 14 - Eon, Eoff (μJ) vs I (A)

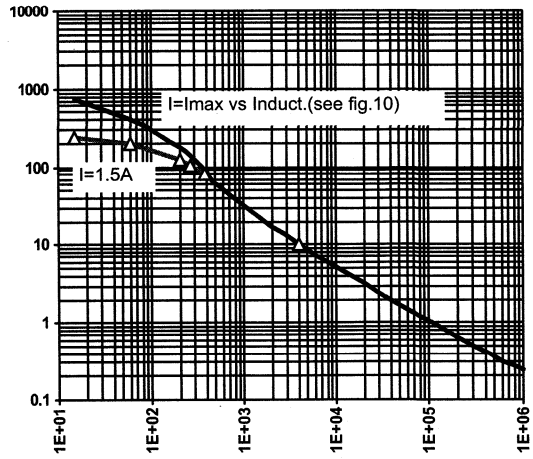


Figure 15 - E_{on} (μJ) Vs Load Inductance (μH)
(see Fig. 3)

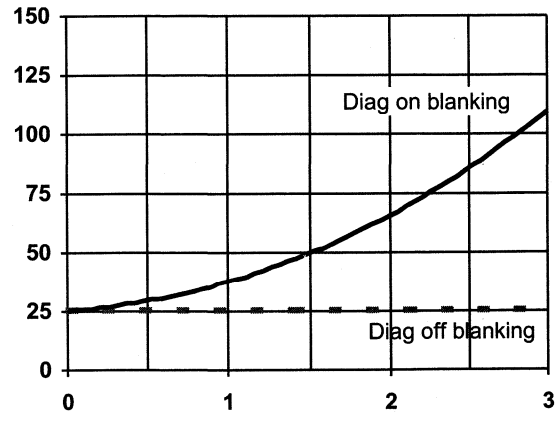


Figure 16 - Diag Blanking time (μS) Vs I_{out} (A)
(resistive load - see Fig. 6)

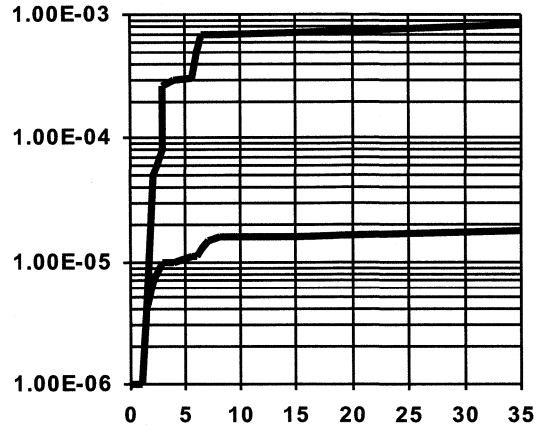
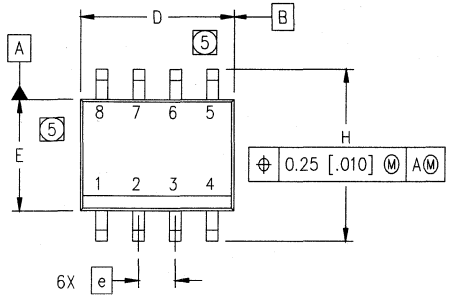
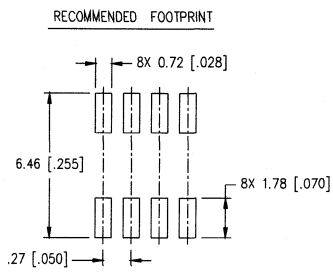


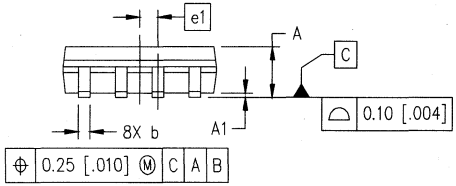
Figure 17 - I_{CC} (mA) Vs V_{CC} (V)

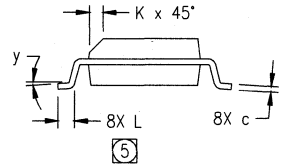
Case Outline - IPS511G





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°





NOTES:

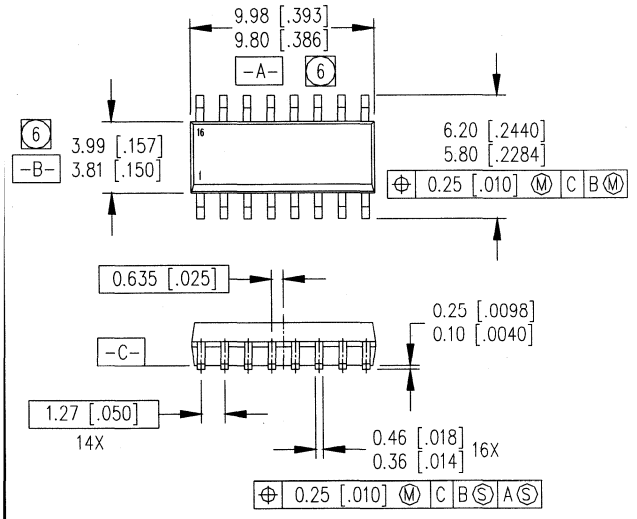
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

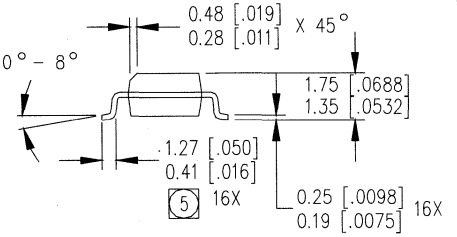
8 Lead SOIC

(MS-012AA) 01-0021 09

Case Outline



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



16 Lead SOIC (narrow body) 01-3064 00

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

nternational
IOR Rectifier

IPS521/IPS521S

FULLY PROTECTED HIGH SIDE POWER MOSFET SWITCH

Features

- Over temperature protection (with auto-restart)
- Short-circuit protection (current limit)
- Active clamp
- E.S.D protection
- Status feedback
- Open load detection
- Logic ground isolated from power ground

Product Summary

$R_{ds(on)}$	80mΩ (max)
V_{clamp}	50V
I_{Limit}	10A
$V_{open\ load}$	3V

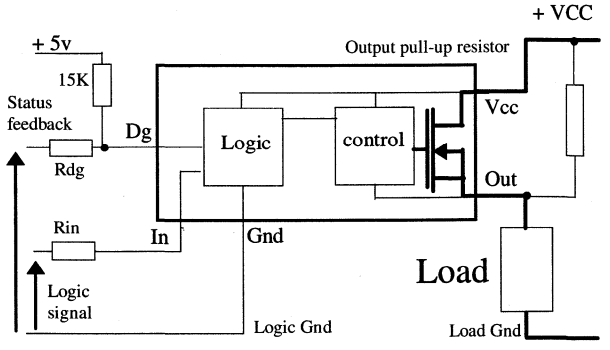
Description

The IPS521/IPS521S are fully protected five terminal high side switches with built in short-circuit , over-temperature, ESD protection, inductive load capability and diagnostic feedback. The output current is controlled when it reaches I_{lim} value. The current limitation is activated until the thermal protection acts. The over-temperature protection turns off the high side switch if the junction temperature exceeds Tshutdown. It will automatically restart after the junction has cooled 7°C below Tshutdown. A diagnostic pin is provided for status feedback of short-circuit, over-temperature and open load detection. The double level shifter circuitry allows large offsets between the logic ground and the load ground.

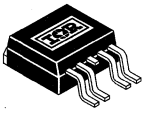
Truth Table

Op. Conditions	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Open load	H	H	H
Open load	L	H	H
Over current	H	L (limiting)	L
Over current	L	L	L
Over-temperature	H	L (cycling)	L
Over-temperature	L	L	L

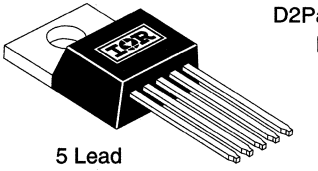
Typical Connection



Packages



5 Lead
D2Pak (SMD220)
IPS521S



5 Lead
TO220 - IPS521

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to GROUND lead. (T_j = 25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{out}	Maximum output voltage	V_{CC}-50	V_{CC}+0.3	V	
V_{offset}	Maximum logic ground to load ground offset	V_{CC}-50	V_{CC}+0.3		
V_{in}	Maximum Input voltage	-0.3	7		
$I_{in, max}$	Maximum positive IN current	-5	10	mA	
V_{dg}	Maximum diagnostic output voltage	-0.3	7	V	
$I_{dg, max}$	Maximum diagnostic output current	-1	10	mA	
$I_{sd\ cont.}$	Diode max. permanent current (1) (rth=62°C/W)	—	2.2	A	
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
P_d	Maximum power dissipation(1) (TC=25°C) IPS521	—	40	W	
	(TC=25°C) IPS521S	—	1.56		
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
T_{lead}	Lead temperature (soldering 10 seconds)	—	300		
Vcc max.	Maximum Vcc voltage	—	50	V	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance junction to case	—	3	—	°C/W	TO-220
R_{th} 2	Thermal resistance junction ambient	—	60	—		
R_{th} 1	Thermal resistance with standard footprint	—	60	—		D^2PAK (SMD220)
R_{th} 2	Thermal resistance with 1" square footprint	—	35	—		
R_{th} 3	Thermal resistance junction to case	—	3	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Continuous V_{CC} voltage	5.5	35	V
V_{IH}	High level input voltage	4	5.5	
V_{IL}	Low level input voltage	-0.3	0.9	
I_{out}	Continuous output current (Tamb = 85°C, Tj = 125°C, R_{th} = 60°C/W,) IPS521	—	2.2	A
I_{out}	Continuous output current (Tamb = 85°C, Tj = 125°C, R_{th} = 80°C/W,) IPS521S	—	1.9	
R_{in}	Recommended resistor in series with IN pin	4	6	kΩ
R_{dg}	Recommended resistor in series with DG pin	10	20	

Static Electrical Characteristics

(T_j = 25°C, V_{CC} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance T_j = 25°C	—	55	80	mΩ	V_{in} = 5V, I_{out} = 5A
$R_{ds(on)}$ (V_{CC}=6V)	ON state resistance @ V_{CC} = 6V	—	55	80		V_{in} = 5V, I_{out} = 2.5A
$R_{ds(on)}$ @Tj=150°C	ON state resistance Tj = 150°C	—	110	140		V_{in} = 5V, I_{out} = 5A
V_{CC} oper.	Operating voltage range	5.5	—	35	V	
V clamp 1	V_{CC} to OUT clamp voltage 1	50	55	—		I_d = 10mA (see Fig.1 & 2)
V clamp 2	V_{CC} to OUT clamp voltage 2	—	56	65		I_d = I_{sd} (see Fig.1 & 2)
V_f	Body diode forward voltage	—	0.9	1.2		I_d = 2.5A, V_{in} = 0V
$I_{cc\ off}$	Supply current when OFF	—	16	50	µA	V_{in} = 0V, V_{out} = 0V
$I_{cc\ on}$	Supply current when ON	—	0.6	2	mA	V_{in} = 5V
$I_{cc\ ac}$	Ripple current when ON (AC RMS)	—	20	—	µA	V_{in} = 5V
V_{dgl}	Low level diagnostic output voltage	—	0.15	0.4	V	I_{dg} = 1.6 mA
I_{oh}	Output leakage current	—	50	120	µA	V_{out} = 6V
I_{ol}	Output leakage current	0	—	25		V_{out} = 0V
$I_{dg\ leakage}$	Diagnostic output leakage current	—	—	10		V_{dg} = 5.5V
V_{ih}	IN high threshold voltage	—	2.2	3	V	
V_{il}	IN low threshold voltage	1	1.9	—		
$I_{in,\ on}$	On state IN positive current	—	70	200	µA	V_{in} = 5V
In hyst	Input hysteresis	0.1	0.25	0.5	V	

Switching Electrical Characteristics

V_{CC} = 14V, Resistive Load = 2.8Ω, T_j = 25°C, (unless otherwise specified).

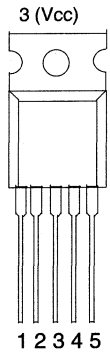
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{don}	Turn-on delay time	—	10	40	µs	See figure 3
T_{r1}	Rise time to V_{out} = V_{CC} - 5V	—	25	60		
T_{r2}	Rise time V_{CC} - 5V to V_{out} = 90% of V_{CC}	—	130	200		
dV/dt (on)	Turn ON dV/dt	—	0.7	2	V/µs	
E_{on}	Turn ON energy	—	1500	—	µJ	
T_{doff}	Turn-off delay time	—	35	70	µs	See figure 4
T_f	Fall time to V_{out} = 10% of V_{CC}	—	25	50		
dV/dt (off)	Turn OFF dV/dt	—	0.9	3	V/µs	
E_{off}	Turn OFF energy	—	250	—	µJ	
T_{diag}	V_{out} to V_{diag} propagation delay	—	5	15	µs	See figure 6

Protection Characteristics

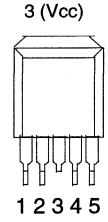
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	7	10	14	A	V_{out} = 0V
T_{sd+}	Over-temp. positive going threshold	—	165	—	°C	See fig. 2
T_{sd-}	Over-temp. negative going threshold	—	158	—		See fig. 2
V_{sc}	Short-circuit detection voltage (3)	2	3	4	V	See fig. 2
$V_{open\ load}$	Open load detection threshold	2	3	4		

(3) Referenced to V_{CC}

Lead Assignments



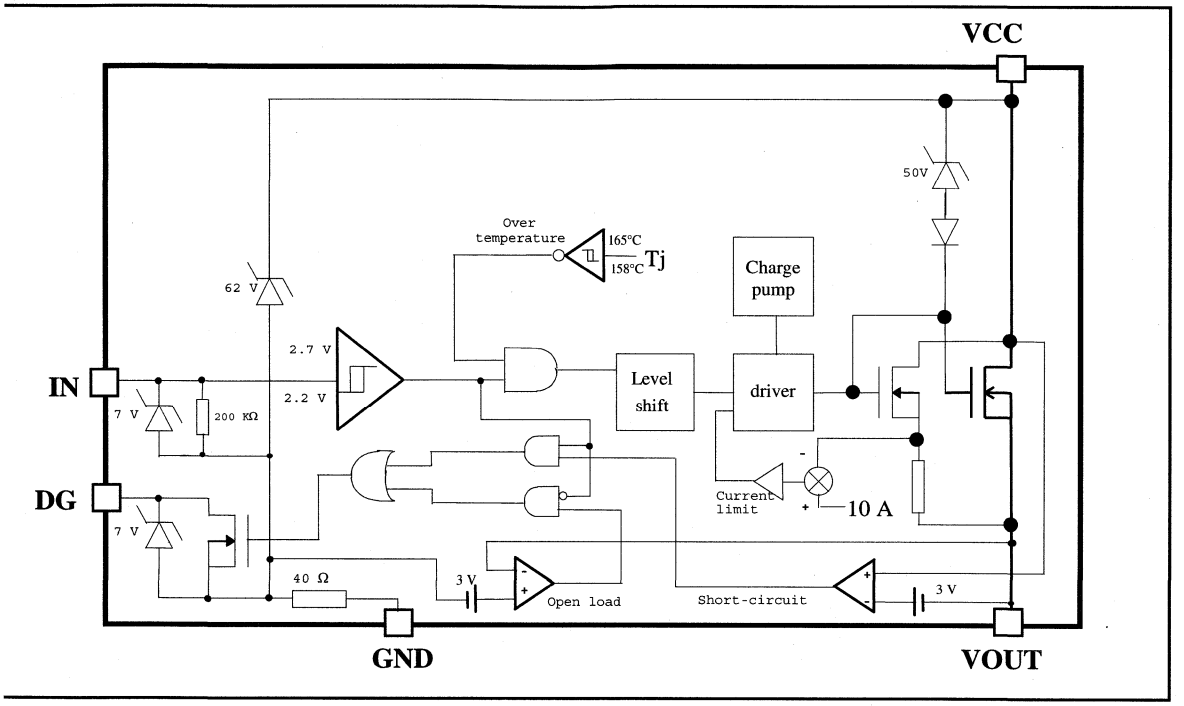
1 - Ground
2 - In
3 - Vcc
4 - DG
5 - Out



5 Lead - TO220	5 Lead - D²PAK (SMD220)
IPS521	**IPS521S**
Part Number	

Functional Block Diagram

All values are typical



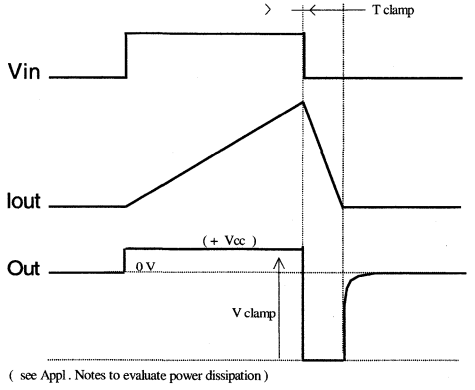


Figure 1 - Active clamp waveforms

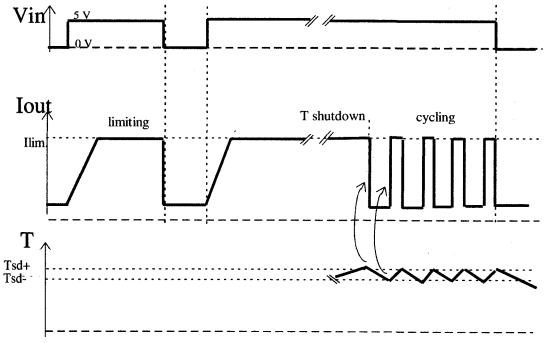


Figure 2 - Protection timing diagram

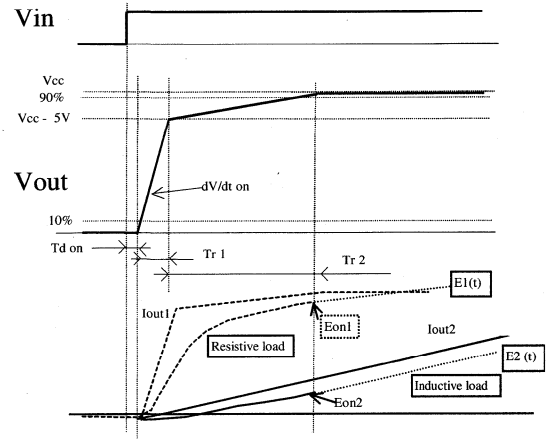


Figure 3 - Switching times definition (turn-on)
Turn on energy with a resistive or an inductive load

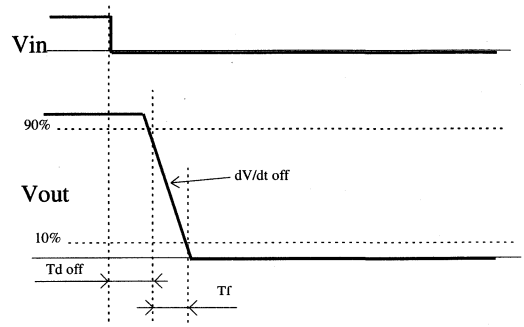


Figure 4 - Switching times definition (turn-off)

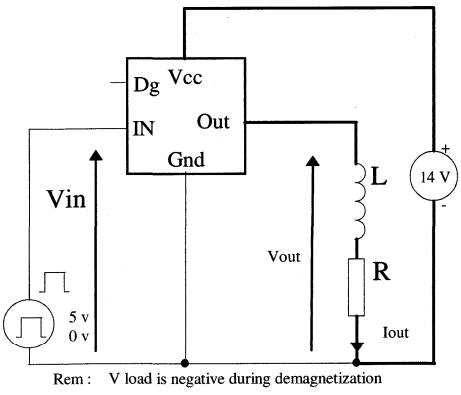


Figure 5 - Active clamp test circuit

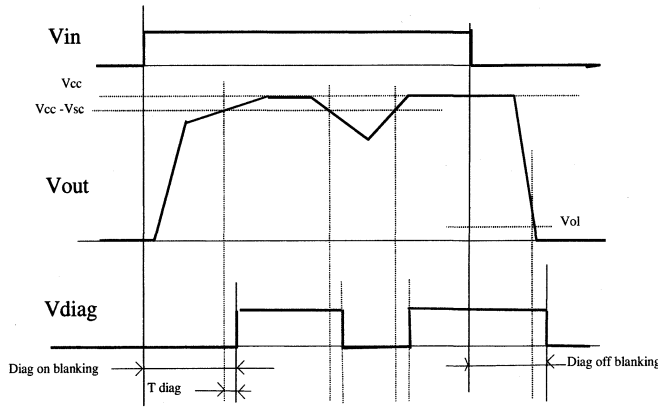


Figure 6 - Diagnostic delay definitions

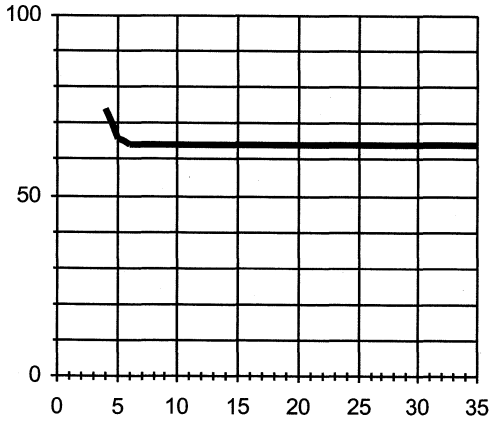


Figure 7 - $R_{ds(on)}$ (mΩ) Vs V_{cc} (V)

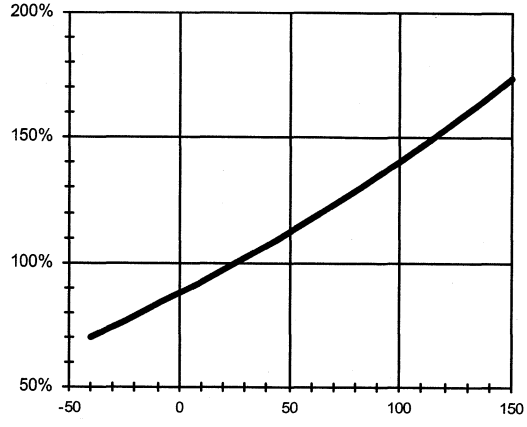


Figure 8 - Normalized $R_{ds(on)}$ (%) Vs T_j (°C)

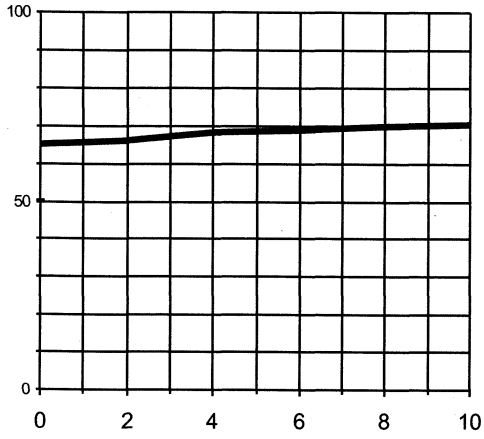


Figure 9 - Rds(on) (mΩ) Vs I_{out} (A)

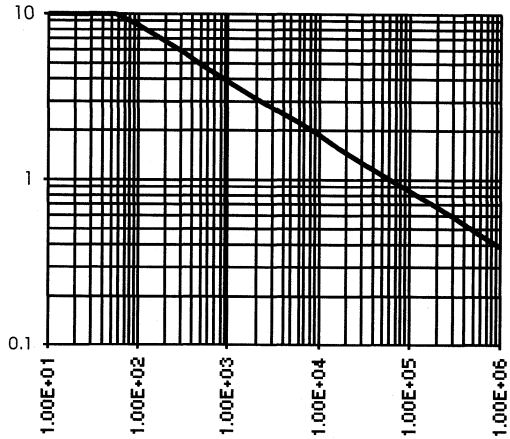


Figure 10 - Max. I_{out} (A) Vs Load Inductance (uH)

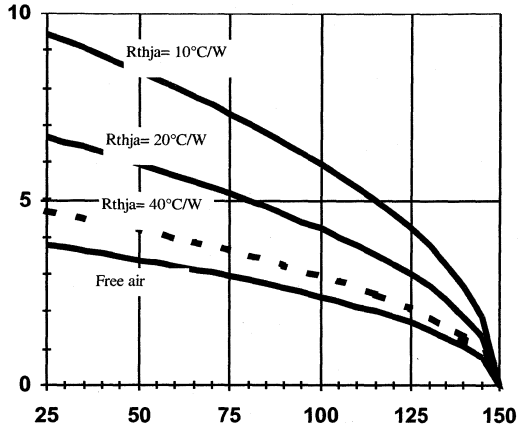


Figure 11a - Max load current (A) Vs Tamb (°C)
IPS521

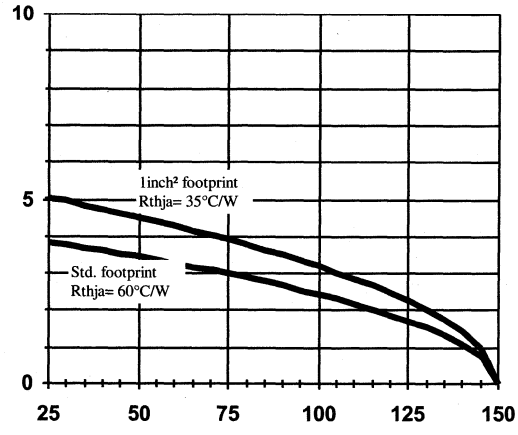


Figure 11b - Max load current (A) Vs Tamb (°C)
IPS521S

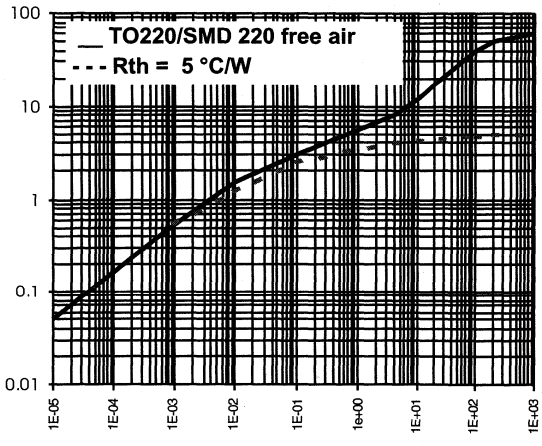


Figure 12 - Transient Thermal Impedance (°C/W)
Vs Time (S)

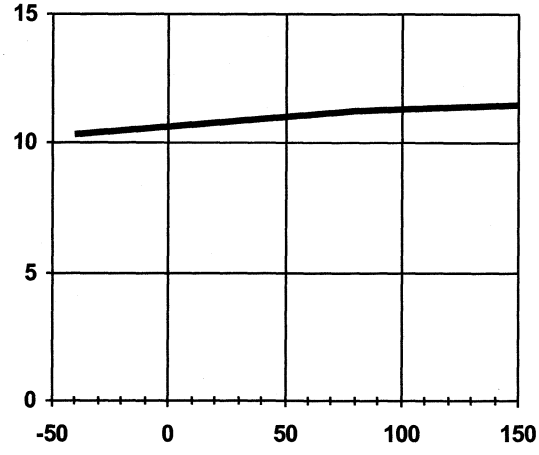


Figure 13 - I_{lim} (A) Vs Tj (°C)

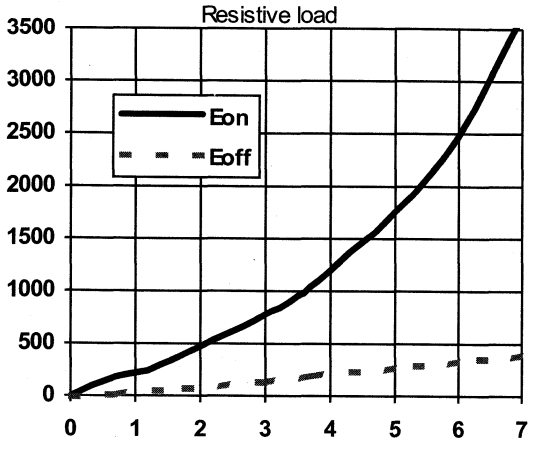


Figure 14 - E_{on}, E_{off} (μJ) Vs I_{out} (A)

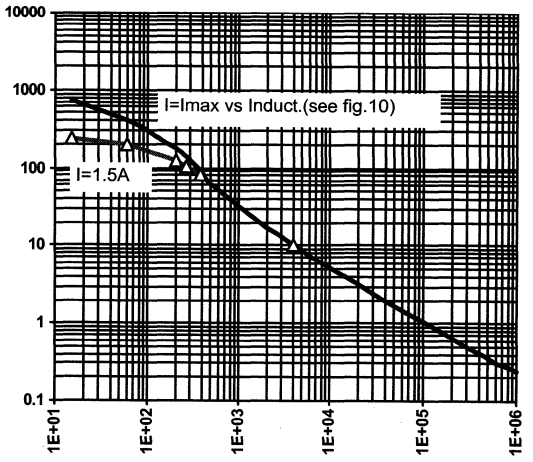


Figure 15 - E_{on} (μJ) Vs Load Inductance (μH)
(see Fig. 3)

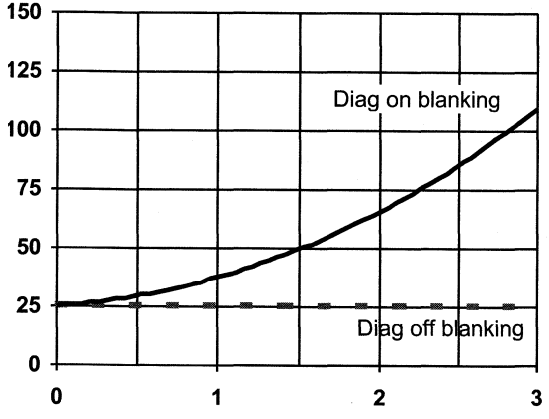


Figure 16 - Diag Blanking time (μS) Vs I_{out} (A)
(resistive load - see Fig. 6)

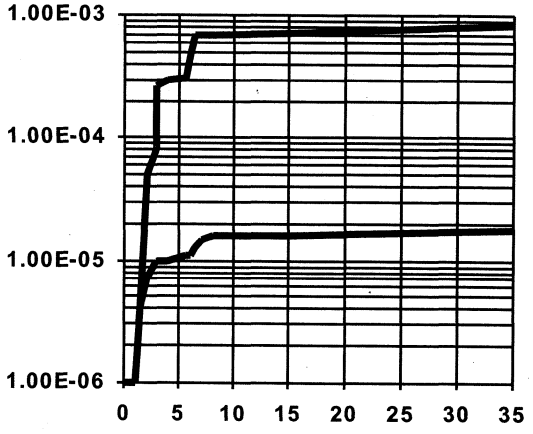
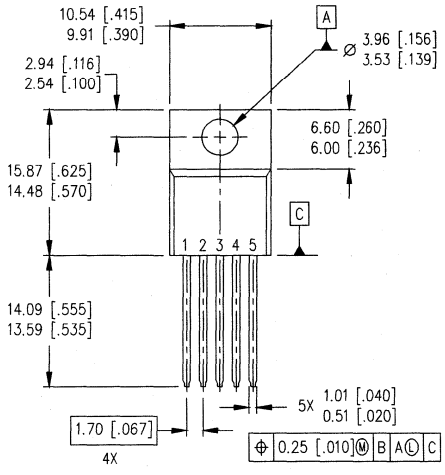
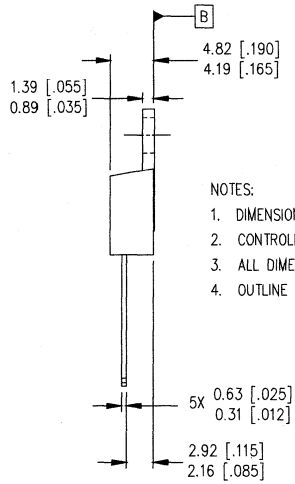


Figure 17 - I_{cc} (mA) Vs V_{cc} (V)

Case Outline 5 Lead - TO220

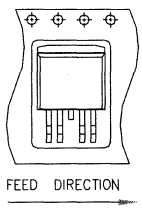


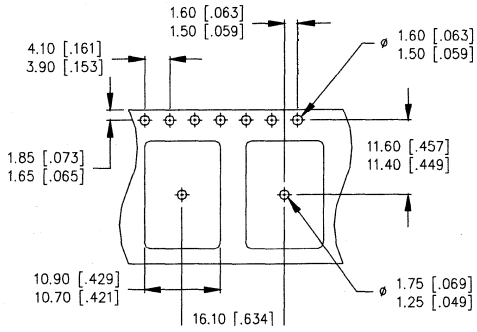


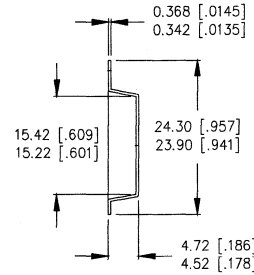
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TS-001.

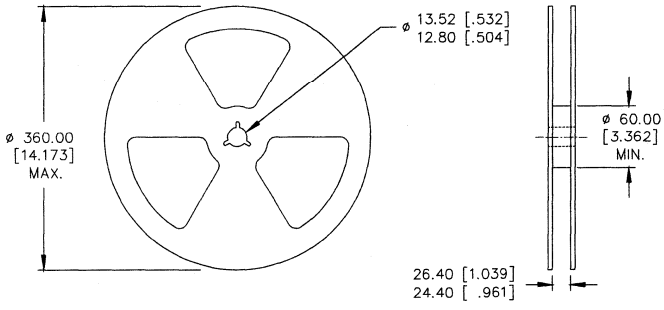
IRGB 01-3042 01

Tape & Reel 5 Lead - D²PAK (SMD220)





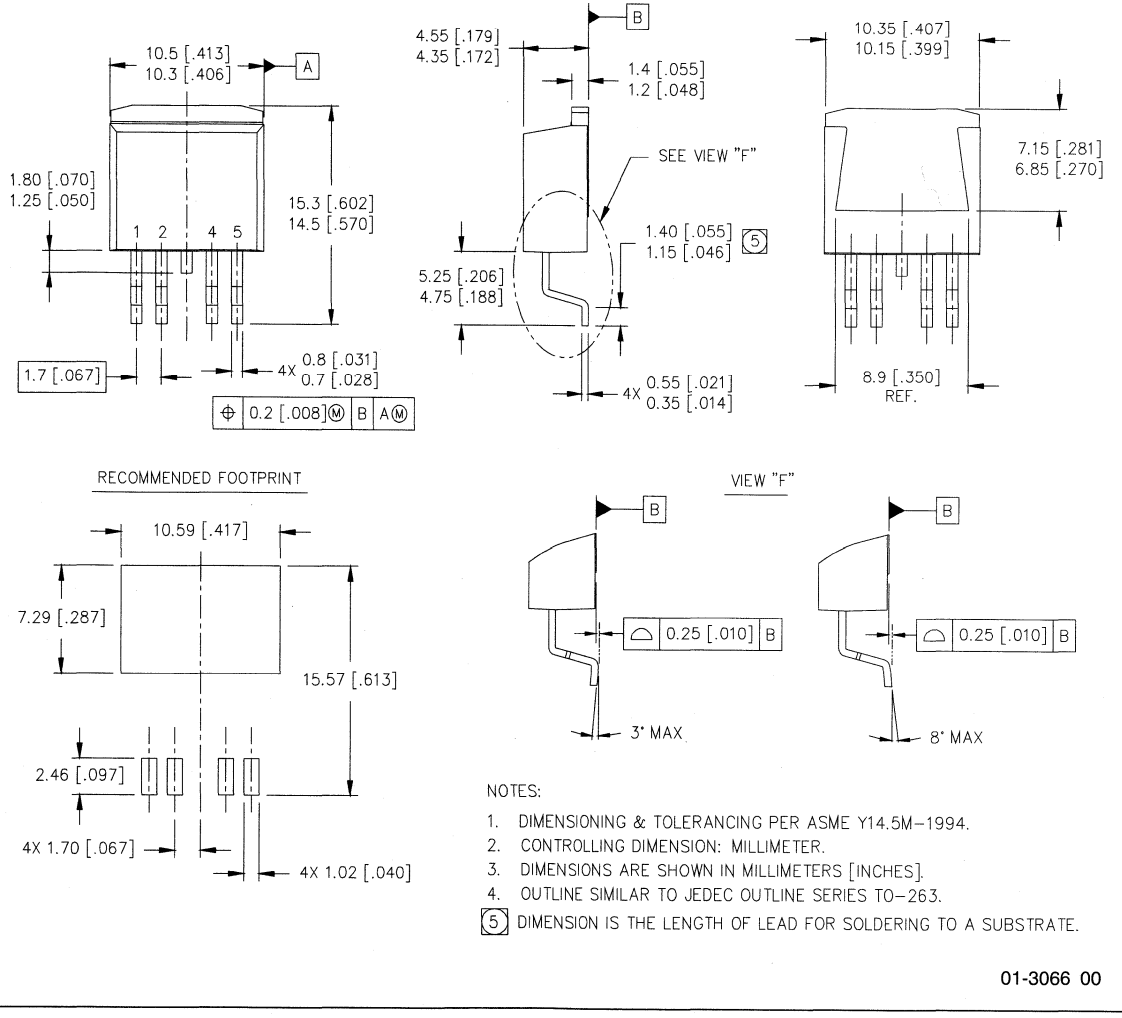




NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

01-3071 00 / 01-3072 0

Case Outline 5 Lead - D²PAK (SMD220)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO–263.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-3066 00

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IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

IPS521G

FULLY PROTECTED HIGH SIDE POWER MOSFET SWITCH

Features

- Over temperature protection (with auto-restart)
- Short-circuit protection (current limit)
- Active clamp
- E.S.D protection
- Status feedback
- Open load detection
- Logic ground isolated from power ground

Product Summary

$R_{ds(on)}$	100mΩ (max)
V_{clamp}	50V
I_{Limit}	10A
$V_{open\ load}$	3V

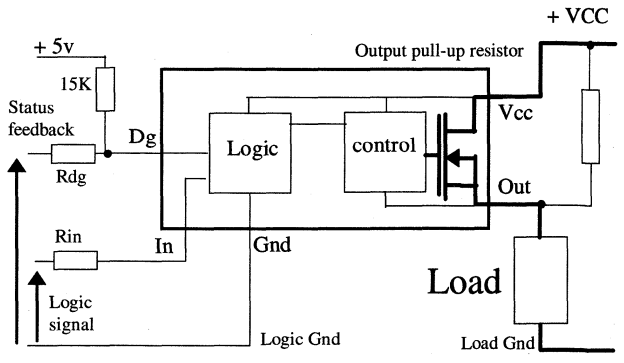
Description

The IPS521G is a fully protected five terminal high side switch with built in short circuit, over-temperature, ESD protection, inductive load capability and diagnostic feedback. The output current is controlled when it reaches I_{lim} value. The current limitation is activated until the thermal protection acts. The over-temperature protection turns off the high side switch if the junction temperature exceeds Tshutdown. It will automatically restart after the junction has cooled 7°C below Tshutdown. A diagnostic pin is provided for status feedback of short-circuit, over-temperature and open load detection. The double level shifter circuitry allows large offsets between the logic ground and the load ground.

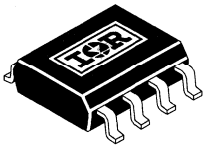
Truth Table

Op. Conditions	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Open load	H	H	H
Open load	L	H	H
Over current	H	L (limiting)	L
Over current	L	L	L
Over-temperature	H	L (cycling)	L
Over-temperature	L	L	L

Typical Connection



Package



8 Lead SOIC

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to GROUND lead. (T_j = 25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{out}	Maximum output voltage	V_{cc}-50	V_{cc}+0.3	V	
V_{offset}	Maximum logic ground to load ground offset	V_{cc}-50	V_{cc}+0.3		
V_{in}	Maximum Input voltage	-0.3	5.5		
$I_{in, max}$	Maximum positive IN current	-5	10	mA	
V_{dg}	Maximum diagnostic output voltage	-0.3	5.5	V	
$I_{dg, max}$	Maximum diagnostic output current	-1	10	mA	
$I_{sd\ cont.}$	Diode max. permanent current (1) (rth = 125°C/W)	—	1.4	A	
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
P_d	Maximum power dissipation (1) (rth=125°C/W)	—	1		
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
Vcc max.	Maximum Vcc voltage	—	50	V	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint	—	100	—	°C/W	8 Lead SOIC
R_{th2}	Thermal resistance with 1" square footprint	—	80	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{cc}	Continuous V_{cc} voltage	5.5	35	V
V_{IH}	High level input voltage	4	5.5	
V_{IL}	Low level input voltage	-0.3	0.9	
I_{out} Tc=85°C	Continuous output current (TAmbient = 85°C, Tj = 125°C, R_{th} = 100°C/W)	—	1.6	A
R_{in}	Recommended resistor in series with IN pin	4	6	kΩ
R_{dg}	Recommended resistor in series with DG pin	10	20	

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Static Electrical Characteristics

(T_j = 25°C, V_{cc} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance T_j = 25°C	—	80	100	mΩ	V_{in} = 5V, I_{out} = 5A
$R_{ds(on)}$ (V_{cc}=6V)	ON state resistance @ V_{cc} = 6V	—	80	100		V_{in} = 5V, I_{out} = 2.5A
$R_{ds(on)}$ @Tj=150°C	ON state resistance Tj = 150°C	—	125	160		V_{in} = 5V, I_{out} = 5A
V_{cc} oper.	Operating voltage range	5.5	—	35	V	
V clamp 1	V_{cc} to OUT clamp voltage 1	50	55	—		I_d = 10mA (see Fig.1 & 2)
V clamp 2	V_{cc} to OUT clamp voltage 2	—	56	65		I_d = I_{sd} (see Fig.1 & 2)
V_f	Body diode forward voltage	—	0.9	1.2		I_d = 2.5A, V_{in} = 0V
I_{cc} off	Supply current when OFF	—	13	50	µA	V_{in} = 0V, V_{out} = 0V
I_{cc} on	Supply current when ON	—	0.6	2	mA	V_{in} = 5V
I_{cc} ac	Ripple current when ON (AC RMS)	—	20	—	µA	V_{in} = 5V
Vdgl	Low level diagnostic output voltage	—	0.4	—	V	I_{dg} = 1.6 mA
Ioh	Output leakage current	—	50	120	µA	V_{out} = 6V
Iol	Output leakage current	0	—	25		V_{out} = 0V
Idg leakage	Diagnostic output leakage current	—	—	10		Vdg = 5.5V
V_{ih}	IN high threshold voltage	—	2.2	3	V	
V_{il}	IN low threshold voltage	1	1.9	—		
$I_{in,\ on}$	On state IN positive current	—	70	200	µA	V_{in} = 5V
In hyst.	Input hysteresis	0.1	0.25	0.5	V	

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 2.8Ω, T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Td_{on}	Turn-on delay time	—	10	40	µs	See figure 3
T_{r1}	Rise time to V_{out} = V_{cc} - 5V	—	25	60		
T_{r2}	Rise time V_{cc} - 5V to V_{out} = 90% of V_{cc}	—	130	200		
dV/dt (on)	Turn ON dV/dt	—	0.7	2	V/µs	
E_{on}	Turn ON energy	—	1500	—	µJ	
Td_{off}	Turn-off delay time	—	35	70	µs	See figure 4
T_f	Fall time to V_{out} = 10% of V_{cc}	—	16	50		
dV/dt (off)	Turn OFF dV/dt	—	0.9	3	V/µs	
E_{off}	Turn OFF energy	—	250	—	µJ	
Tdiag	Vout to Vdiag propagation delay	—	5	15	µs	See figure 6

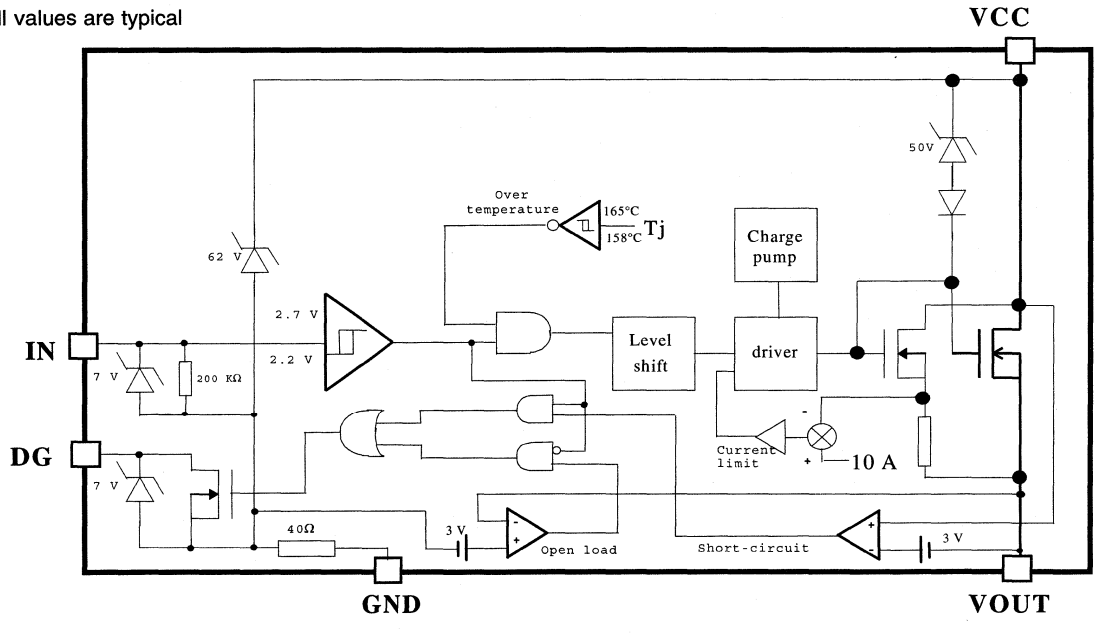
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	7	10	14	A	V_{out} = 0V
T_{sd+}	Over-temp. positive going threshold	—	165	—	°C	See fig. 2
T_{sd-}	Over-temp. negative going threshold	—	158	—	°C	See fig. 2
V_{sc}	Short-circuit detection voltage (3)	2	3	4	V	See fig. 2
$V_{open\ load}$	Open load detection threshold	2	3	4	V	

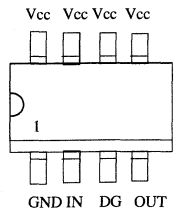
(3) Referenced to V_{cc}

Functional Block Diagram

All values are typical



Lead Assignments



8 Lead SOIC

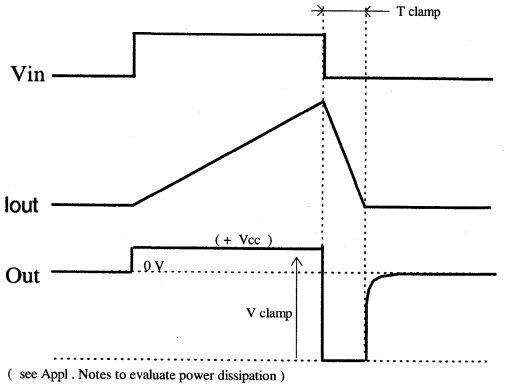


Figure 1 - Active clamp waveforms

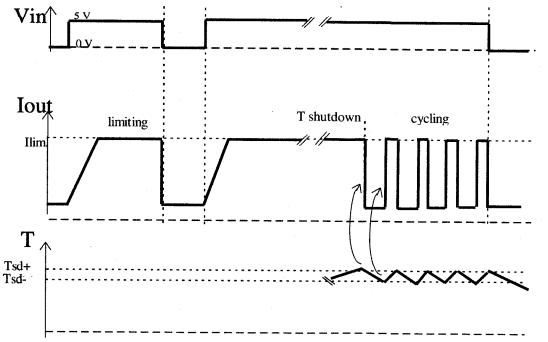


Figure 2 - Protection timing diagram

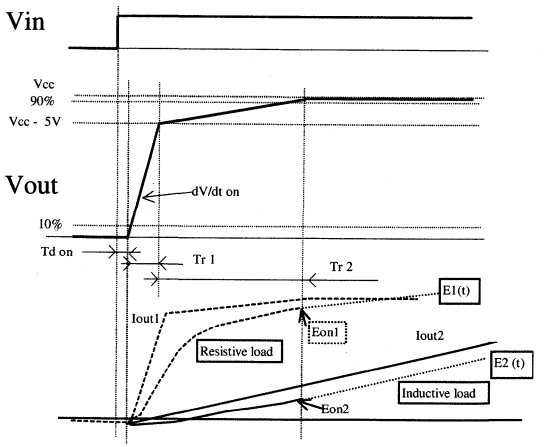


Figure 3 - Switching times definition (turn-on)
Turn on energy with a resistive or an inductive load

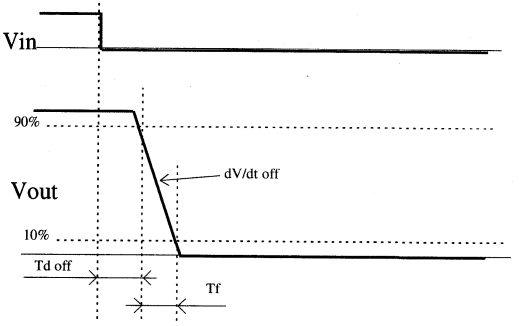


Figure 4 - Switching times definition (turn-off)

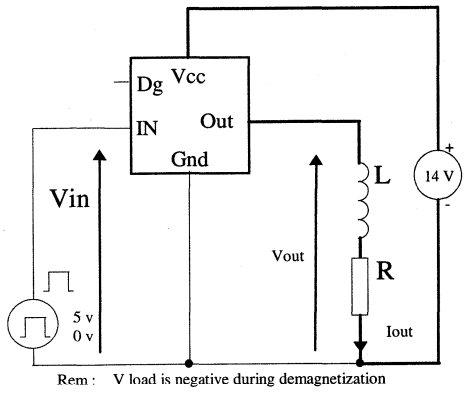


Figure 5 - Active clamp test circuit

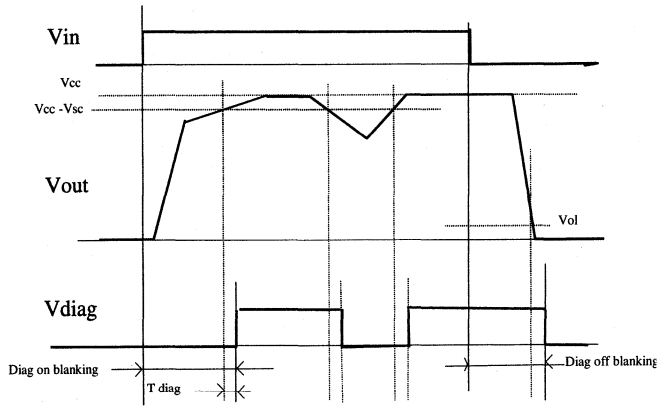


Figure 6 - Diagnostic delay definitions

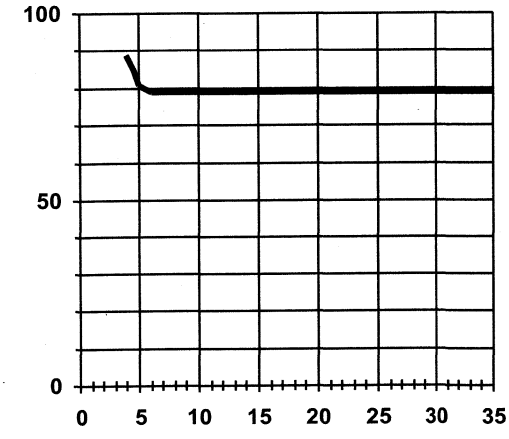


Figure 7 - $R_{ds(on)}$ (mΩ) Vs V_{CC} (V)

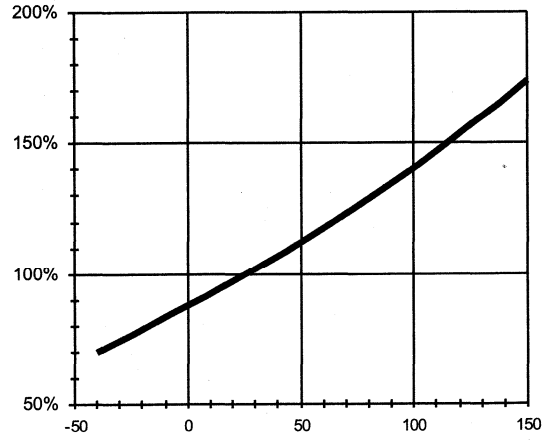


Figure 8 - Normalized $R_{ds(on)}$ (mΩ) Vs T_j (°C)

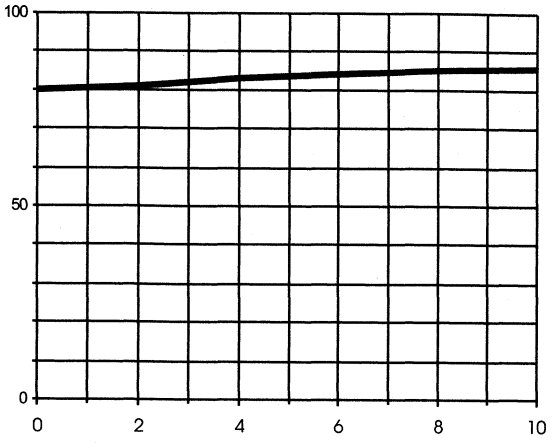


Figure 9 - Rds(on) (mΩ) Vs I_{out} (A)

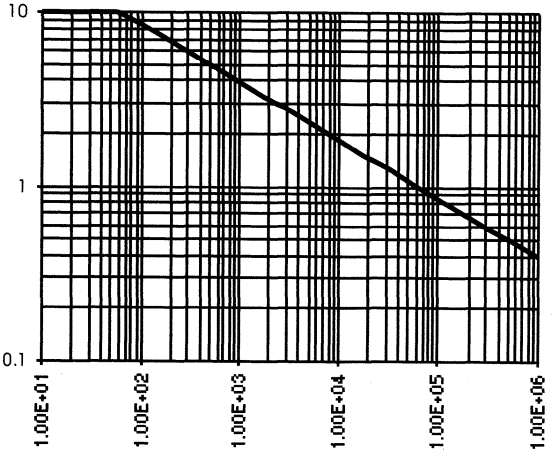


Figure 10 - Max. I_{out} (A) Vs Load Inductance (uH)

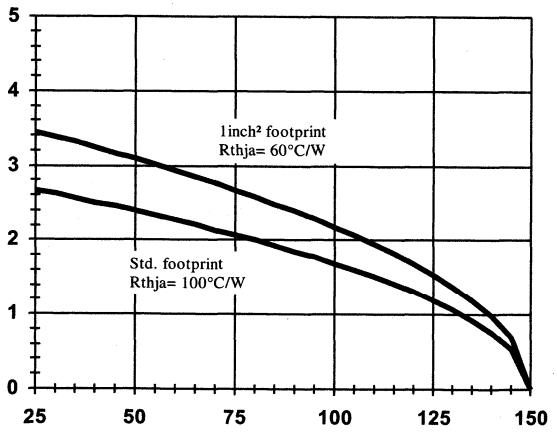


Figure 11 - Max load current (A) Vs Tamb (°C)

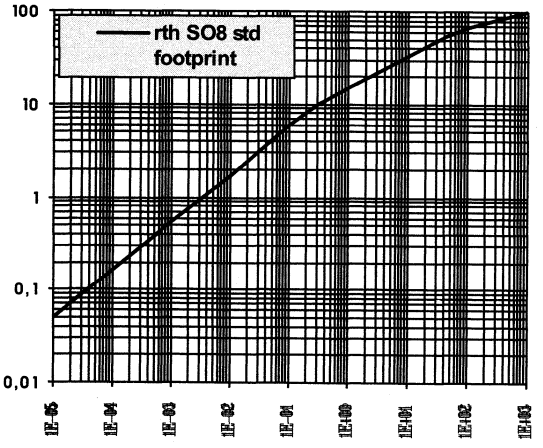


Figure 12 - Transient Thermal Impedance (°C/W) Vs Time (s)

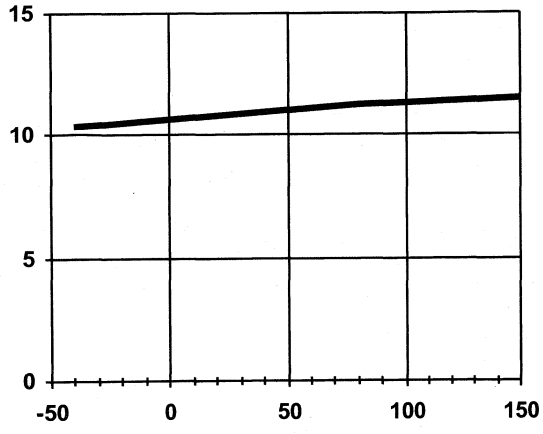


Figure 13 - I_{lim} (A) Vs Tj (°C)

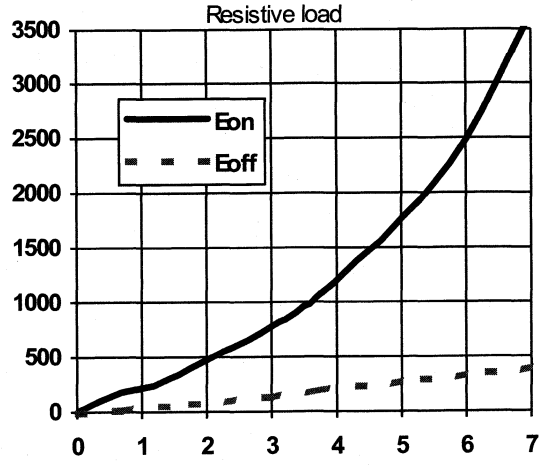


Figure 14 - E_{on}, E_{off} (µJ) Vs I_{out} (A)

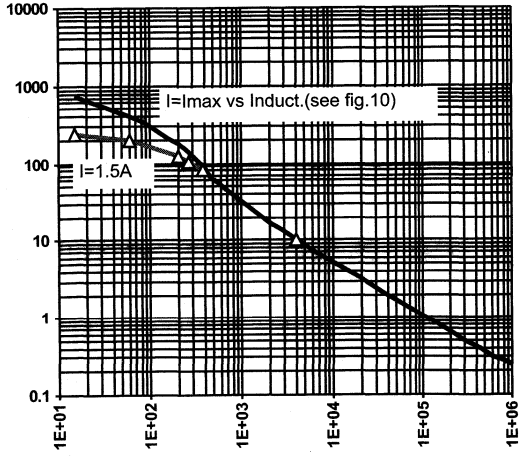


Figure 15 - E_{on} (µJ) Vs Load Inductance (µH)
(see Fig. 3)

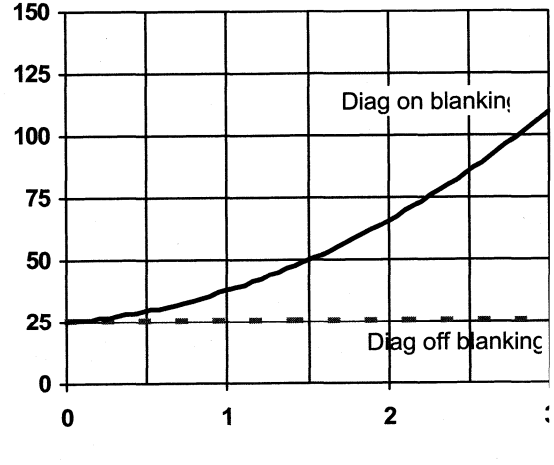


Figure 16 - Diag Blanking time (µS) Vs I_{out} (A)
(resistive load - see Fig. 6)

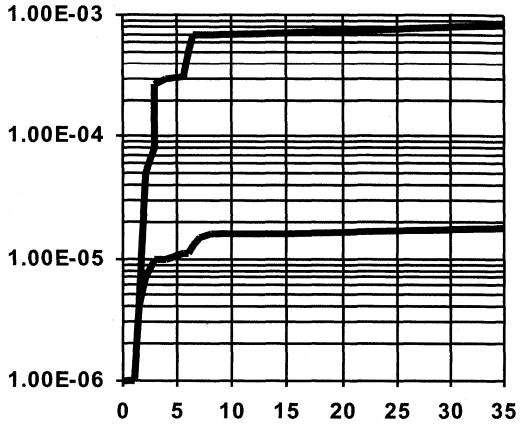
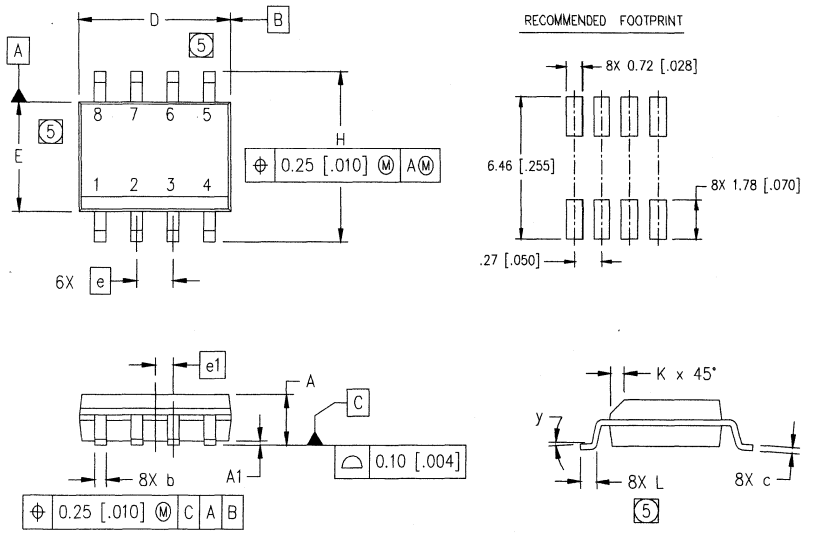


Figure 17 - I_{cc} (mA) Vs V_{cc} (V)

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

4/11/2000

International
IOR Rectifier

IPS5451/IPS5451S

FULLY PROTECTED HIGH SIDE POWER MOSFET SWITCH

Features

- Over temperature protection (with auto-restart)
- Over current shutdown
- Active clamp
- E.S.D protection
- Status feedback
- Open load detection
- Logic ground isolated from power ground

Product Summary

$R_{ds(on)}$	25mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	35A
$I_{open\ load}$	1A

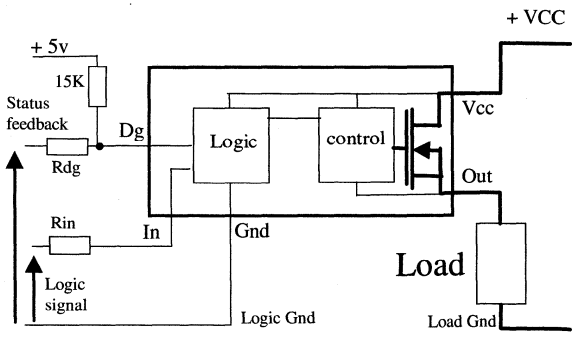
Description

The IPS5451/IPS5451S are fully protected five terminal high side switch with built in short circuit, over-temperature, ESD protection, inductive load capability and diagnostic feedback. The over-current protection latches off the device if the output current exceeds Ishutdown. It can be reset by turning the input pin low. The over-temperature protection turns off the high side switches if the junction temperature exceeds Tshutdown. It will automatically restart after the junction has cooled 7°C below Tshutdown. A diagnostic pin is provided for status feedback of over-current, over-temperature and open load detection. The double level shifter circuitry allows large offsets between the logic ground and the load ground.

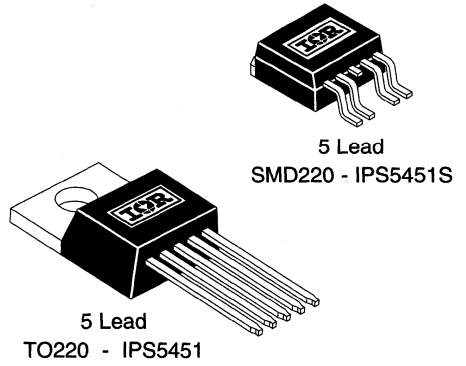
Truth Table

Op. Conditions	In	Out	Dg
Normal	H	H	H
Normal	L	L	H
Open load	H	H	L
Open load	L	X	H
Over current	H	L (latched)	L
Over current	L	L	H
Over-temperature	H	L (cycling)	L (cycling)
Over-temperature	L	L	H

Typical Connection



Packages



5 Lead
SMD220 - IPS5451S

5 Lead
TO220 - IPS5451

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to GROUND lead. ($T_{Ambient}$ = 25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{out}	Maximum output voltage	V_{CC}-45	V_{CC}+0.3	V	
V_{offset}	Maximum logic ground to load ground offset	V_{CC}-45	V_{CC}+0.3		
V_{in}	Maximum Input voltage	-0.3	5.5		
$I_{in, max}$	Maximum IN current	-5	10	mA	
V_{dg}	Maximum diagnostic output voltage	-0.3	5.5	V	
$I_{dg, max}$	Maximum diagnostic output current	-1	10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(rth=62°C/W) IPS5451	—	2.8		
	(rth=80°C/W) IPS5451S	—	2.2		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	45		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
P_d	Maximum power dissipation(1)			W	
	(rth=62°C/W) IPS5451	—	2		
	(rth=80°C/W) IPS5451S	—	1.56		
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
T_{lead}	Lead temperature (soldering 10 seconds)	—	300		
Vcc max.	Maximum Vcc voltage	—	45	V	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance junction to case	—	2	—	°C/W	TO-220
R_{th} 2	Thermal resistance junction to ambient	—	55	—		
R_{th} 1	Thermal resistance with standard footprint	—	60	—		D^2PAK (SMD220)
R_{th} 2	Thermal resistance with 1" square footprint	—	35	—		
R_{th} 3	Thermal resistance junction to case	—	5	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{cc}	Continuous V_{cc} voltage	5.5	18	V
V_{IH}	High level input voltage	4	5.5	
V_{IL} 1	Low level input voltage	-0.3	0.9	
I_{out}	Continuous output current			A
	(TAmbient = 85°C, Tj = 125°C, R_{th} = 62°C/W) IPS5451	—	4	
	(TAmbient = 85°C, Tj = 125°C, R_{th} = 80°C/W) IPS5451S	—	3.5	
I_{out} Tc=85°C	Continuous output current (TCase = 85°C, IN = 5V, Tj = 125°C, R_{th} = 5°C/W)	—	14	
R_{in}	Recommended resistor in series with IN pin	4	6	kΩ
R_{dg}	Recommended resistor in series with DG pin	10	20	

Static Electrical Characteristics

(T_j = 25°C, V_{cc} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance T_j = 25°C	—	19	25	mΩ	V_{in} = 5V, I_{out} = 14A
$R_{ds(on)}$ (V_{cc}=6V)	ON state resistance @ V_{cc} = 6V	—	22	30		V_{in} = 5V, I_{out} = 7A
$R_{ds(on)}$ @Tj=150°C	ON state resistance Tj = 150°C	—	32	—		V_{in} = 5V, I_{out} = 14A
V_{cc} oper.	Functional operating range	5.5	—	35	V	
V clamp 1	V_{cc} to OUT clamp voltage 1	45	49	—		I_d = 10mA (see Fig.1 & 2)
V clamp 2	V_{cc} to OUT clamp voltage 2	—	50	60		I_d = $I_{shutdown}$ (see Fig.1 & 2)
V_f	Body diode forward voltage	—	0.9	1.2		I_d = 14A, V_{in} = 0V
I_{out} leakage	Output leakage current	—	10	50	µA	V_{out} = 0V, Tj = 25°C
I_{cc} off	Supply current when OFF	—	10	50		V_{in} = 0V, V_{out} = 0V
I_{cc} on	Supply current when ON	—	3.5	10	mA	V_{in} = 5V
I_{cc} ac	Ripple current when ON (AC RMS)	—	20	—	µA	V_{in} = 5V
Vdgl	Low level diagnostic output voltage	—	0.1	0.4	V	I_{dg} = 1.6 mA
Idg leakage	Diagnostic output leakage current	—	1.5	10	µA	V_{dg} = 4.5V
V_{ih}	IN high threshold voltage	—	2.7	3.4	V	
V_{il}	IN low threshold voltage	1	2.0	—		
$I_{in,\ on}$	On state IN positive current	—	30	80	µA	V_{in} = 4V
V_{ccuv+}	V_{cc} UVLO positive going threshold	—	4.7	5.5	V	
V_{ccuv-}	V_{cc} UVLO negative going threshold	3.0	4.4	—		
$In_{hyst.}$	Input hysteresis	0.2	0.6	1.5		

Switching Electrical Characteristics

V_{CC} = 14V, Resistive Load = 1Ω, T_j = 25°C, (unless otherwise specified).

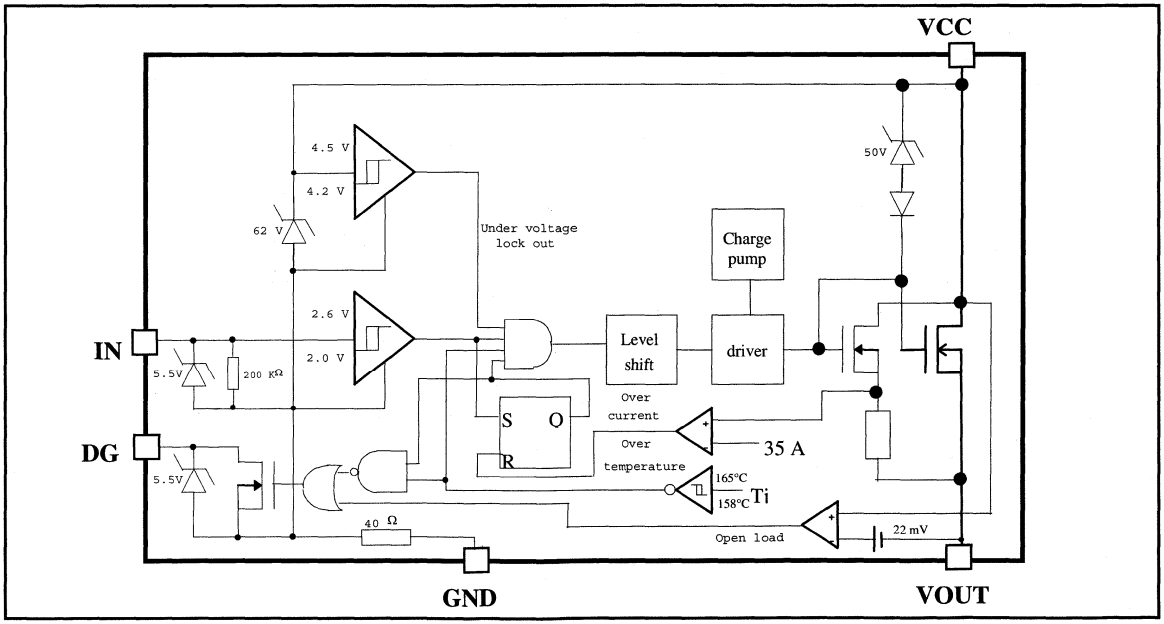
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Td_{on}	Turn-on delay time	—	5	20	µs	See figure 3
T_{r1}	Rise time to V_{out} = V_{CC} - 5V	—	4	20		
T_{r2}	Rise time from the end of Tr1 to V_{out} = 90% of V_{CC}	—	65	150		
dV/dt (on)	Turn ON dV/dt	—	3	6	V/µs	
E_{on}	Turn ON energy	—	3	—	mJ	See figure 4
Td_{off}	Turn-off delay time	—	65	150	µs	
T_f	Fall time to V_{out} = 10% of V_{CC}	—	8	20		
dV/dt (off)	Turn OFF dV/dt	—	5	10	V/µs	
E_{off}	Turn OFF energy	—	0.75	—	mJ	

Protection Characteristics

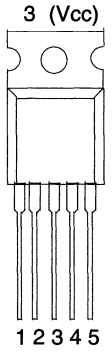
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd+}	Over-temp. positive going threshold	—	165	—	°C	See fig. 2
T_{sd-}	Over-temp. negative going threshold	—	158	—	°C	See fig. 2
I_{sd}	Over-current threshold	22	35	50	A	See fig. 2
$I_{open\ load}$	Open load detection threshold	0.3	1	2	A	
T_{reset}	Minimum time to reset protections	—	50	—	µs	V_{in} = 0V
T_{dg}	Blanking time before considering Dg	—	7	100	µs	Part turned on with Vin =5V

Functional Block Diagram

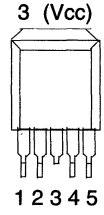
All values are typical



Lead Assignments



1 - Ground
2 - In
3 - Vcc
4 - DG
5 - Out



5 Lead - TO220	5 Lead - D²PAK (SMD220)
IPS5451	**IPS5451S**
Part Number	

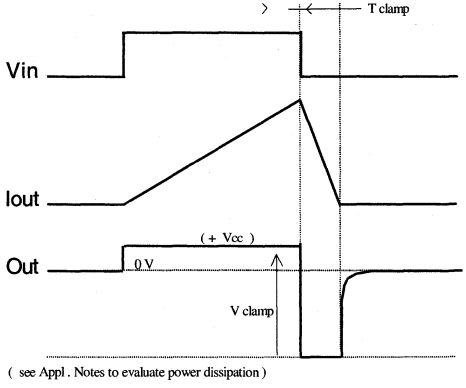


Figure 1 - Active clamp waveforms

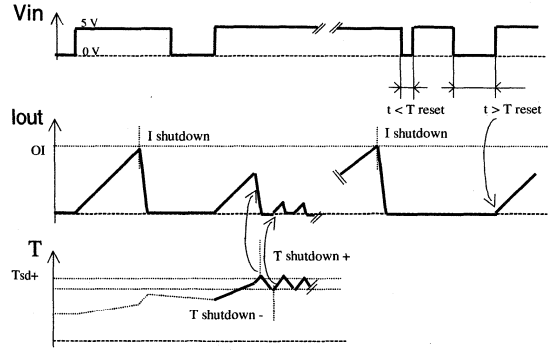


Figure 2 - Protection timing diagram

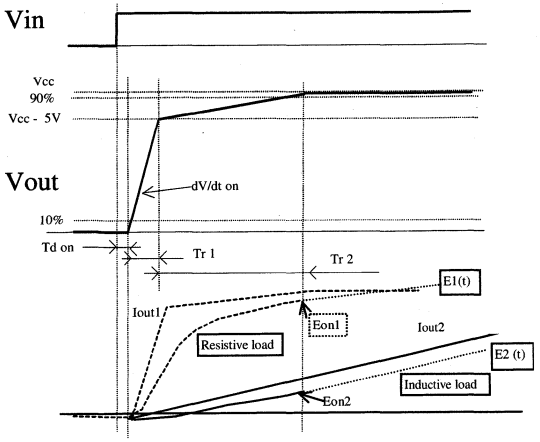


Figure 3 - Switching times definition (turn-on)
Turn on energy with a resistive or an inductive load

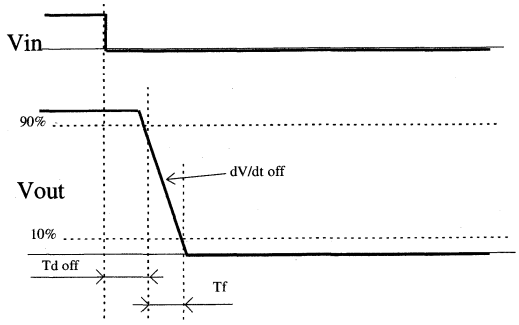


Figure 4 - Switching times definition (turn-off)

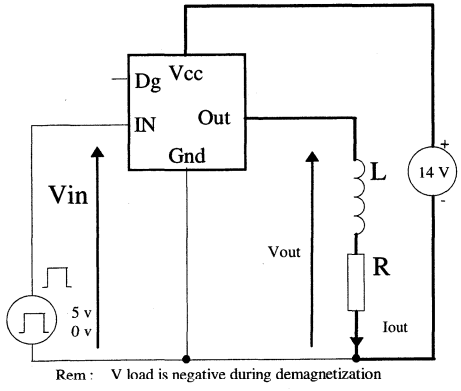


Figure 5 - Active clamp test circuit

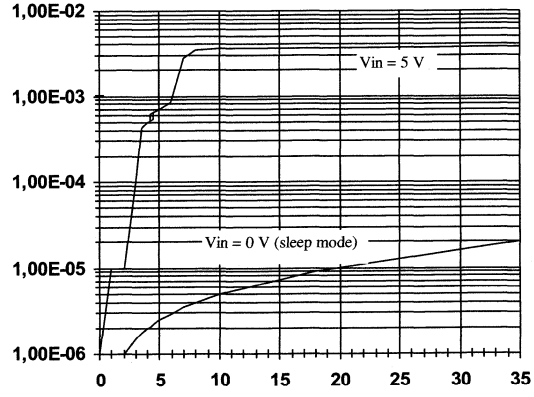


Figure 6 - Icc (mA) Vs Vcc (V)

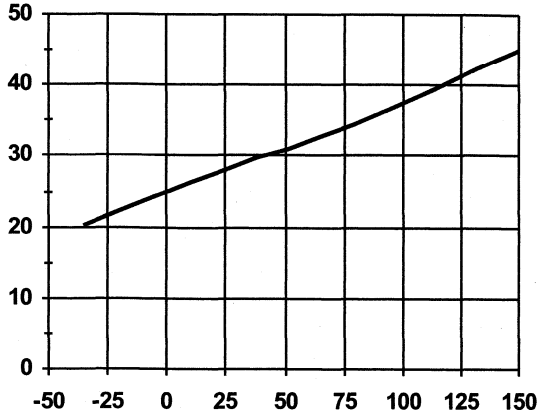


Figure 7 - Iin (µA) Vs Tj (°C)

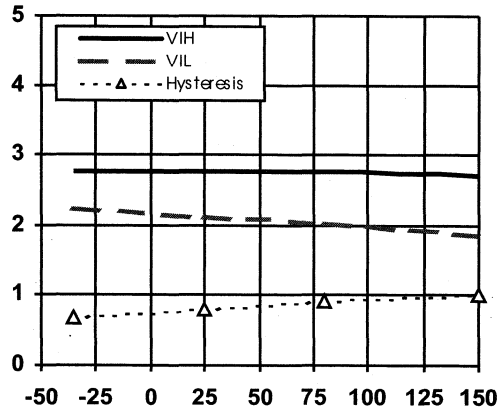


Figure 8 - VIH, VIL threshold (V) Vs Tj (°C)

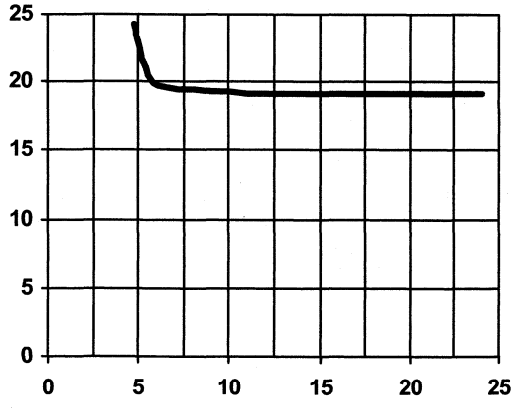


Figure 9 - Rdson (mΩ) vs Vcc (V)

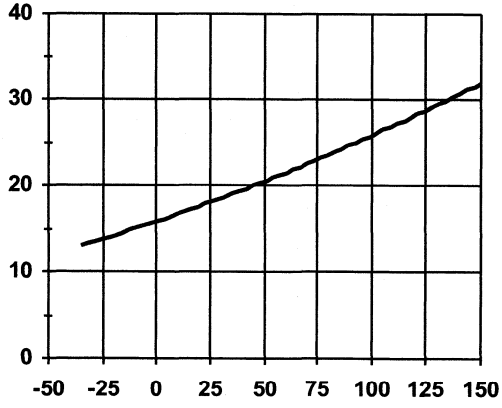


Figure 10 - Rdson (mΩ) vs Tj (°C)

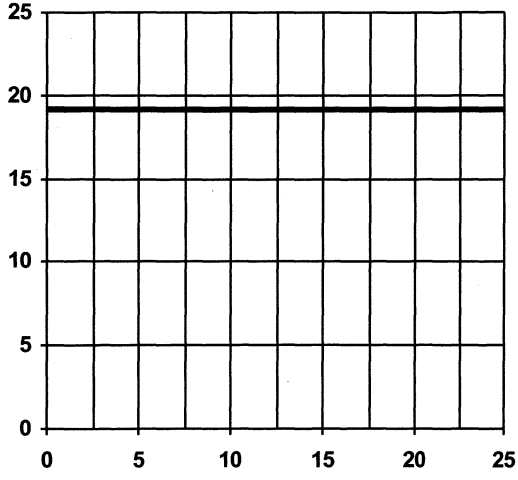


Figure 11 - Rdson (mΩ) vs Iout (A)

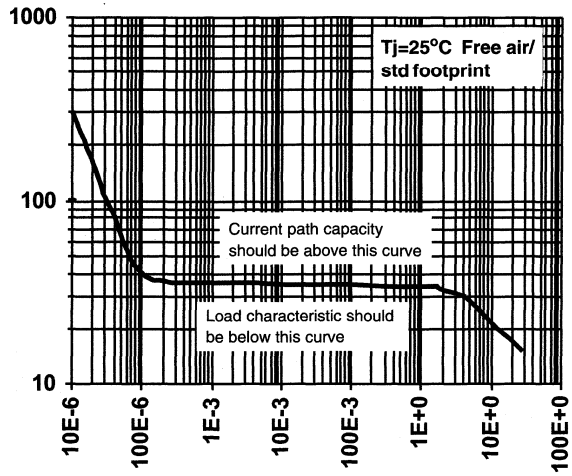


Figure 12 - Isd (A) vs Time (S)

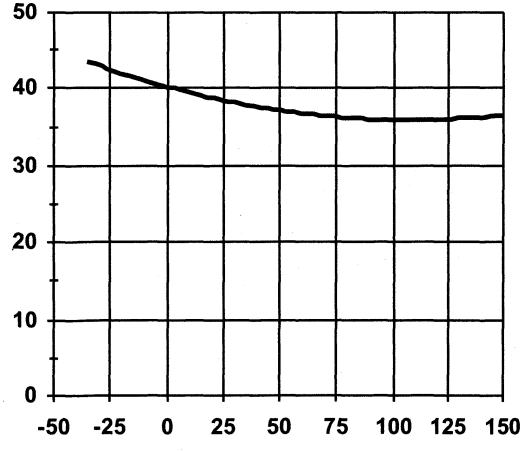


Figure 13 - Isd (A) vs Tj (°C)

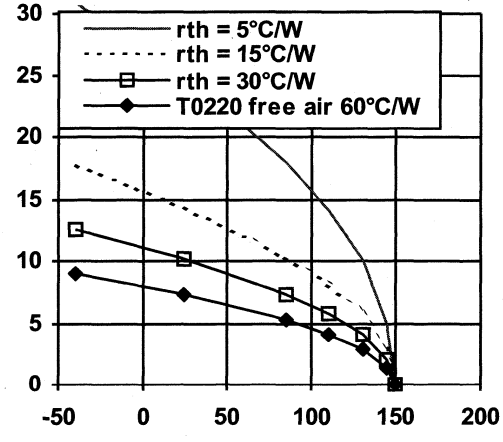


Figure 14 - Max. Cont. Ids (A) Vs
Amb. Temperature (°C)

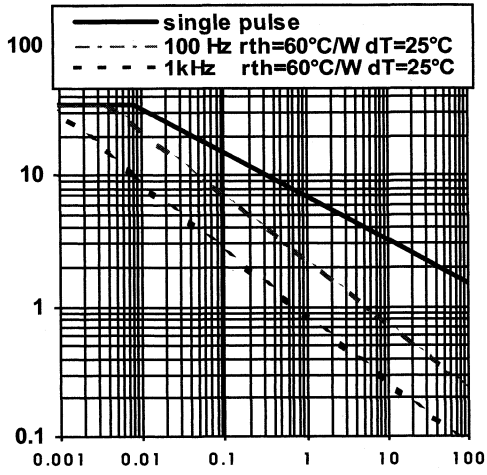


Figure 15 -Max. I clamp (A) Vs Inductive Load (m H)

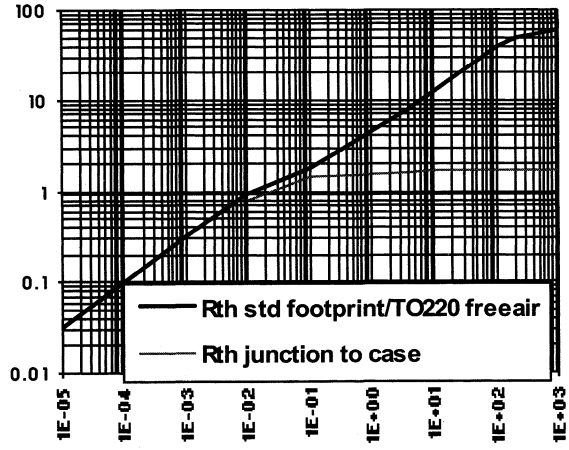


Figure 16 - Transient Rth (°C/W) Vs Time (s)

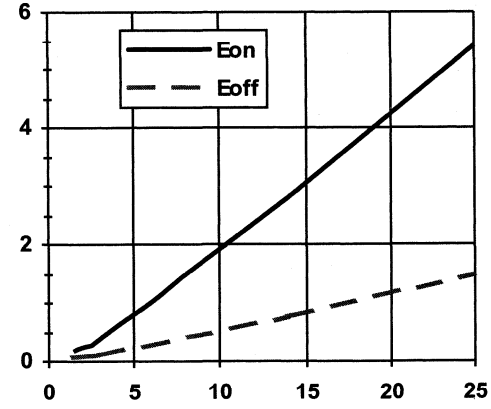


Figure 17 - Eon, Eoff (mJ) vs I_{out} (A)

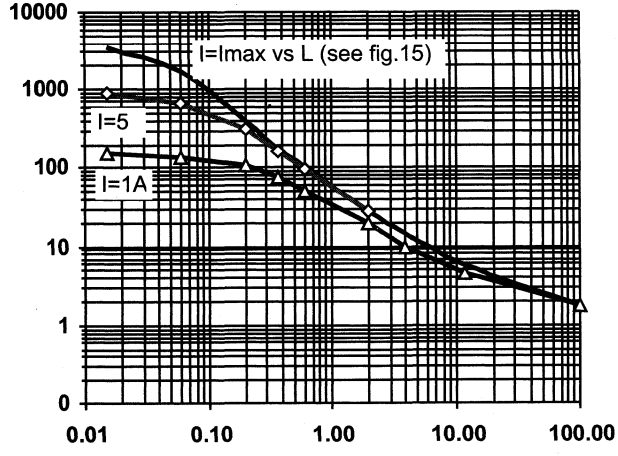


Figure 18 - Eon @ Vcc=14V (mJ) vs Inductance (mH)

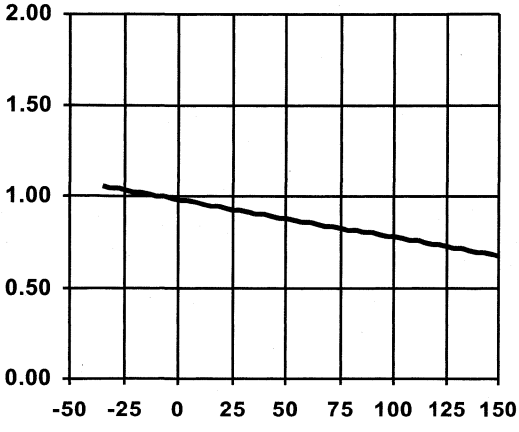


Figure 19 - I open load (A) vs Tj (°C)

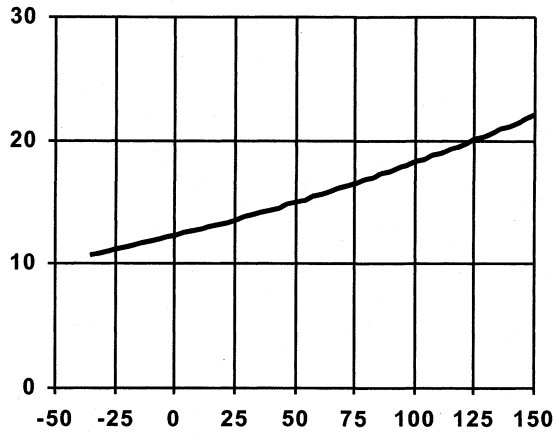
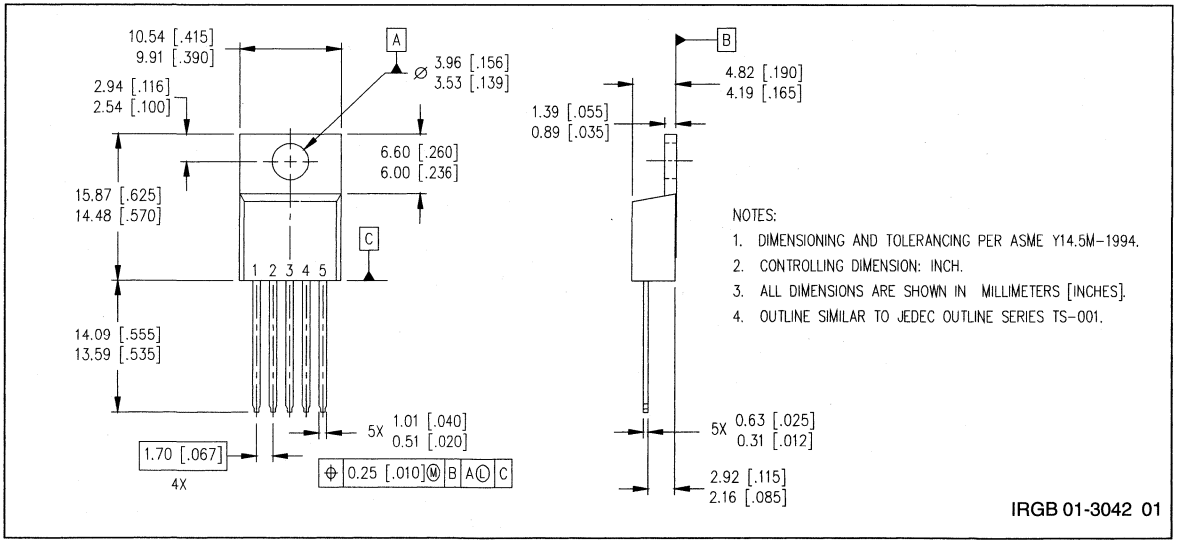
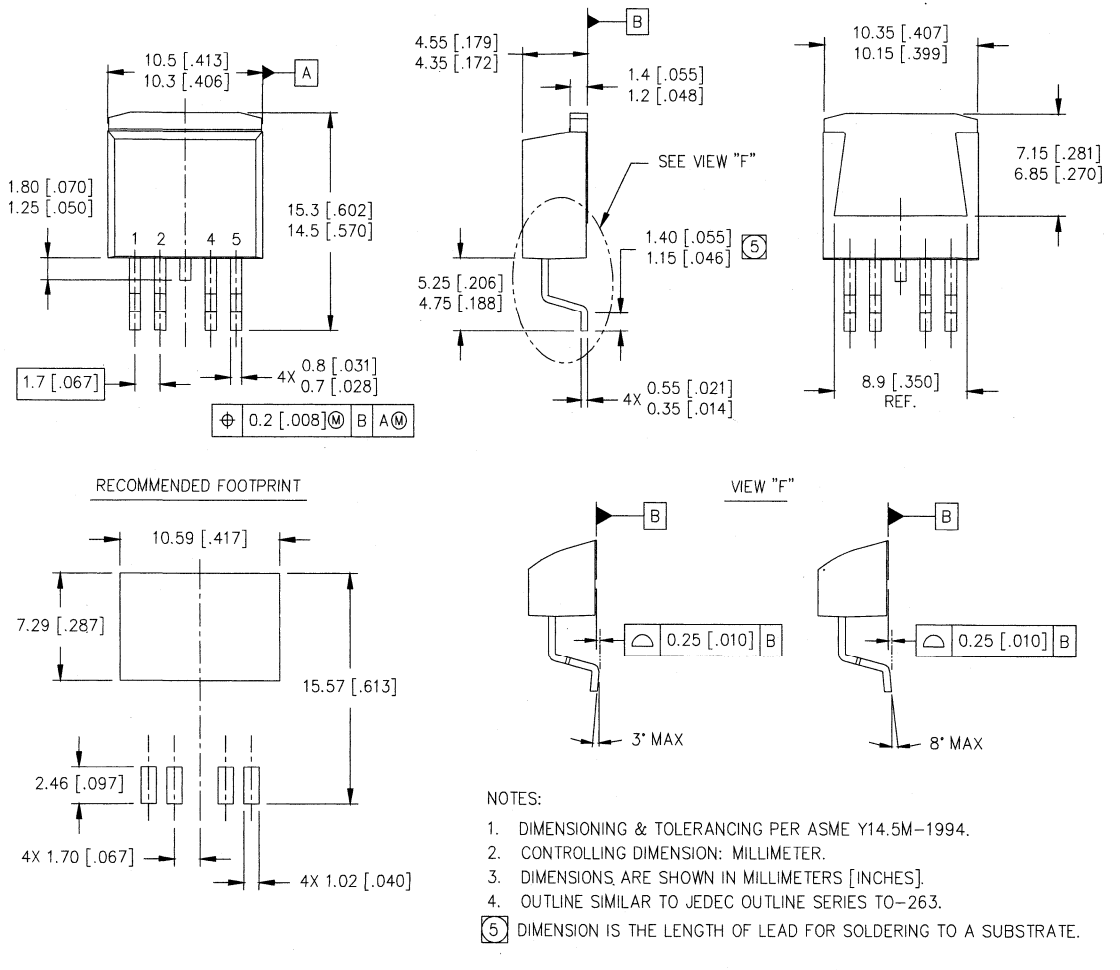


Figure 20 - Icc off (µA) vs Tj (°C)

Case Outline - TO220 (5 lead)



Case Outline - D²PAK (SMD220) - 5 Lead



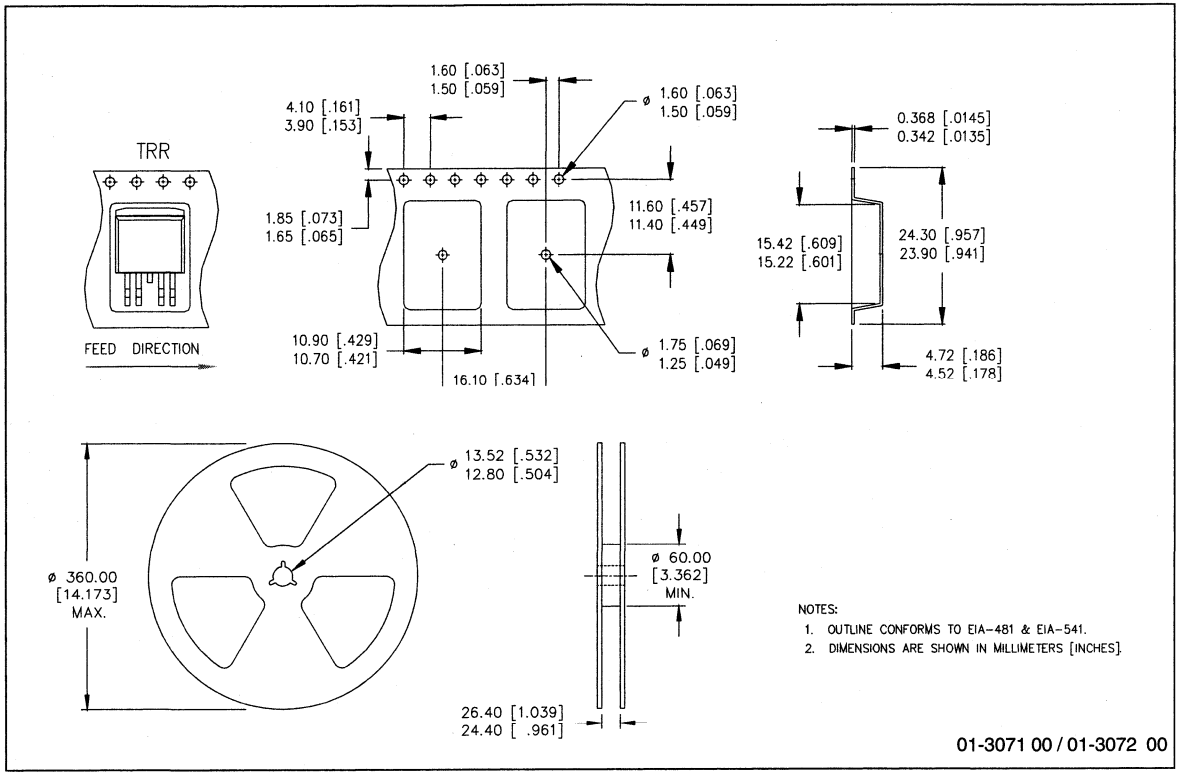
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO–263.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-3066 00

Tape & Reel - D²PAK (SMD220) - 5 Lead



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

IPS5551T

FULLY PROTECTED HIGH SIDE POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Input referenced to + V_{CC}
- E.S.D protection
- Input referenced to

Description

The IPS5551T is a fully protected three terminal high side switch with built-in short-circuit, over-temperature, ESD protection, inductive load capability. The input signal is referenced to Vcc. When the input voltage Vcc - Vin is higher than the specified threshold, the output power MOSFET is turned on. When the Vcc - Vin is lower than the specified Vil threshold, the output MOSFET is turned off. Input noise immunity is improved by an hysterisis. When the input is left floating, an internal current source pulls it up to Vcc. The overcurrent protection latches off the high side switch if the output current exceeds the specified Isd. The overtemperature protection latches off the switch if the junction temperature exceeds the specified value Tsd. The device is reset by opening the input pin high.

Product Summary

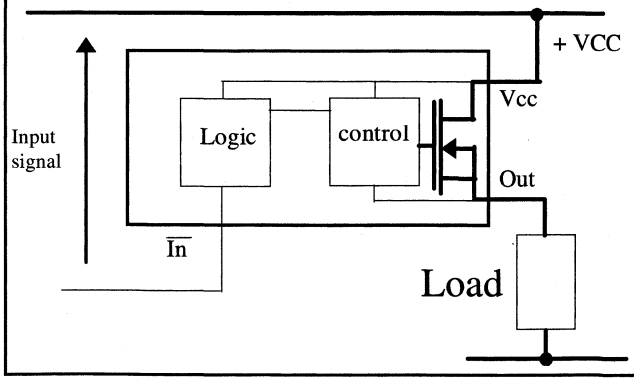
$R_{ds(on)}$	5.2mΩ (max)
V clamp	40V
Ishutdown	100A
V_{cc} (op.)	5.5 - 18V

Truth Table

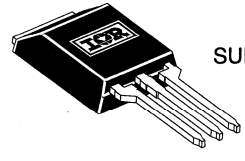
Op. Conditions	$\overline{In}$ (3)	Out
Normal	L	H
Normal	H	L
Over current	L	L (latched)
Over current	H	L
Over-temperature	L	L (latched)
Over-temperature	H	L

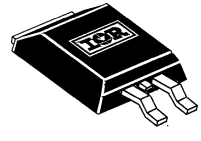
(3) $\overline{In}$ is referenced to Vcc.
$\overline{In}$ = L means (Vcc -Vin) >Vih
$\overline{In}$ = H means (Vcc - Vin) <Vil

Typical Connection



Packages


SUPER TO220


SUPER SMD220
Advance Information

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to V_{CC} lead. (T_j = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70μm copper thickness

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{CC} -V_{in} max	Maximum input voltage	-0.3	30	V	
V_{CC} -V_{in1} max	Max. transient Input voltage (less than 1s)	-0.3	40		
I_{in} max	Maximum input current	-1	20	mA	
V_{CC} -V_{out} max	Maximum output voltage	-0.3	40	V	
I_{sd} cont.	Diode max. continuous current (1) (rth = 62°C/W)	—	2.8	A	
I_{sd1} cont.	Diode max. continuous current (1) (rth = 5°C/W)	—	35		
I_{sd} pulsed	Diode max. pulsed current (1)	—	100		
P_d	Power dissipation (rth = 62°C/W)	—	2	W	
ESD1	Electrostatic discharge voltage (Human Body)	—	tbd	kV	C = 100 pF, R = 1500Ω
ESD2	Electrostatic discharge voltage (Machine Model)	—	tbd		C = 200 pF, R = 0Ω, L=10μH
T_j max.	Max. storage & junction temp.	-40	150	°C	
Tlead	Lead temperature (soldering 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance free air	60	—	°C/W	
R_{th} 2	Thermal resistance with standard footprint	60	—		
R_{th} 3	Thermal resistance with 1" footprint	35	—		
R_{th} 4	Thermal resistance junction to case	0.7	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{CC} - V_{in}	Continuous input voltage	6	18	V
V_{CC}	Supply to power ground voltage	6	18	
I_{out}	Continuous output current (rth c/amb. < 5°C/W, Tj = 125°C)	—	35	A
I_{out} Tamb=85°C	Continuous output current (TAmbient = 85°C, Tj = 125°C, free air)	—	8	

(1) Limited by junction temperature. Pulsed current is also limited by wiring)

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ 1	ON state resistance	—	4.6	5.2	mΩ	I_{out}=35A,Vcc -Vin=12V see Fig. 6
$R_{ds(on)}$ 2	ON state resistance	—	4.6	—		I_{out}=17A, V_{cc} -V_{in}= 6V
$R_{ds(on)}$ 3	ON state resistance T_j = 150°C	—	7.4	—		I_{out} = 35A, T_j = 150°C
V_{clamp} 1	V_{cc} to V_{out} active clamp voltage	35	40	—	V	I_{out} = 10mA
V_{clamp} 2	V_{cc} to V_{out} active clamp voltage	—	42	48		I_{out} = 35A
V_{sd}	Body diode forward voltage	—	0.85	1		I_d = 35A, V_{cc} -V_{in} = 0V
$V_{cc\ (op)}$	Operating voltage range	5.5	—	28		
I_q	Quiescent current	—	13	50	µA	V_{cc}-V_{in}=0V,V_{cc}-V_{out}= 12V
I_{in}	Input current	3	6.5	12	mA	V_{cc} - V_{in} = 14V
$I_{in,\ on}$	Input current when ON	—	1.3	—		V_{cc} - V_{in} = V_{ih}
V_{ih}	High level input threshold voltage	—	4.75	5.5	V	(note 2)
V_{il}	Low level input threshold voltage	3	4.05	—		(note 2)
V_{hys}	Input hysterisis	0.4	0.6	1.5		

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 0.4Ω, T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Td_{on}	Turn-on delay time to V_{cc} -V_{out} = 0.9 V_{cc}	—	10	30	µs	See figure 2
T_r 1	Rise time to V_{cc} -V_{out} = 5 V	—	16	50		
T_r 2	Rise time from the end of Tr1 to Vcc -Vout = 0.1 Vcc	—	200	400		
dV/dt (on)	Turn on dV/dt	—	1.2	5	V/µs	
E_{on}	Turn ON energy	—	25	—	mJ	See figure 3
Td_{off}	Turn-off delay time V_{cc} -V_{out} = 0.1 V_{cc}	—	130	300	µs	
T_f	Fall time to V_{cc} -V_{out} = 0.9 V_{cc}	—	25	50		
dV/dt (off)	Turn OFF dV/dt	—	2	6	V/µs	
E_{off}	Turn OFF energy	—	6	—	mJ	

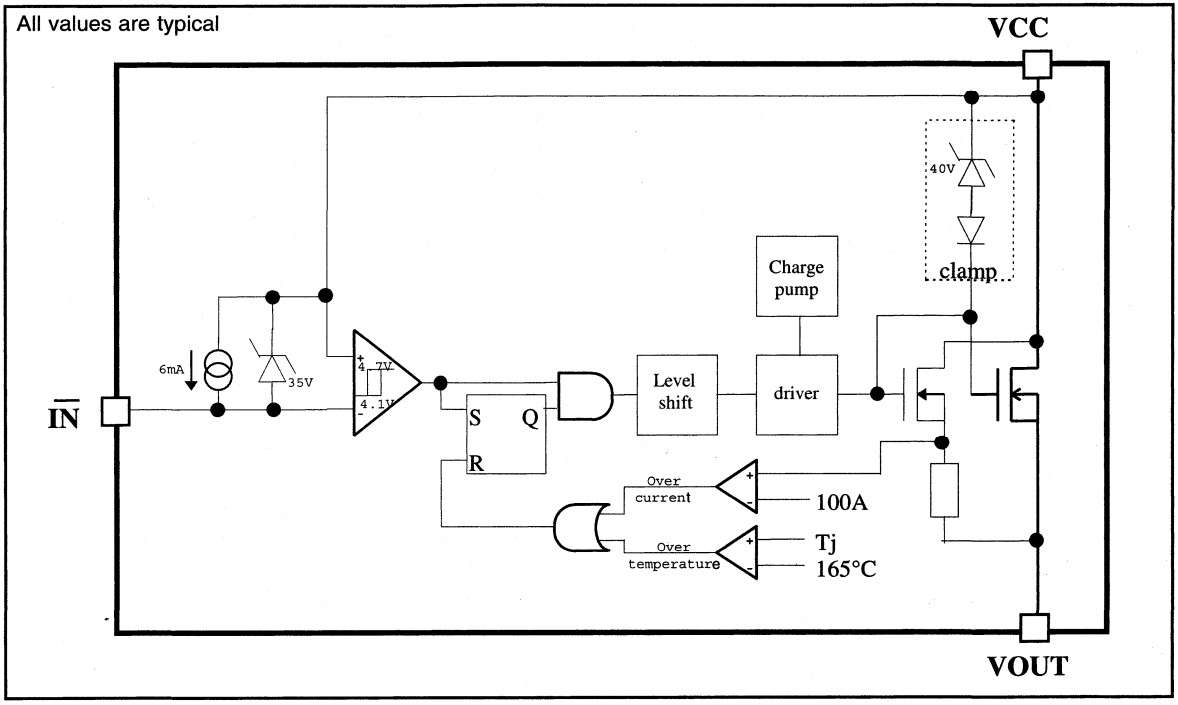
Protection Characteristics

T_j = 25°C, (unless otherwise specified).

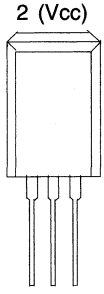
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature shutdown threshold	—	165	—	°C	See fig. 4
I_{sc}	Over current shutdown threshold	70	100	130	A	
T_{reset}	Minimum time for protection reset	—	50	—	µs	

(2) Input threshold are measured directly between the the input pin and the tab. Any parasitic resistance in common between the load current path and the input signal path can significantly affect the thresholds.

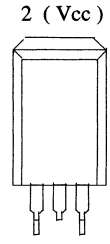
Functional Block Diagram



Lead Assignments



SuperTO220



SuperSMD220

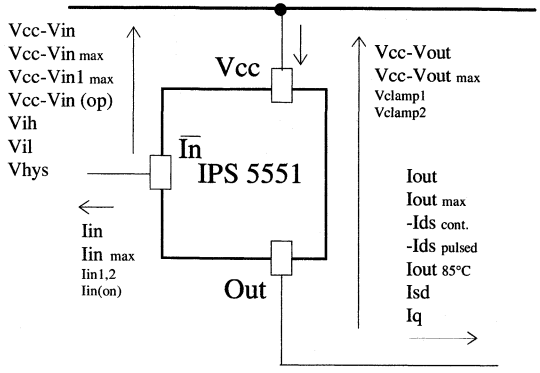


Figure 1 - Voltages and currents definition

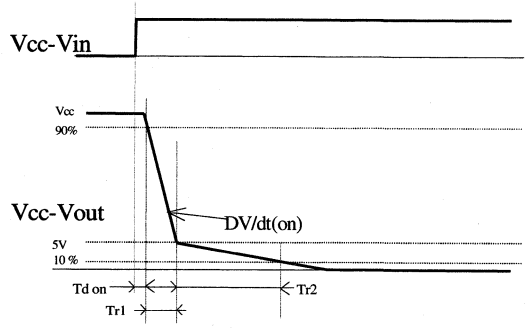


Figure 2 - Switching time definitions (turn-on)

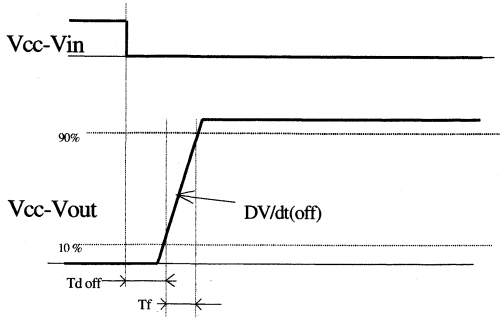


Figure 3 - Switching time definitions (turn-off)

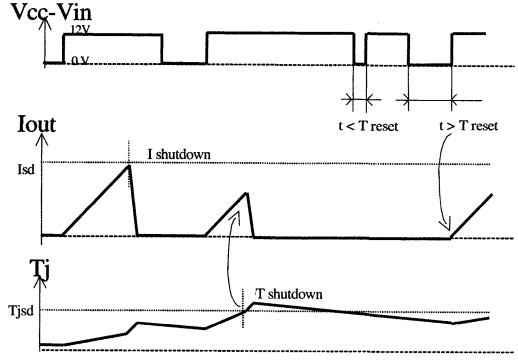


Figure 4 - Protection timing diagram

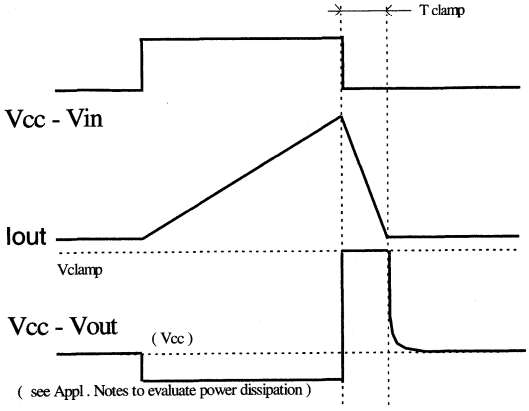


Figure 5 - Active clamp waveforms

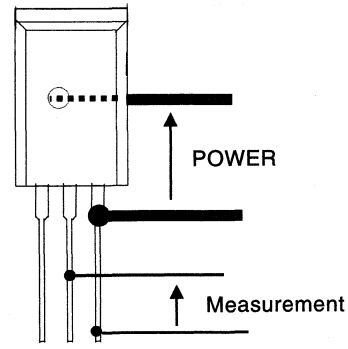


Figure 6 - Rds(on) measurement schematic

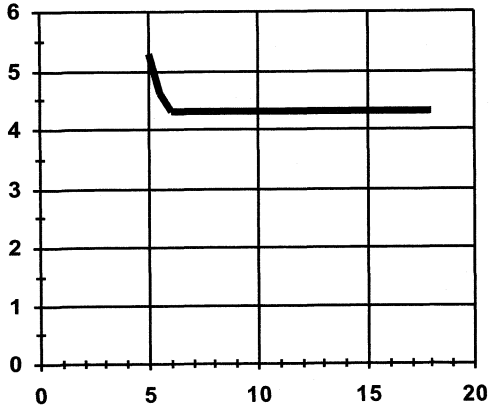


Figure 7 - $Rds_{(on)}$ (mΩ) Vs V_{cc}-V_{in} (V)

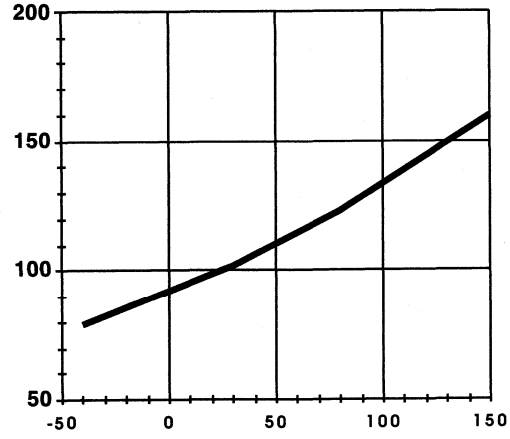


Figure 8 - Normalized $Rds_{(on)}$ (%) Vs T_j (°C)

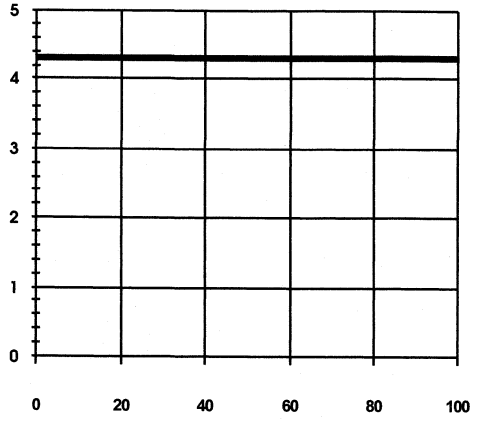


Figure 9 - $Rds_{(on)}$ (mΩ) Vs I_{out} (A)

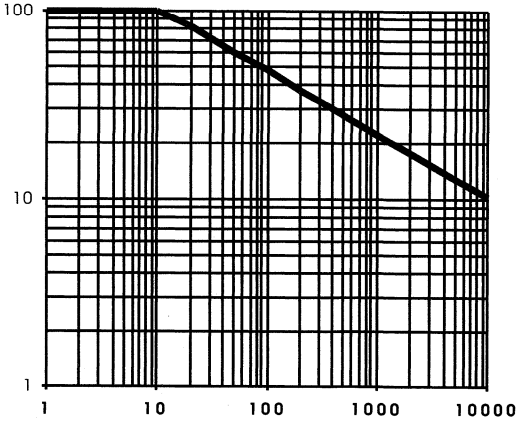


Figure 10 - Max Iout (A) Vs Load Inductance (μH)

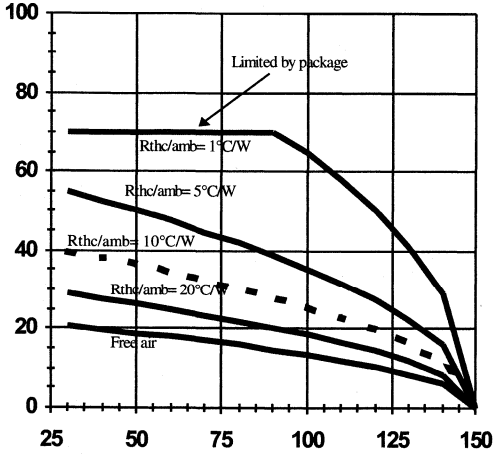


Figure 11 - Max. load current (A) Vs Temperature (°C)

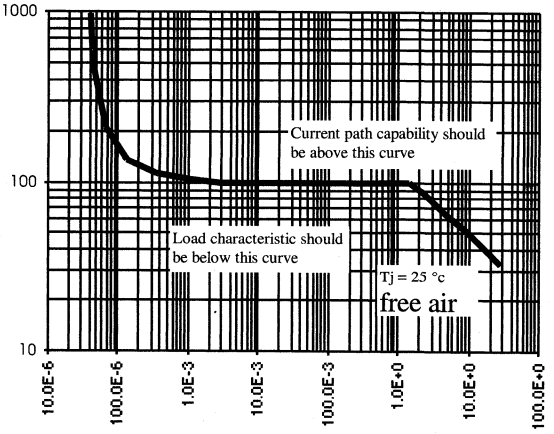


Figure 12 - I_{out} (A) Vs Protection resp. Time (ms)

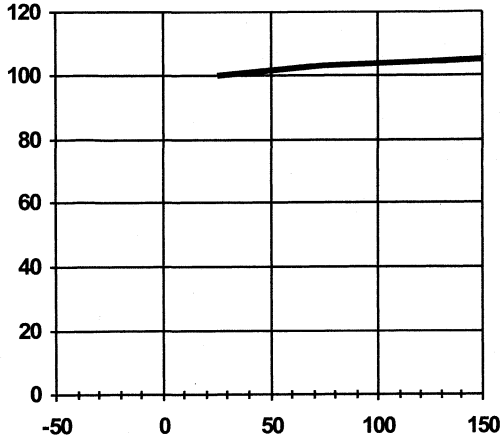


Figure 13 - I_{sd} (A) Vs T_j (°C)

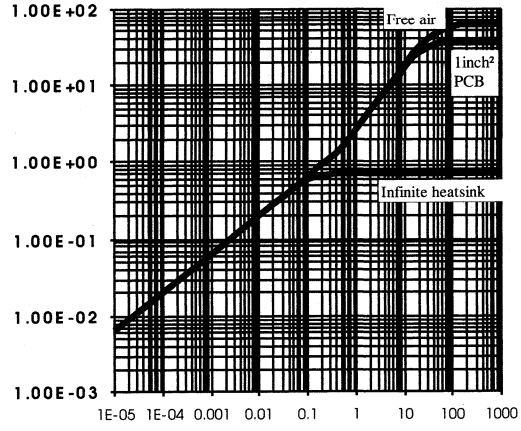


Figure 14 - Transient thermal impedance (°C/W) Vs Time (S)

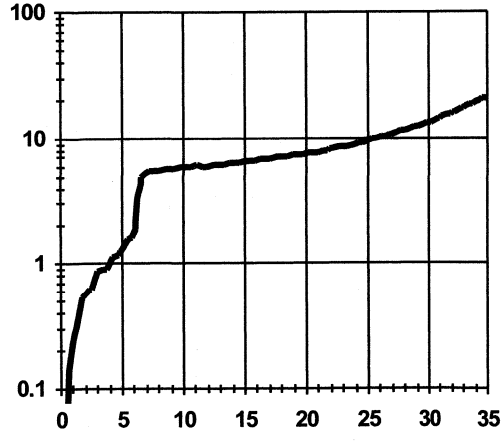


Figure 15 - I_{cc} (mA) Vs V_{cc}-V_{in} (V)

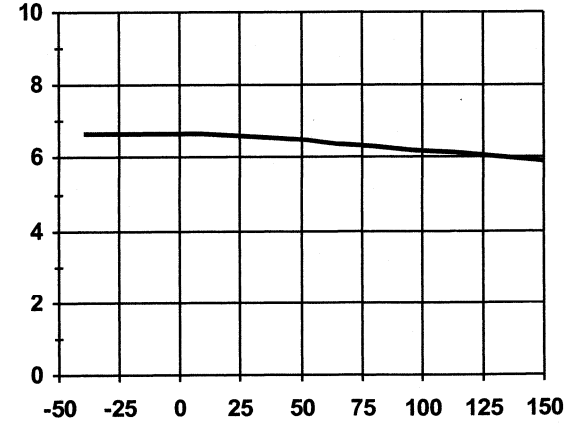


Figure 16 - I_{in} (µA) Vs T_j (°C)

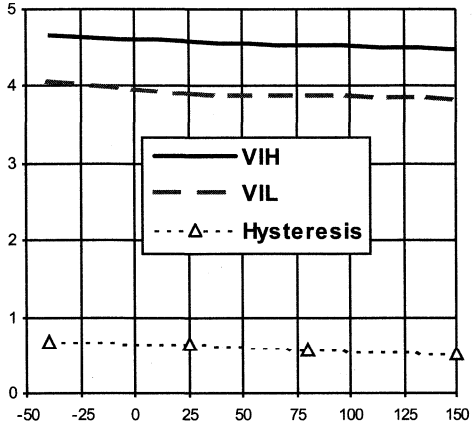


Figure 17 - V_{ih}, V_{il} threshold (V) Vs Tj (°C)

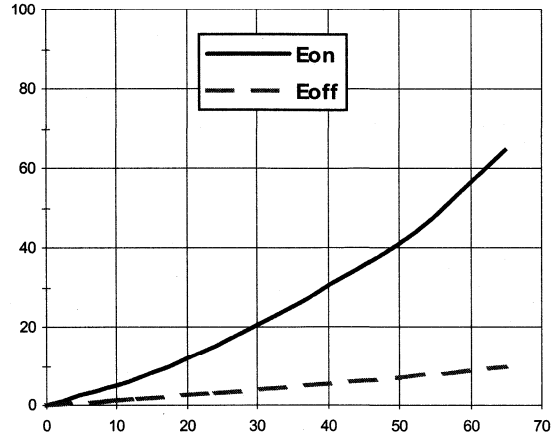


Figure 18 - E_{on}, E_{off} (mJ) Vs I_{out} (A)

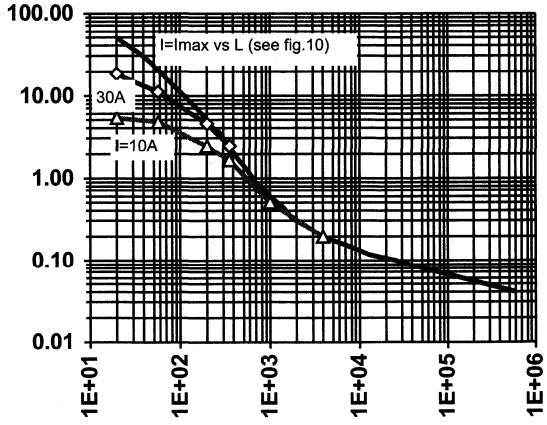
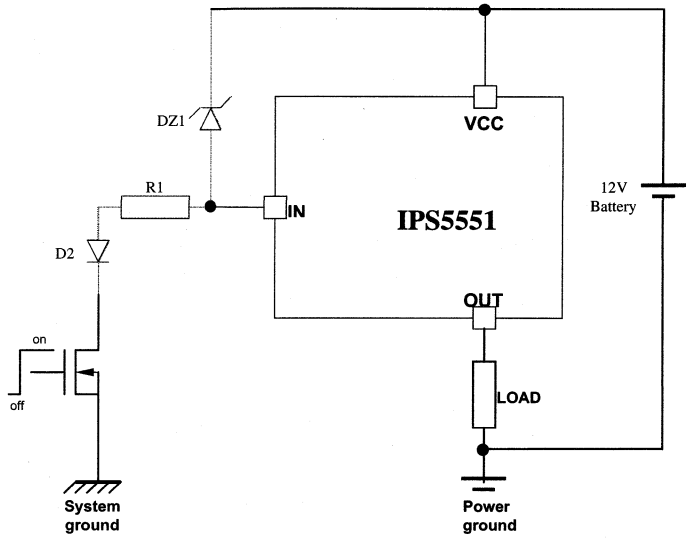


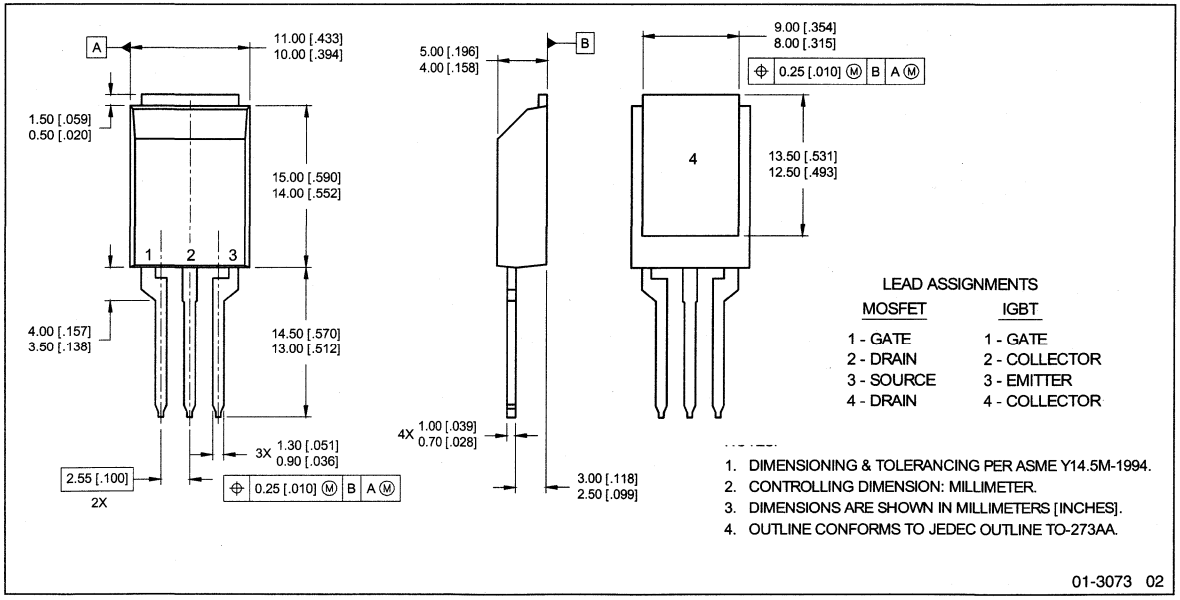
Figure 19 - E_{on} (mJ) Vs Inductive load (µH)
(Vcc = 14V, R load =0.5Ω)



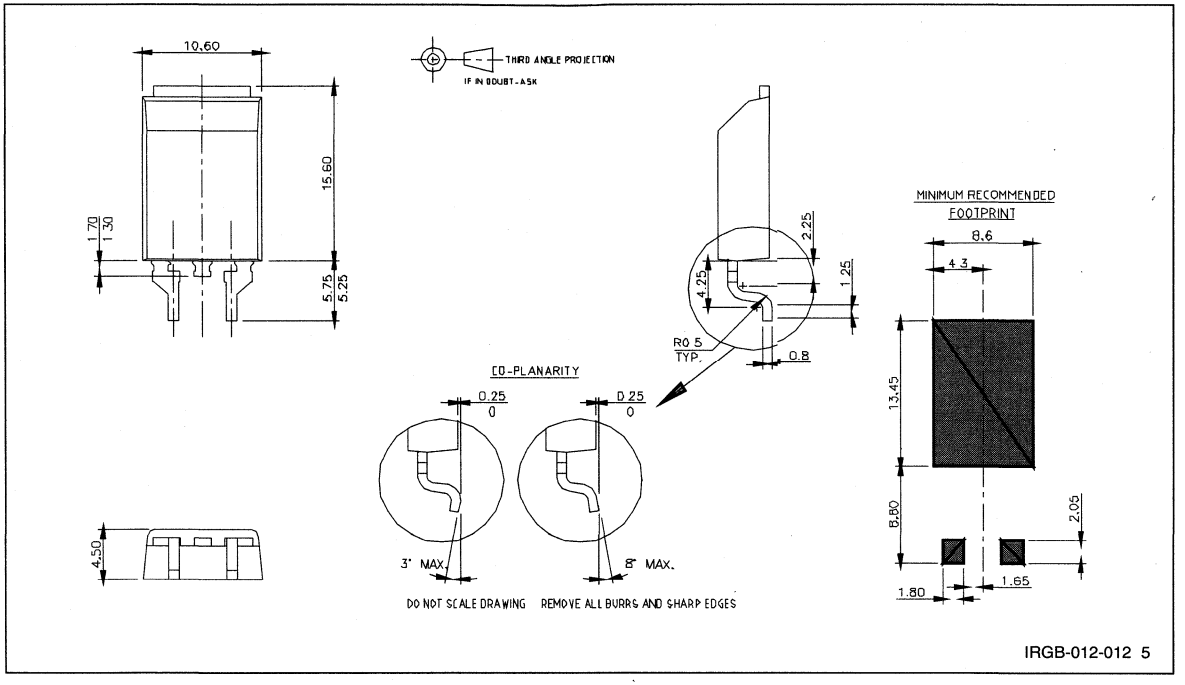
DZ1, R1 : optional additional voltage transient protection
D2 : optional additional reverse battery protection
See application note for details

Figure 20 - Automotive typical connection

Case outline Super TO220



Case outline Super SMD220 (advance information)



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

Data Sheet No. PD 60068-I

IRSF3021 (NOTE: For new designs, we recommend IR's new products IPS021 and IPS021L)

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Controlled slew rate reduces EMI
- Over temperature protection with auto-restart
- Linear current-limit protection
- Active drain-to-source clamp
- ESD protection
- Lead compatible with standard Power MOSFET
- Low operating input current
- Monolithic construction

Product Summary

$V_{ds(clamp)}$	50V
$R_{ds(on)}$	200mΩ
I_{lim}	5.5A
$T_{j(sd)}$	165°C
E_{AS}	200mJ

Description

The IRSF3021 Lamp and DC motor driver is a fully protected three terminal monolithic Smart Power MOSFET that features current limiting, over-temperature protection, ESD protection and over-voltage protection.

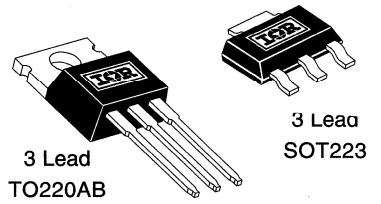
The on-chip protection circuit limits the drain current at 5.5A (typical) in the on-state, when the load is short circuited. The over-temperature circuitry turns off the Power MOSFET when the junction temperature exceeds 165°C (typical). The device restarts automatically once it has cooled down below the reset temperature.

The IRSF3021 is specifically designed for driving loads that require overload protection and in-rush current control while operating in automotive and industrial environments. Targeted applications include resistive loads such as lamps or capacitive loads such as airbag squibs and DC motor drives.

Applications

- Cabin Lighting
- Airbag System
- Programmable Logic Controller
- DC Motor Drive

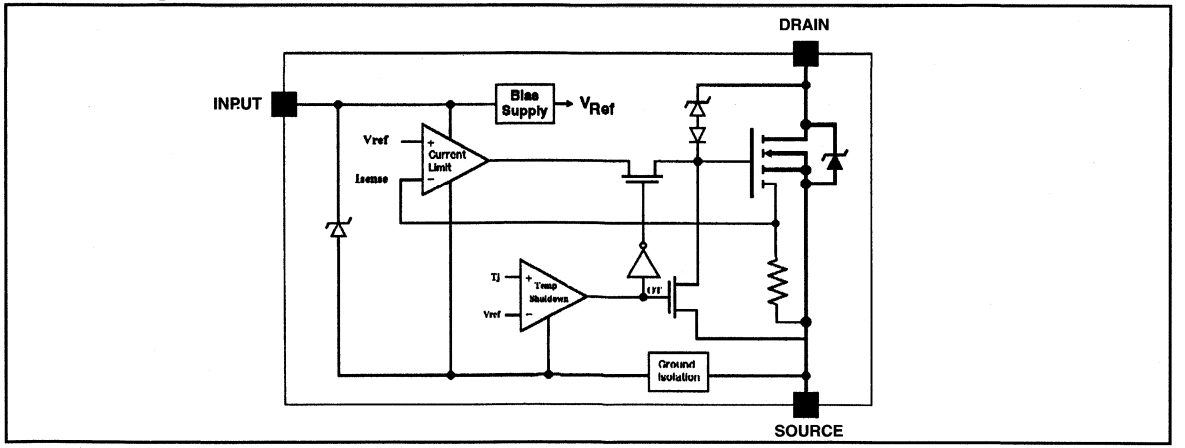
Packages



3 Lead TO220AB

3 Lead SOT223

Block Diagram



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. (T_C = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
$V_{ds,\ max}$	Continuous drain to source voltage	—	50	V	
$V_{in,\ max}$	Continuous input voltage	-0.3	10		
I_{ds}	Continuous drain current	—	self limited	A	
P_d	Power dissipation	—	30	W	$T_C \leq 25°C$, TO220
		—	3	W	$T_C \leq 25°C$, SOT223
EAS	Unclamped single pulse inductive energy②	—	200	mJ	
V_{esd1}	Electrostatic discharge voltage (Human Body Model)	—	4000	V	100pF, 1.5kΩ
V_{esd2}	Electrostatic discharge voltage (Machine Model)	—	1000		200pF, 0Ω
T_{Jop}	Operating junction temperature range	-55	150	°C	
T_{Stg}	Storage temperature range	-55	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

Static Electrical Characteristics

(T_C = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{ds,clamp}$	Drain to source clamp voltage	50	56	65	V	I_{ds} = 6A, t_p = 700 µS
$R_{ds(on)}$	Drain to source on resistance	—	155	200	mΩ	V_{in} = 5V, I_{ds} = 2A
I_{dss}	Drain to source leakage current	—	—	250	µA	V_{ds} = 40V, V_{in} = 0V
V_{th}	Input threshold voltage	1.0	2.0	3.0	V	V_{ds}= V_{in}, I_{ds}+ I_{in}= 10mA
$I_{i,on}$	Input supply current (Normal Operation)	—	100	300	µA	V_{in} = 5V
$I_{i,off}$	Input supply current (Protection Mode)	—	250	500	µA	V_{in} = 5V
$V_{in,\ clamp}$	Input clamp voltage	9	10	—	V	I_{in} = 1mA
V_{sd}	Body-drain diode forward drop③	—	1.5	—		I_{ds} = -2A, R_{in} = 1kΩ

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{thjc}	Junction to case	—	—	4	°C/W	TO-220AB
R_{thja}	Junction to ambient	—	—	60		
R_{thjc}	Junction to case	—	—	40	°C/W	SOT-223
R_{thja}	Junction to PCB ①	—	—	60		

NOTES:

① When mounted on a 1" square PCB (FR-4 or G10 material). For recommended footprint and soldering techniques, refer to International Rectifier Application Note AN-994.

② E_{AS} is tested with a constant current source of 6A applied for 700µS with V_{in} = 0V and starting T_j = 25°C.

③ Input current must be limited to less than 5mA with a 1kΩ resistor in series with the input when the Body-Drain Diode is forward biased.

Switching ElectricalCharacteristics

(V_{CC} = 14V, resistive load (R_L) = 10Ω, R_{in}= 100Ω. Specifications measured at T_C= 25°C unless otherwise specified.)

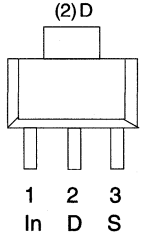
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_{don}	Turn-on delay time	—	10	50	µs	V_{in}= 0V to 5V, 50% to 90%
t_r	Rise Time	—	30	80		V_{in}= 0V to 5V, 90% to 10%
t_{doff}	Turn-off delay time	—	20	60		V_{in}= 5V to 0V, 50% to 10%
t_f	Fall time	—	15	50		V_{in}= 5V to 0V, 10% to 90%
SR	Output positive slew rate	-4	—	4	V/µs	V_{in}= 0V to 5V, +dVds/dt
SR	Output negative slew rate	-4	—	4		V_{in}= 5V to 0V, -dVds/dt

Protection Characteristics

(T_C= 25°C unless otherwise specified.

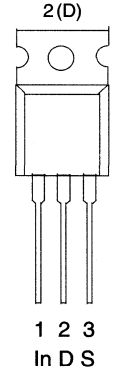
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_{ds(lim)}$	Current limit	3.0	5.5	8.0	A	V_{in} = 5V, V_{ds} = 14V
$T_{j(sd)}$	Over temperature shutdown threshold	155	165	—	°C	V_{in} = 5V, I_{ds} = 2A
$V_{protect}$	Min. input voltage for over-temp function	—	3	—	V	
t_{Iresp}	Current limit response time	—	TBD	—	µs	
I_{peak}	Peak short circuit current	—	10	—	A	
t_{Tresp}	Over-temperature response time	—	TBD	—	µs	

Lead Assignments



3 Lead - SOT223

IRSF3021L

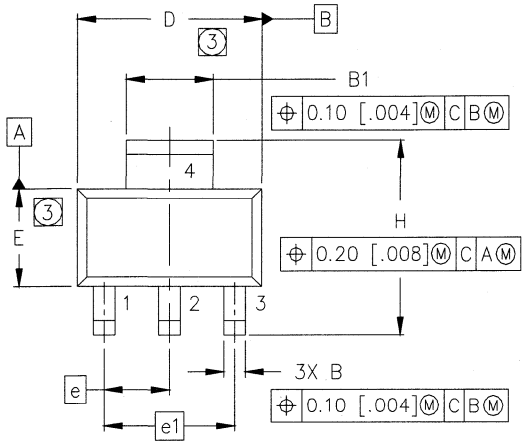


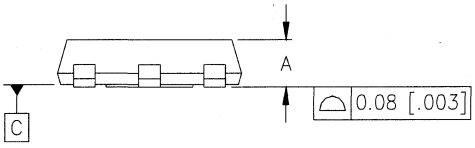
3 Lead - TO220

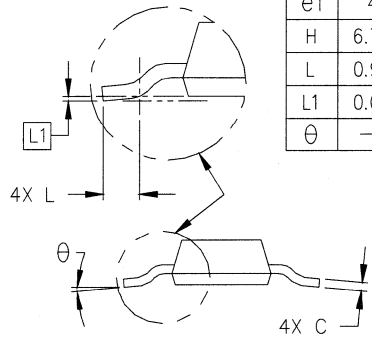
IRSF3021

Part Number

Case Outline - SOT-223

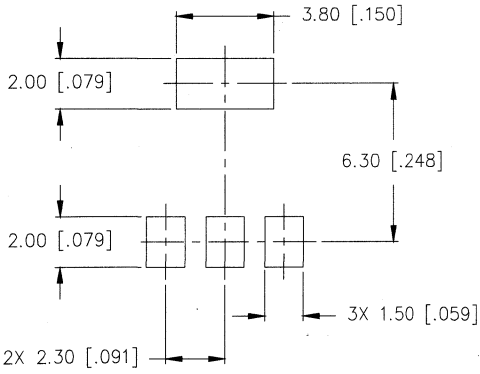






DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.55	1.80	.061	.071
B	0.65	0.85	.026	.033
B1	2.95	3.15	.116	.124
C	0.25	0.35	.010	.014
D	6.30	6.70	.248	.264
E	3.30	3.70	.130	.146
e	2.30	BSC	.0905	BSC
e1	4.60	BSC	.181	BSC
H	6.71	7.29	.264	.287
L	0.91	—	.036	—
L1	0.061	BSC	.0024	BSC
θ	—	10°	—	10°

MINIMUM RECOMMENDED FOOTPRINT



LEAD ASSIGNMENTS

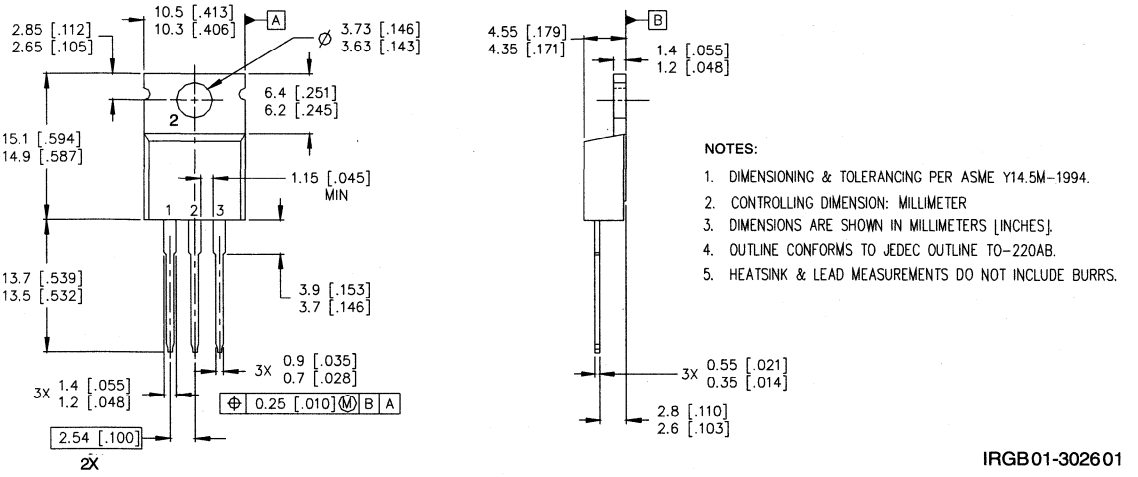
1 – GATE
2 = DRAIN
3 = SOURCE

NOTES:

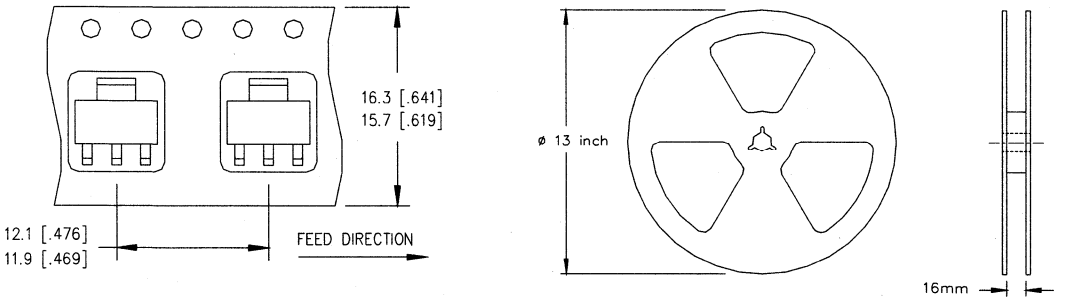
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

(TO-261AA) 01-0022 05

Case Outline 3 Lead - TO220



Tape & Reel - SOT223



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 81 (0) 33 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon, Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

Data Sheet No. PD 60069-H

IRSF3031 (NOTE: For new designs, we recommend IR's new products IPS021 and IPS021L)

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Controlled slew rate reduces EMI
- Over temperature protection
- Over current protection
- Active drain-to-source clamp
- ESD protection
- Lead compatible with standard Power MOSFET
- Low operating input current
- Monolithic construction
- Dual set/reset threshold input

Product Summary

Vds(clamp)	50 V
Rds(on)	200 mΩ
Ids(sd)	4 A
Tj(sd)	165°C
EAS	200 mJ

Description

The IRSF3031 is a three-terminal monolithic Smart Power MOSFET with built-in short circuit, over-temperature, ESD and over-voltage protections and dual set/reset input threshold .

The on-chip protection circuit latches off the Power MOSFET in case the drain current exceeds 4A (typical) or the junction temperature exceeds 165°C (typical) and keeps it off until the input is driven below the Reset Threshold voltage.

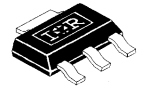
The drain to source voltage is actively clamped at 55V prior to the avalanche of the Power MOSFET, thus improving its performance during turn-off with inductive loads.

The input requirements are very low (100µA typical) which makes the IRSF3031 compatible with most existing designs based on standard power MOSFETs.

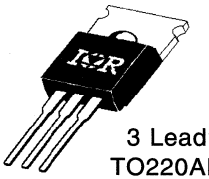
Applications

- Solenoid Driver
- DC Motor Driver
- Programmable Logic Controller

Packages

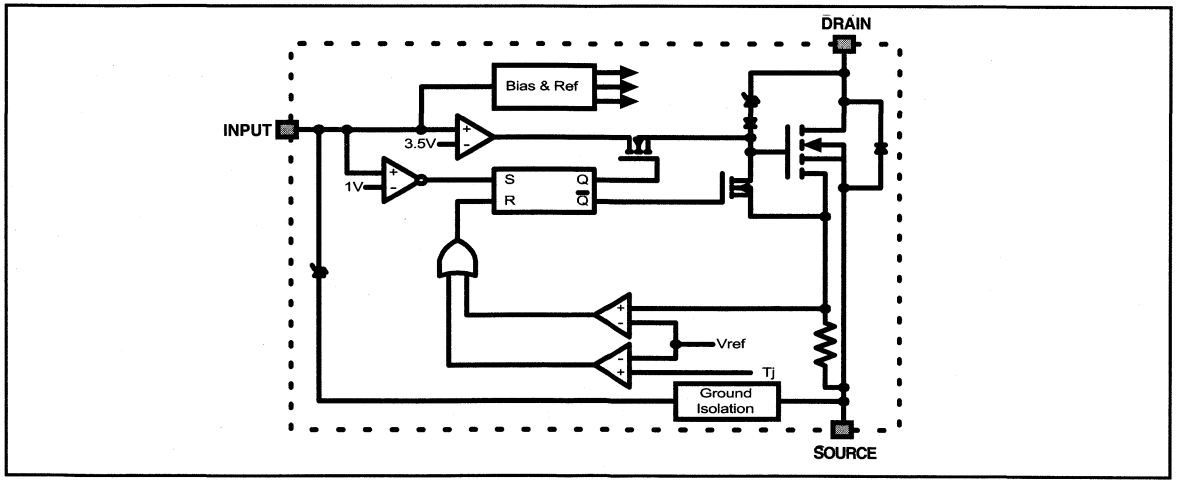


3 Lead
SOT-223



3 Lead
TO220AB

Block Diagram



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. (T_c = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
$V_{ds,\ max}$	Continuous drain to source voltage	—	50	V	
$V_{in,\ max}$	Continuous input voltage	-0.3	10		
I_{ds}	Continuous drain current	—	self limited	A	
P_d	Power dissipation	—	30	W	$T_C \leq 25°C$, TO220
		—	3.0	W	$T_C \leq 25°C$, SOT223
EAS	Unclamped single pulse inductive energy②	—	200	mJ	
V_{esd1}	Electrostatic discharge voltage (Human Body Model)	—	4000	V	100pF. 1.5kΩ
V_{esd2}	Electrostatic discharge voltage (Machine Model)	—	1000		200pF, 0Ω
T_{Jop}	Operating junction temperature range	-55	150	°C	
T_{Stg}	Storage temperature range	-55	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

Static Electrical Characteristics

(T_c = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{ds,clamp}$	Drain to source clamp voltage	50	56	65	V	I_{ds} = 2A
$R_{ds(on)}$	Drain to source on resistance	—	155	200	mΩ	V_{in} = 5V, I_{ds} = 2A
I_{dss}	Drain to source leakage current	—	—	250	μA	V_{ds} = 40V, V_{in} = 0V
V_{set}	Input threshold voltage	2.5	3.2	4.0	V	V_{ds} = 5V, I_{ds} > 10mA
V_{reset}	Input protection reset threshold voltage	0.5	1.0	1.5	V	V_{ds} = 5V, I_{ds} < 10μA
$I_{i,on}$	Input supply current (normal operation)	—	100	300	μA	V_{in} = 5V
$I_{i,off}$	Input supply current (protection mode)	—	120	400	μA	V_{in} = 5V
$V_{in,\ clamp}$	Input clamp voltage	9	10	—	V	I_{in} = 1mA
V_{sd}	Body-drain diode forward drop③	—	1.5	—	V	I_{ds} = -2A, R_{in} = 1kΩ

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{thjc}	Thermal resistance, junction-to-case	—	—	4	°C/W	TO-220AB
R_{thja}	Thermal resistance, junction-to-ambient	—	—	60		
R_{thjc}	Thermal resistance, junction-to-case	—	—	40	°C/W	SOT-223
R_{thja}	Thermal resistance, junction-to-PCB ①	—	—	60		

NOTES:

① When mounted on a 1" square PCB (FR-4 or G10 material). For recommended footprint and soldering techniques, refer to International Rectifier Application Note AN-994.

② E_{AS} is tested with a constant current source of 6A applied for 700μS with V_{in} = 0V and starting T_j = 25°C.

③ Input current must be limited to less than 5mA with a 1kΩ resistor in series with the input when the Body-Drain Diode is forward biased.

Switching ElectricalCharacteristics

(V_{CC} = 14V, resistive load (R_L) = 10Ω, R_{in}= 100Ω. Specifications measured at T_C= 25°C unless otherwise specified.)

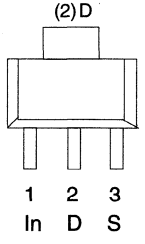
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_{don}	Turn-on delay time	—	—	30	µs	V_{in} = 2V to 5V, 50% to 90%
t_r	Rise time	—	—	30		V_{in} = 2V to 5V, 90% to 10%
tdoff	Turn-off delay time	—	—	30		V_{in} = 5V to 2V, 50% to 10%
t_r	Fall time	—	—	30		V_{in} = 5V to 2V, 10% to 90%
SR	Output positive slew rate	-6	—	6	V/µs	V_{in} = 2V to 5V, +dVds/dt
SR	Output negative slew rate	-6	—	6		V_{in} = 5V to 2V, -dVds/dt

Protection Characteristics

T_C= 25°C unless otherwise specified.

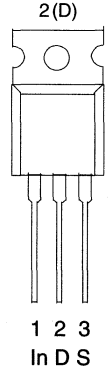
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_{ds(sd)}$	Current limit	1.8	4	6	A	Vin = 5V
$T_{j(sd)}$	Over temperature shutdown threshold	155	165	—	°C	Vin = 5V, Ids = 2A
$V_{protect}$	Min. input voltage for over-temp function	—	3	—	V	
tIresp	Over current response time	—	TBD	—	µs	
I_{peak}	Peak short circuit current	—	TBD	—	A	
t_{reset}	Protection reset time	—	TBD	—	µs	
tTresp	Over-temperature response time	—	TBD	—		

Lead Assignments



3 Lead - SOT223

IRSF3031L

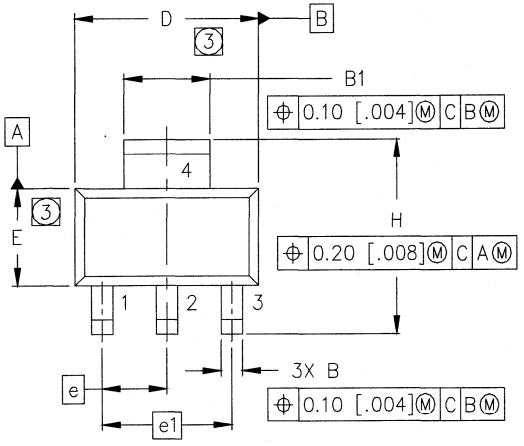


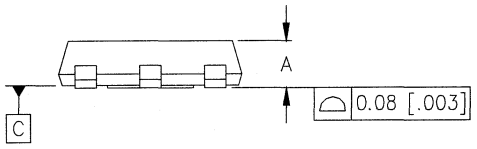
3 Lead - TO220

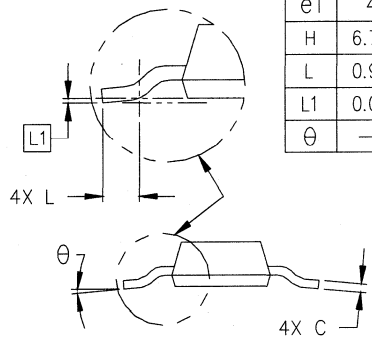
IRSF3031

Part Number

Case Outline - SOT-223

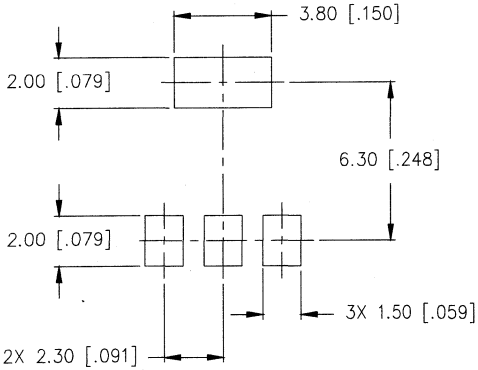






DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.55	1.80	.061	.071
B	0.65	0.85	.026	.033
B1	2.95	3.15	.116	.124
C	0.25	0.35	.010	.014
D	6.30	6.70	.248	.264
E	3.30	3.70	.130	.146
e	2.30 BSC		.0905 BSC	
e1	4.60 BSC		.181 BSC	
H	6.71	7.29	.264	.287
L	0.91	—	.036	—
L1	0.061 BSC		.0024 BSC	
θ	—	10°	—	10°

MINIMUM RECOMMENDED FOOTPRINT



LEAD ASSIGNMENTS

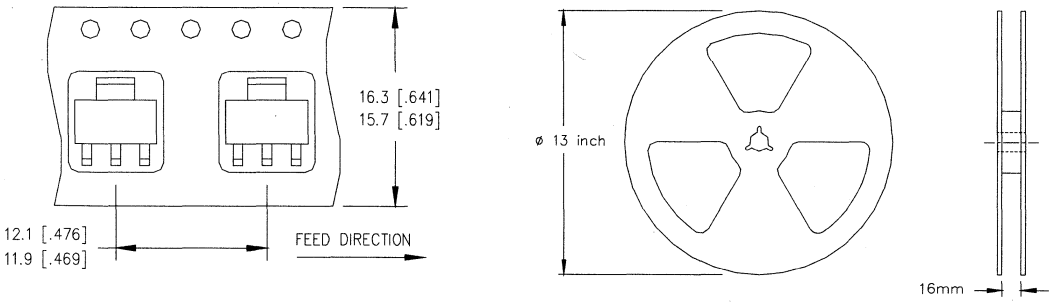
1 = GATE
2 = DRAIN
3 = SOURCE

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

(TO-261AA) 01-0022 05

Tape & Reel - SOT223

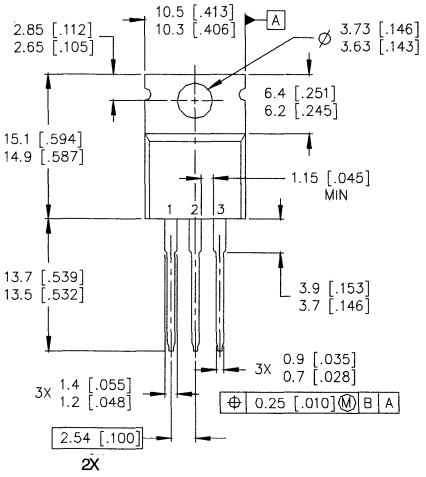


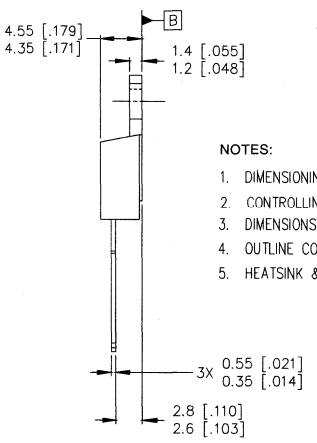
NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.
4. EACH ø 330.00 [ø 13.00] REEL CONTAINS 2,500 DEVICES.

01-0028 05 / 01-0008 02

Case Outline 3 Lead - TO220





NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
5. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

IRGB 01-3026 01

International
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IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon,
Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

IR6210 (NOTE: For new designs, we recommend IR's new products IPS511 and IPS511S)

INTELLIGENT HIGH SIDE MOSFET POWER SWITCH

Features

- PWM current limit for short circuit protection
- Over-temperature protection
- Active output negative clamp
- Reverse battery protection for logic circuit
- Broken ground protection
- Short to V_{CC} protection
- Low noise charge pump
- Sleep mode supply current
- 4kV ESD protection on all leads
- Logic ground isolated from power ground

General Description

The IR6210 is a 5 terminal monolithic high side switch with built in short circuit, over- temperature, ESD protections, inductive load turn off capability and diagnostic feedback.

The on-chip protection circuit goes into PWM mode, limiting the average current during short circuit if the drain current exceeds 5A. The protection circuit latches off the high side switch if the junction temperature exceeds 170°C and latches on after the junction temperature falls by 10°C. The Vcc (drain) to out (source) voltage is actively clamped at 55V, improving its performance during turn off with inductive loads.

The on-chip charge pump high side driver stage is floating and referenced to the source of the Power MOSFET. Thus the logic to power ground isolation can be as high as 50V. This allows operation with larger offset as well as controlling the switch during load energy recirculation or regeneration.

A diagnostic pin is provided for status feedback of short circuit, over temperature and open load detection.

Product summary

$V_{cc(op)}$	5-50V
$R_{DS(on)}$	200mΩ
I_{lim}	5A
$T_{j(sd)}$	170°C
E_{av}	100mJ

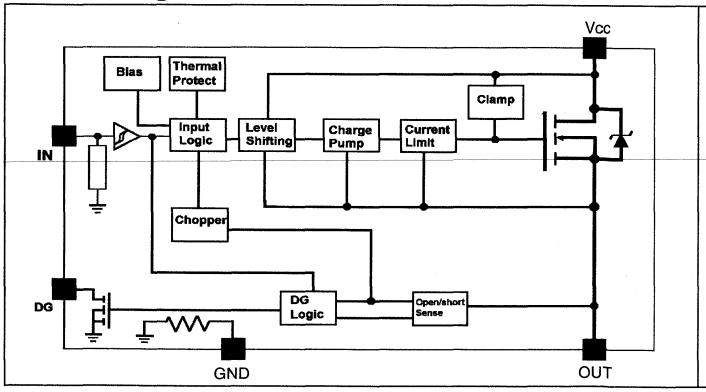
Applications

- Solenoid driver
- Programmable logic controller

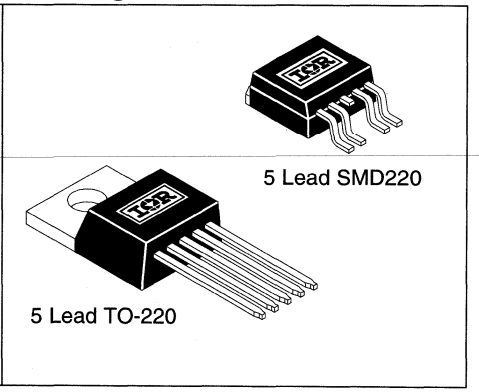
Truth Table

Condition	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Output Open	H	H	H
Output Open	L	H	H
Shorted Output	H	Current-Limiting PWM Mode	L
Shorted Output	L	L	L
Over-Temperature	H	L	L
Over-Temperature	L	L	L

Block Diagram



Packages



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (T_C = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{cc}	Supply voltage permanent	-0.3	50	V	
	reverse	-16	—		For 10 seconds, (1)
V_{offset}	Logic to power ground offset	Vcc -50	Vcc +0.3		
V_{in}	Input voltage	-0.3	30		
I_{in}	Input current	—	10	mA	
V_{out}	Output voltage	Vcc -50	Vcc +0.3	V	
I_{out}	Output current	—	self-limited	A	
V_{dg}	Diagnostic output voltage	-0.3	30	V	
I_{dg}	Diagnostic output current	—	10	mA	
E_{av}	Repetitive avalanche energy	—	100	mJ	I = 2A (2)
ESD1	Electrostatic discharge (Human Body Model)	—	4000	V	C = 100 pF,R = 1500Ω
ESD2	Electrostatic discharge (Machine Model)	—	1000	V	C = 200 pF, R = 0Ω
PD	Power dissipation	—	28	W	Tcase= 25°C
T_{Jop}	Operating junction temperature range	-40	150	°C	
T_{Stg}	Storage temperature range	-40	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

NOTES: (1) with 15kΩ resistors in input and diagnostic

(2) maximum frequency depends on heatsink (rectangular waveform)

Static Electrical Characteristics

(T_C= 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ccop}	Operating voltage range	5	—	35	V	
I_{ccoff}	Sleep mode supply current	—	40	—	µA	V_{cc}=24V, V_{in}= 0V
I_{ccon}	Supply current (average)	—	3	—	mA	V_{in} = 5V
I_{ccac}	Supply current (AC RMS)	—	20	—	µA	V_{in} = 5V
V_{ih}	High level input threshold voltage	—	2	2.5	V	
V_{il}	Low level input threshold voltage	1	1.8	—		
I_{ion}	On-state input current	10	—	70	µA	V_{in} = 3.5V
I_{ioff}	Off-state input current	1	—	30		V_{in} = 0.4V
I_{oh}	Output leakage current	—	20	—		V_{out} = 6V
I_{ol}	Output leakage current	0	—	10		V_{out} = 0V
V_{dgl}	Low level diagnostic output voltage	—	0.3	—	V	I_{dg} = 1.6mA
I_{dgh}	Diagnostic output leakage current	0	—	10	µA	V_{dg} = 5V
$R_{DS(on)}$	On-state resistance	—	150	200	mΩ	I_{out} = 1A
		—	200	—		V_{cc} = 5V, I_{out} = 1A

Switching Electrical Characteristics

(V_{CC} = 14V, resistive load (R_L) = 12Ω, T_C= 25°C.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_c	Over-current cycle time	—	5	—	ms	
D_c	Over-current duty cycle	—	10	—	%	
t_{on}	Turn-on delay time to 90%	—	50	—	µs	
t_{off}	Turn-off delay time to 10%	—	60	—		
dv/dt_{on}	Slew rate on	—	3	—	V/µs	
dv/dt_{off}	Slew rate off	—	5	—		

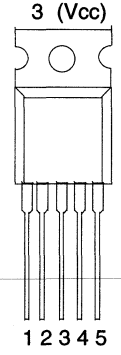
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	—	5	—	A	
V_{sc}	Short circuit detection voltage	—	3.5	—	V	
V_{slh}	Open load detection voltage	—	3.5	—		
V_{cl1}	Output negative clamp	50	54	—		I_{out} = 10mA
V_{cl2}	Output negative clamp	—	56	62		I_{out} = 2A

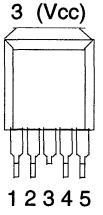
Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{jsd}	Thermal shutdown temperature	—	170	—	°C	
T_{hys}	Thermal hysteresis	—	10	—		
R_{thjc}	Thermal resistance,junction to case	—	3.5	—	°C/W	
R_{thja}	Thermal resistance, junction to ambient	—	50	—		

Lead Assignments



1 - Ground
2 - In
3 - Vcc
4 - DG
5 - Out

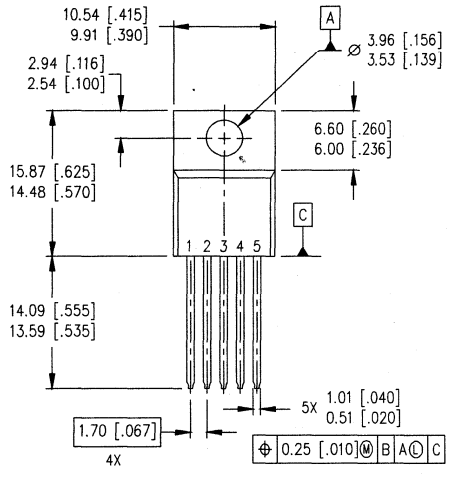


5 Lead - TO-220

5 Lead - D²PAK (SMD220)

IR6210	IR6210S
Part Number	

Case Outline 5 Lead - TO-220

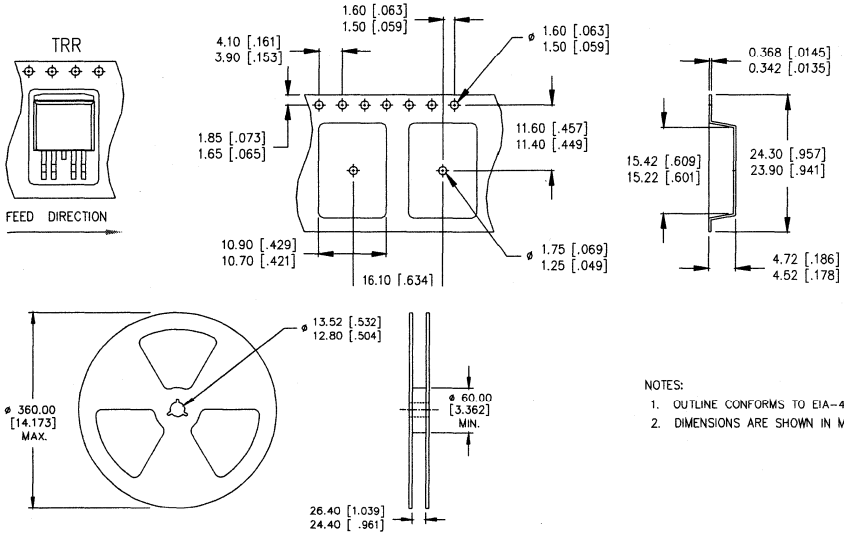


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TS-001.

IRGB 01-3042 01

Tape & Reel 5 Lead - D²PAK (SMD220)

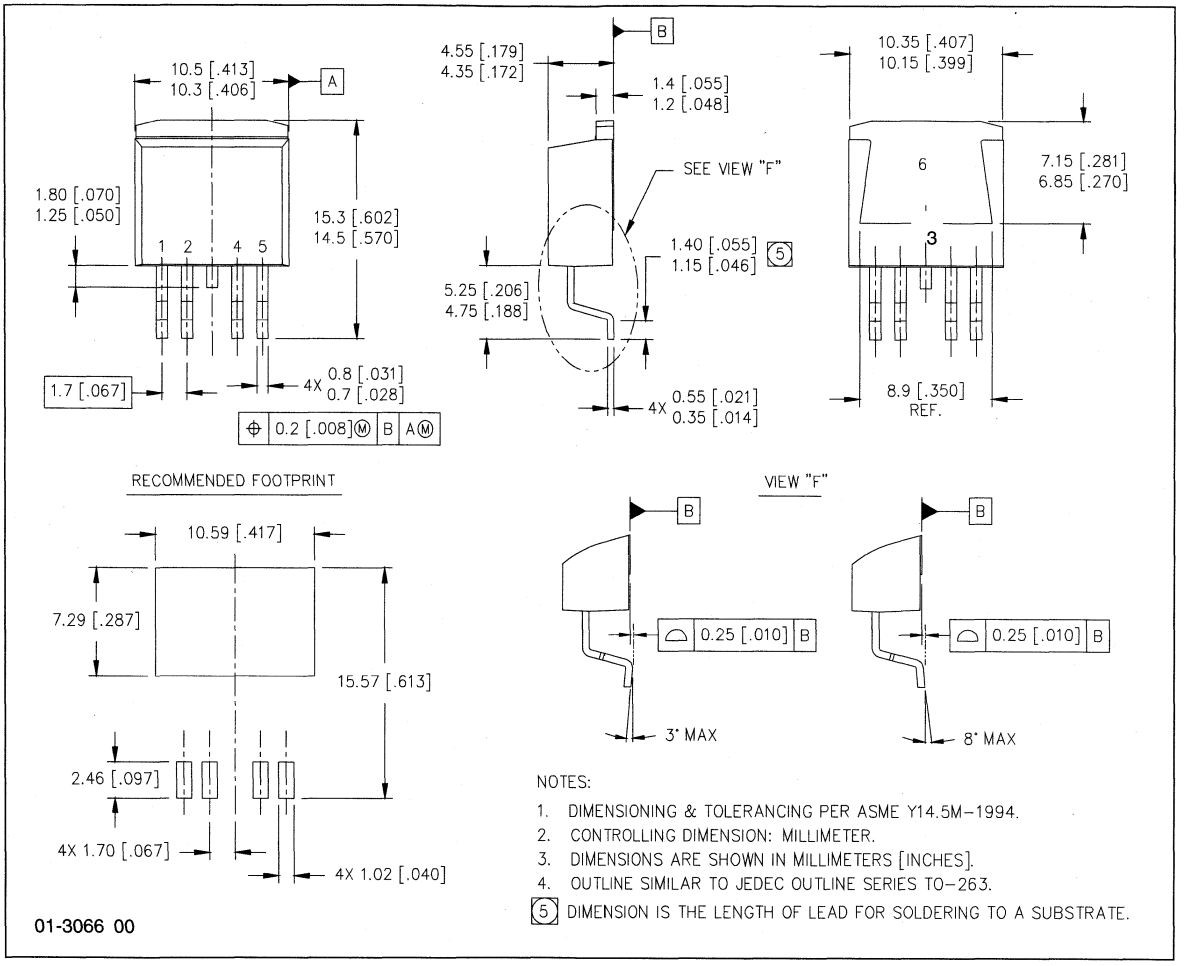


NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

01-3071 00 / 01-3072 00

Case Outline 5 Lead - SMD220 (D^2PAK)



01-3066 00

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO–263.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

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Tel: ++44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 81 (0) 33 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon, Hong Kong Tel: (852) 2803-7380

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IR6220 (NOTE: For new designs, we recommend IR's new products IPS521 and IPS521S)

INTELLIGENT HIGH SIDE MOSFET POWER SWITCH

Features

- PWM current limit for short circuit protection
- Over-temperature protection
- Active output negative clamp
- Reverse battery protection for logic circuit
- Broken ground protection
- Short to V_{CC} protection
- Low noise charge pump
- Sleep mode supply current
- 4kV ESD protection on all leads
- Logic ground isolated from power ground

Product summary

$V_{cc(op)}$	5-50V
$R_{DS(on)}$	100mΩ
I_{lim}	10A
$T_{j(sd)}$	170°C
E_{av}	200mJ

General Description

The IR6220 is a 5 terminal monolithic HIGH SIDE SWITCH with built in short circuit, over- temperature, ESD protections, inductive load turn off capability and diagnostic feedback. The on-chip protection circuit goes into PWM mode, limiting the average current during short circuit if the drain current exceeds 10A. The protection circuit latches off the high side switch if the junction temperature exceeds 170°C and latches on after the junction temperature falls by 10°C. The Vcc (drain) to out (source) voltage is actively clamped at 55V, improving its performance during turn off with inductive loads.

The on-chip charge pump high side driver stage is floating and referenced to the source of the Power MOSFET. Thus the logic to power ground isolation can be as high as 50V. This allows operation with larger offset as well as controlling the switch during load energy recirculation or regeneration.

A diagnostic pin is provided for status feedback of short circuit, over temperature and open load detection.

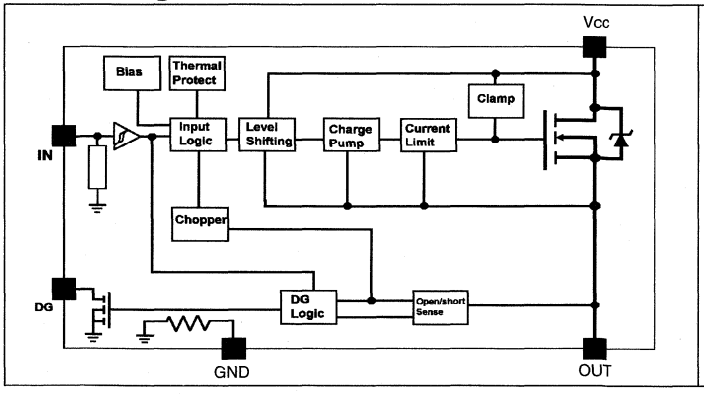
Applications

- Solenoid driver
- Programmable logic controller

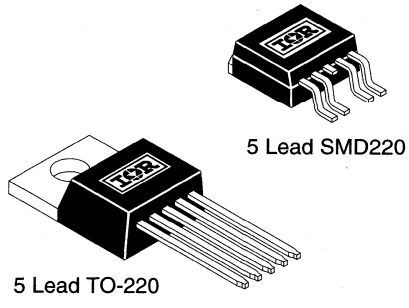
Truth Table

Condition	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Output Open	H	H	H
Output Open	L	H	H
Shorted Output	H	Current-Limiting PWM Mode	L
Shorted Output	L	L	L
Over-Temperature	H	L	L
Over-Temperature	L	L	L

Block Diagram



Available Packages



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (T_C = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{cc}	Supply voltage permanent	-0.3	50	V	
	reverse	-16	—		For 10 seconds, (1)
V_{offset}	Logic to power ground offset	V_{cc} -50	V_{cc} +0.3		
V_{in}	Input voltage	-0.3	30		
I_{in}	Input current	—	10	mA	
V_{out}	Output voltage	V_{cc} -50	V_{cc} +0.3	V	
I_{out}	Output current	—	self-limited	A	
V_{dg}	Diagnostic output voltage	-0.3	30	V	
I_{dg}	Diagnostic output current	—	10	mA	
Eav	Repetitive avalanche energy	—	200	mJ	I = 2A (2)
ESD1	Electrostatic discharge (Human Body Model)	—	4000	V	C = 100 pF,R = 1500Ω
ESD2	Electrostatic discharge (Machine Model)	—	1000	V	C = 200 pF, R = 0Ω
PD	Power dissipation	—	28	W	Tcase= 25°C
T_{Jop}	Operating junction temperature range	-40	150	°C	
T_{Stg}	Storage temperature range	-40	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

NOTES: (1) with 15kΩ resistors in input and diagnostic

(2) maximum frequency depends on heatsink (rectangular waveform)

Static Electrical Characteristics

(T_C= 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ccop}	Operating voltage range	5	—	35	V	
I_{ccoff}	Sleep mode supply current	—	40	—	μA	V_{cc}=24V, V_{in}= 0V
I_{ccon}	Supply current (average)	—	3	—	mA	V_{in} = 5V
I_{ccac}	Supply current (AC RMS)	—	20	—	μA	V_{in} = 5V
V_{ih}	High level input threshold voltage	—	2	2.5	V	
V_{il}	Low level input threshold voltage	1	1.8	—		
I_{lon}	On-state input current	10	—	70	μA	V_{in} = 3.5V
I_{loff}	Off-state input current	1	—	30		V_{in} = 0.4V
I_{oh}	Output leakage current	—	20	—		V_{out} = 6V
I_{ol}	Output leakage current	0	—	10		V_{out} = 0V
V_{dgl}	Low level diagnostic output voltage	—	0.3	—	V	I_{dg} = 1.6mA
I_{dgh}	Diagnostic output leakage current	0	—	10	μA	V_{dg} = 5V
$R_{DS(on)}$	On-state resistance	—	80	100	mΩ	I_{out} = 1A
		—	120	—		V_{cc} = 5V, I_{out} = 1A

Switching Electrical Characteristics

(V_{CC} = 14V, resistive load (R_L) = 12Ω, T_C= 25°C.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_c	Over-current cycle time	—	5	—	ms	
D_c	Over-current duty cycle	—	10	—	%	
t_{on}	Turn-on delay time to 90%	—	50	—	µs	
t_{off}	Turn-off delay time to 10%	—	60	—		
dv/dt_{on}	Slew rate on	—	3	—	V/µs	
dv/dt_{off}	Slew rate off	—	5	—		

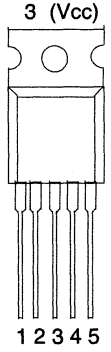
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	—	10	—	A	
V_{sc}	Short circuit detection voltage	—	3.5	—	V	
V_{slh}	Open load detection voltage	—	3.5	—		
V_{cl1}	Output negative clamp	50	54	—		I_{out} = 10mA
V_{cl2}	Output negative clamp	—	56	62		I_{out} = 2A

Thermal Characteristics

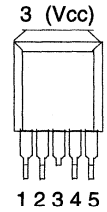
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{jsd}	Thermal shutdown temperature	—	170	—	°C	
T_{hys}	Thermal hysteresis	—	10	—		
R_{thjc}	Thermal resistance, junction to case	—	3.5	—	°C/W	
R_{thja}	Thermal resistance, junction to ambient	—	50	—		

Lead Assignments



5 Lead - TO-220

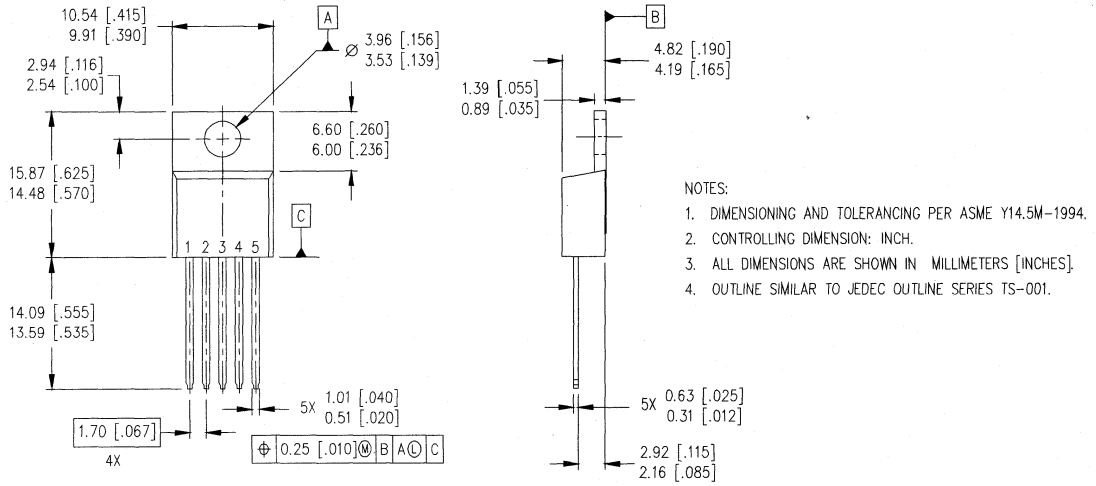
1 - Ground
2 - In
3 - Vcc
4 - DG
5 - Out



5 Lead - D²PAK (SMD220)

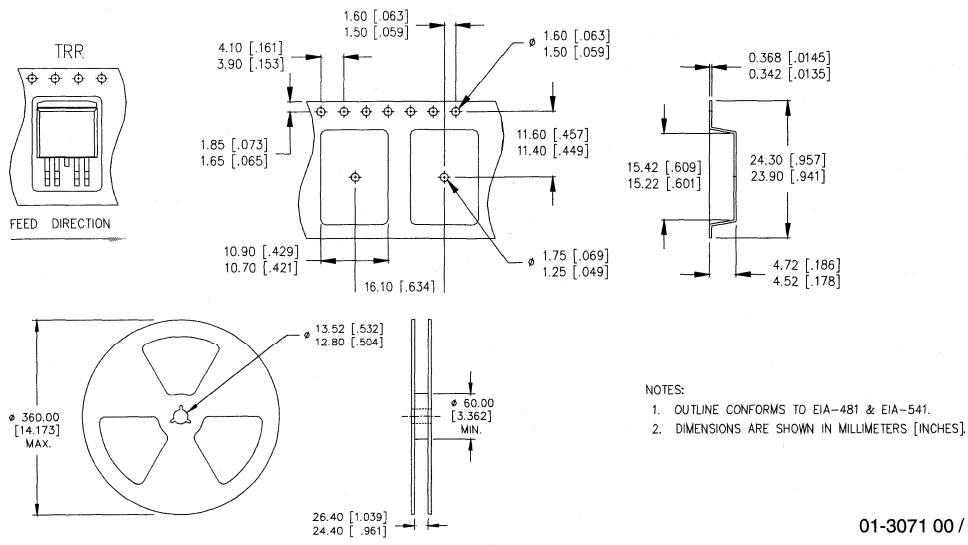
IR6220	IR6220S
Part Number	

Case Outline 5 Lead - TO-220



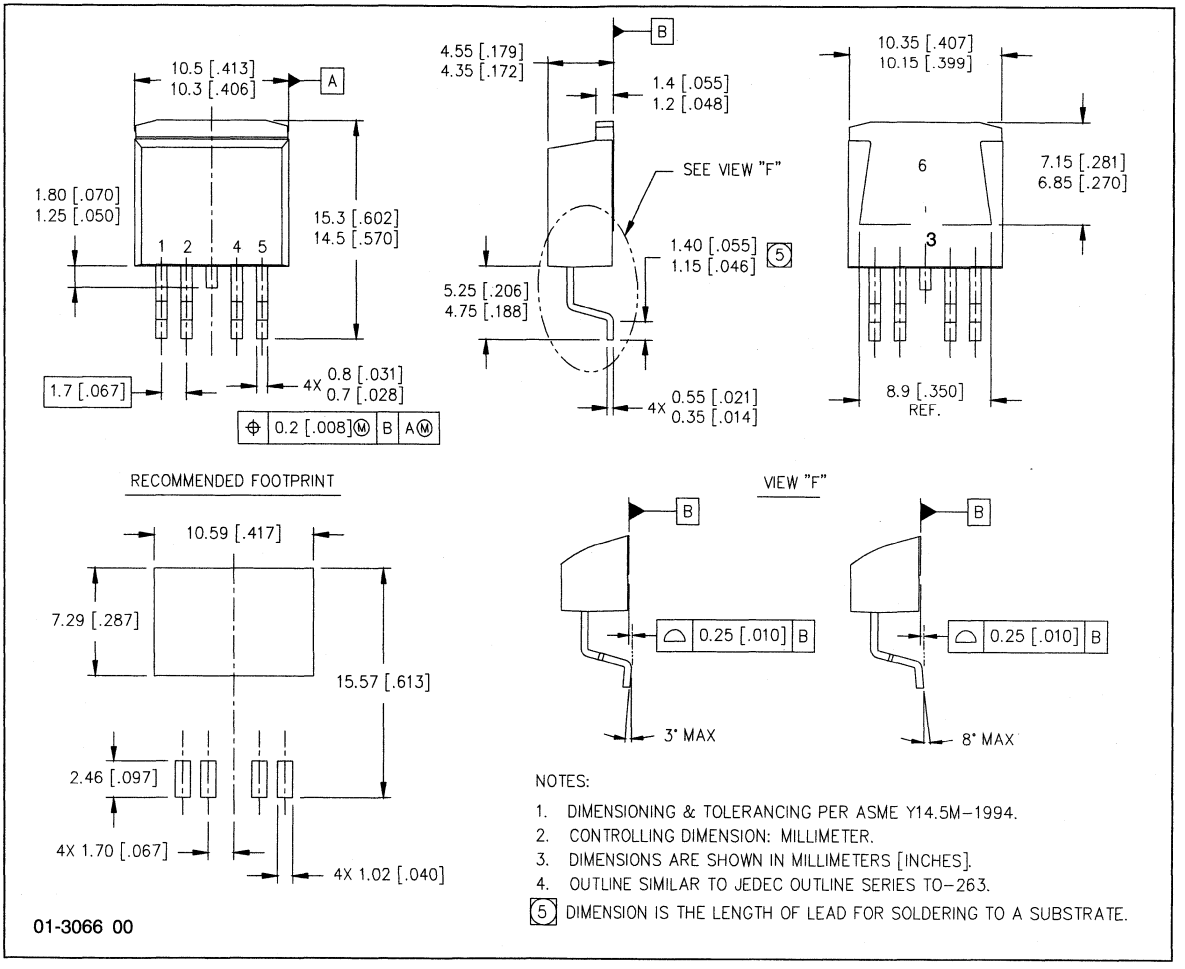
IRGB 01-3042 01

Tape & Reel 5 Lead - D²PAK (SMD220)



01-3071 00 / 01-3072 00

Case Outline 5 Lead - SMD220 (D^2PAK)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO–263.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

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International
IOR Rectifier

IR6224 (NOTE: For new designs, we recommend IR's new products IPS521 and IPS521S)

INTELLIGENT HIGH SIDE MOSFET POWER SWITCH

Features

- PWM current limit for short circuit protection
- Over-temperature protection
- Active output negative clamp
- Reverse battery protection for logic circuit
- Broken ground protection
- Short to V_{CC} protection
- Low noise charge pump
- Sleep mode supply current
- 4kV ESD protection on all leads
- Logic ground isolated from power ground

General Description

The IR6224 is a 5 terminal monolithic HIGH SIDE SWITCH with built in short circuit, over- temperature, ESD protections, inductive load turn off capability and diagnostic feedback.

The on-chip protection circuit goes into PWM mode, limiting the average current during short circuit if the drain current exceeds 20A. The protection circuit latches off the high side switch if the junction temperature exceeds 170°C and latches on after the junction temperature falls by 10°C. The Vcc (drain) to out (source) voltage is actively clamped at 55V, improving its performance during turn off with inductive loads.

The on-chip charge pump high side driver stage is floating and referenced to the source of the Power MOSFET. Thus the logic to power ground isolation can be as high as 50V. This allows operation with larger offset as well as controlling the switch during load energy recirculation or regeneration.

A diagnostic pin is provided for status feedback of short circuit, over temperature and open load detection.

Product summary

$V_{cc(op)}$	5-50V
$R_{DS(on)}$	100mΩ
I_{lim}	20A
$T_{j(sd)}$	170°C
E_{av}	200mJ

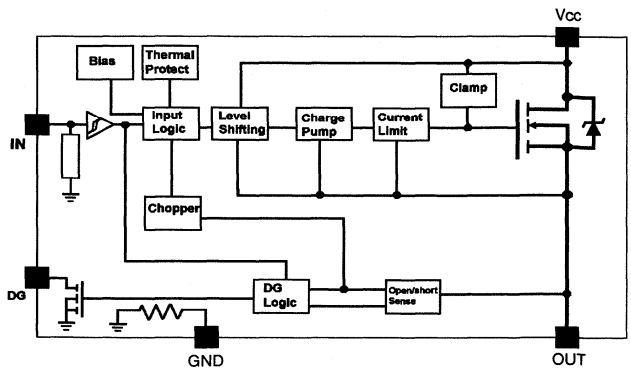
Applications

- Solenoid driver
- Programmable logic controller

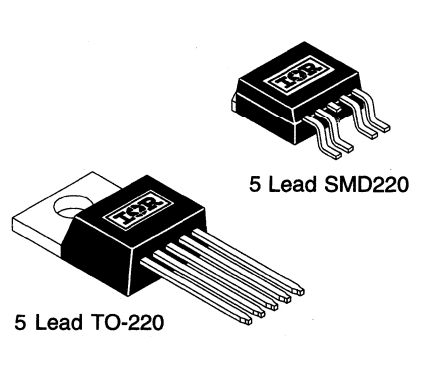
Truth Table

Condition	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Output Open	H	H	H
Output Open	L	H	H
Shorted Output	H	Current-Limiting PWM Mode	L
Shorted Output	L	L	L
Over-Temperature	H	L	L
Over-Temperature	L	L	L

Block Diagram



Available Packages



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (T_C = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{cc}	Supply voltage permanent	-0.3	35	V	
	reverse	-16	—		For 10 seconds, (1)
V_{offset}	Logic to power ground offset	V_{cc} -50	V_{cc} +0.3		
V_{in}	Input voltage	-0.3	30		
I_{in}	Input current	—	10	mA	
V_{out}	Output voltage	V_{cc} -50	V_{cc} +0.3	V	
I_{out}	Output current	—	self-limited	A	
V_{dg}	Diagnostic output voltage	-0.3	30	V	
I_{dg}	Diagnostic output current	—	10	mA	
E_{av}	Repetitive avalanche energy	—	200	mJ	I = 2A (2)
ESD1	Electrostatic discharge (Human Body Model)	—	4000	V	C = 100 pF,R = 1500Ω
ESD2	Electrostatic discharge (Machine Model)	—	1000	V	C = 200 pF, R = 0Ω
P_D	Power dissipation	—	28	W	Tcase= 25°C
T_{Jop}	Operating junction temperature range	-40	150	°C	
T_{Stg}	Storage temperature range	-40	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

NOTES: (1) with 15kΩ resistors in input and diagnostic

(2) maximum frequency depends on heatsink (rectangular waveform)

Static Electrical Characteristics

(T_C= 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ccop}	Operating Voltage Range	5	—	50	V	
I_{ccoff}	Sleep Mode Supply Current	—	40	—	µA	V_{cc}=24V, V_{in}= 0V
I_{ccon}	Supply Current (Average)	—	3	—	mA	V_{in} = 5V
I_{ccac}	Supply Current (AC RMS)	—	20	—	µA	V_{in} = 5V
V_{ih}	High Level Input Threshold Voltage	—	2	2.5	V	
V_{il}	Low Level Input Threshold Voltage	1	1.8	—		
I_{lon}	On-State Input Current	10	—	70	µA	V_{in} = 3.5V
I_{loff}	Off-State Input Current	1	—	30		V_{in} = 0.4V
I_{oh}	Output Leakage Current	—	20	—		V_{out} = 6V
I_{ol}	Output Leakage Current	0	—	10		V_{out} = 0V
V_{dgl}	Low Level Diagnostic Output Voltage	—	0.3	—	V	I_{dg} = 1.6mA
I_{dgh}	Diagnostic Output Leakage Current	0	—	10	µA	V_{dg} = 5V
$R_{DS(on)}$	On-State Resistance	—	80	100	mΩ	I_{out} = 1A
		—	120	—		V_{cc} = 5V, I_{out} = 1A

Switching Electrical Characteristics

(V_{CC} = 14V, resistive load (R_L) = 12Ω, T_C= 25°C.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_c	Over-current cycle time	—	5	—	ms	
D_c	Over-current duty cycle	—	10	—	%	
t_{on}	Turn-on delay time to 90%	—	50	—	µs	
t_{off}	Turn-off delay time to 10%	—	60	—		
dv/dt_{on}	Slew rate on	—	3	—	V/µs	
dv/dt_{off}	Slew rate off	—	5	—		

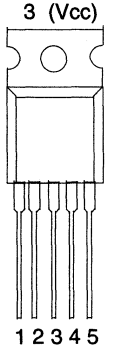
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	—	20	—	A	
V_{sc}	Short circuit detection voltage	—	3.5	—	V	
V_{slh}	Open load detection voltage	—	3.5	—		
V_{cl1}	Output negative clamp	50	54	—		I_{out} = 10mA
V_{cl2}	Output negative clamp	—	56	62		I_{out} = 2A

Thermal Characteristics

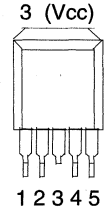
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{jsd}	Thermal shutdown temperature	—	170	—	°C	
T_{hys}	Thermal hysteresis	—	10	—		
R_{thjc}	Thermal resistance, junction to case	—	3.5	—	°C/W	
R_{thja}	Thermal resistance, junction to ambient	—	50	—		

Lead Assignments



5 Lead - TO-220

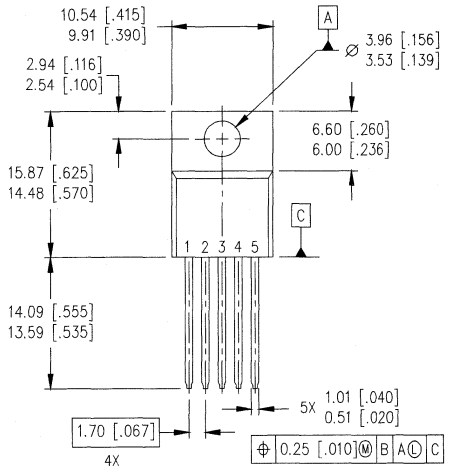
1 - Ground
2 - In
3 - Vcc
4 - DG
5 - Out

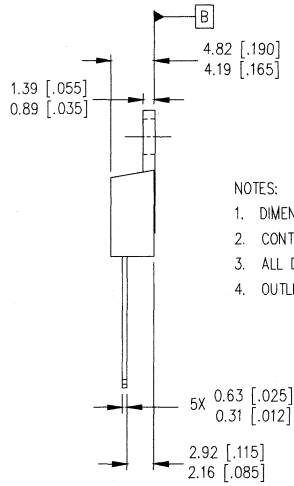


5 Lead - D²PAK (SMD220)

IR6224	IR6224S
Part Number	

Case Outline 5 Lead - TO-220

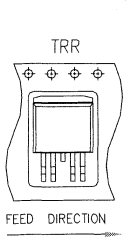


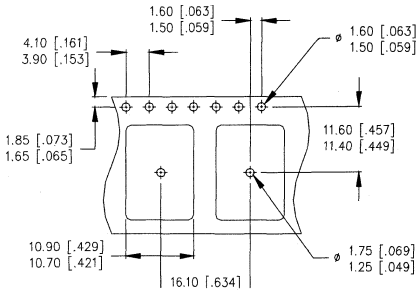


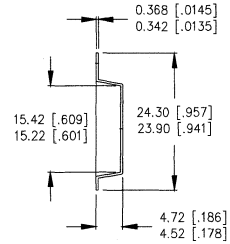
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TS-001.

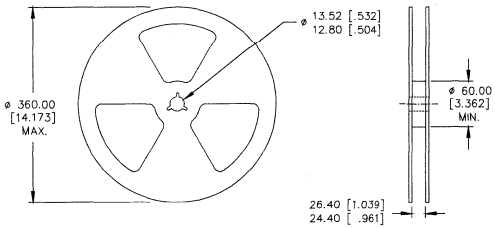
IRGB01-3042 01

Tape & Reel 5 Lead - D²PAK (SMD220)





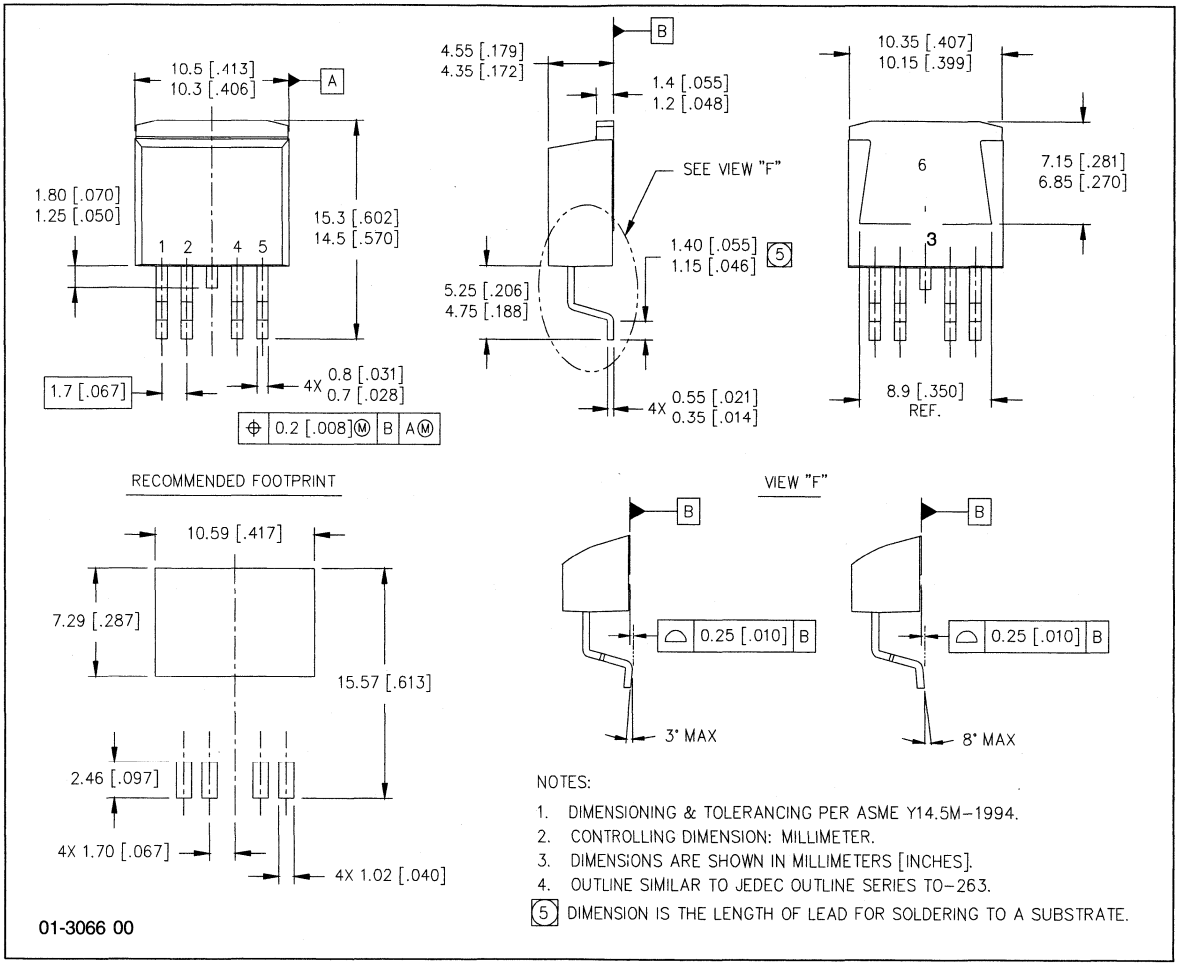




NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

01-3071 00 / 01-3072 00

Case Outline 5 Lead - SMD220 (D^2PAK)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO-263.

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International
IOR Rectifier

IR6226 (NOTE: For new designs, we recommend IR's new products IPS521 and IPS521S)

INTELLIGENT HIGH SIDE MOSFET POWER SWITCH

Features

- Current limit for short circuit protection
- Over-temperature protection
- Active output negative clamp
- Reverse battery protection for logic circuit
- Broken ground protection
- Short to V_{CC} protection
- Low noise charge pump
- Sleep mode supply current
- 4kV ESD protection on all leads
- Logic ground isolated from power ground

General Description

The IR6226 is a 5 terminal monolithic HIGH SIDE SWITCH with built in short circuit, over- temperature, ESD protections, inductive load turn off capability and diagnostic feedback.

The on-chip protection circuit limits the average current during short circuit if the drain current exceeds 20A. The protection circuit latches off the high side switch if the junction temperature exceeds 170°C and latches on after the junction temperature falls by 10°C. The Vcc (drain) to OUT (source) voltage is actively clamped at 55V, improving its performance during turn off with inductive loads.

The on-chip charge pump high side driver stage is floating and referenced to the source of the Power MOSFET. Thus the logic to power ground isolation can be as high as 50V. This allows operation with larger offset as well as controlling the switch during load energy recirculation or regeneration.

A diagnostic pin is provided for status feedback of short circuit, over temperature and open load detection.

Product summary

$V_{cc(op)}$	5-50V
$R_{DS(on)}$	100mΩ
I_{lim}	20A
$T_{j(sd)}$	170°C
E_{av}	200mJ

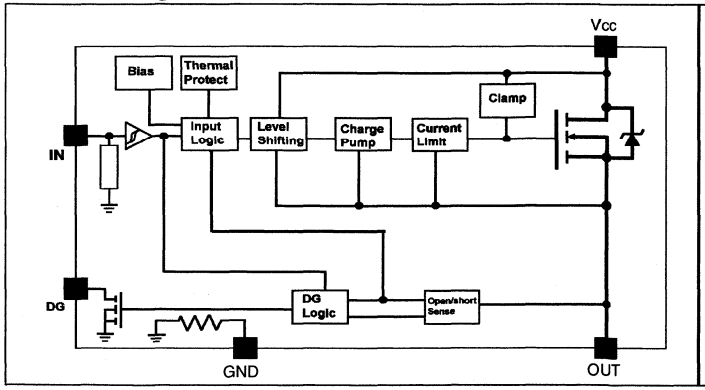
Applications

- Lamp driver
- Programmable logic controller

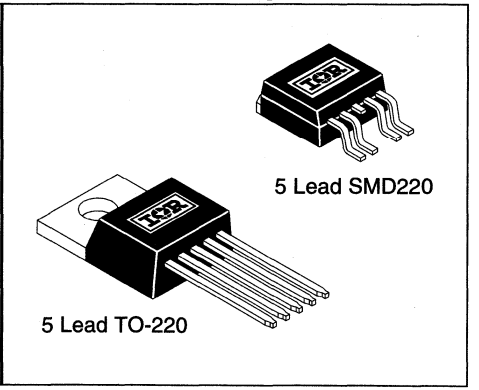
Truth Table

Condition	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Output Open	H	H	H
Output Open	L	H	H
Shorted Output	H	Current-Limiting Linear Mode	L
Shorted Output	L	L	L
Over-Temperature	H	L	L
Over-Temperature	L	L	L

Block Diagram



Available Packages



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. (T_C = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{cc}	Supply voltage permanent	-0.3	50	V	
	reverse	-16	—		For 10 seconds, (1)
V_{offset}	Logic to power ground offset	Vcc -50	Vcc +0.3		
V_{in}	Input voltage	-0.3	30		
I_{in}	Input current	—	10	mA	
V_{out}	Output voltage	Vcc -50	Vcc +0.3	V	
I_{out}	Output current	—	self-limited	A	
V_{dg}	Diagnostic output voltage	-0.3	30	V	
I_{dg}	Diagnostic output current	—	10	mA	
E_{av}	Repetitive avalanche energy	—	200	mJ	I = 2A (2)
ESD1	Electrostatic discharge (Human Body Model)	—	4000	V	C = 100 pF,R = 1500Ω
ESD2	Electrostatic discharge (Machine Model)	—	1000	V	C = 200 pF, R = 0Ω
PD	Power dissipation	—	28	W	Tcase= 25°C
T_{Jop}	Operating junction temperature range	-40	150	°C	
T_{Stg}	Storage temperature range	-40	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

NOTES: (1) with 15kΩ resistors in input and diagnostic

(2) maximum frequency depends on heatsink (rectangular waveform)

Static Electrical Characteristics

(T_C= 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ccop}	Operating voltage range	5	—	35	V	
I_{ccoff}	Sleep mode supply current	—	40	—	µA	V_{cc}=24V, V_{in}= 0V
I_{ccon}	Supply current (average)	—	3	—	mA	V_{in} = 5V
I_{ccac}	Supply current (AC RMS)	—	20	—	µA	V_{in} = 5V
V_{ih}	High level input threshold voltage	—	2	2.5	V	
V_{il}	Low level input threshold voltage	1	1.8	—		
I_{lon}	On-state input current	10	—	70	µA	V_{in} = 3.5V
I_{loff}	Off-state input current	1	—	30		V_{in} = 0.4V
I_{oh}	Output leakage current	—	20	—		V_{out} = 6V
I_{ol}	Output leakage current	0	—	10		V_{out} = 0V
V_{dgl}	Low level diagnostic output voltage	—	0.3	—	V	I_{dg} = 1.6mA
I_{dgh}	Diagnostic output leakage current	0	—	10	µA	V_{dg} = 5V
$R_{DS(on)}$	On-state resistance	—	80	100	mΩ	I_{out} = 1A
		—	120	—		V_{cc} = 5V, I_{out} = 1A

Switching Electrical Characteristics

(V_{CC} = 14V, Resistive Load (R_L) = 12Ω, T_C= 25°C.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on delay time to 90%	—	50	—	µs	
t_{off}	Turn-off delay time to 10%	—	60	—		
dv/dt_{on}	Slew rate on	—	3	—	V/µs	
dv/dt_{off}	Slew rate off	—	5	—		

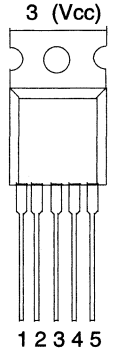
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	—	20	—	A	
V_{sc}	Short circuit detection voltage	—	3.5	—	V	
V_{slh}	Open load detection voltage	—	3.5	—		
V_{cl1}	Output negative clamp	50	54	—		I_{out} = 10mA
V_{cl2}	Output negative clamp	—	56	62		I_{out} = 2A

Thermal Characteristics

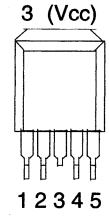
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{jsd}	Thermal shutdown temperature	—	170	—	°C	
T_{hys}	Thermal hysteresis	—	10	—		
R_{thjc}	Thermal resistance, junction to case	—	3.5	—	°C/W	
R_{thja}	Thermal resistance, junction to ambient	—	50	—		

Lead Assignments



5 Lead - TO-220

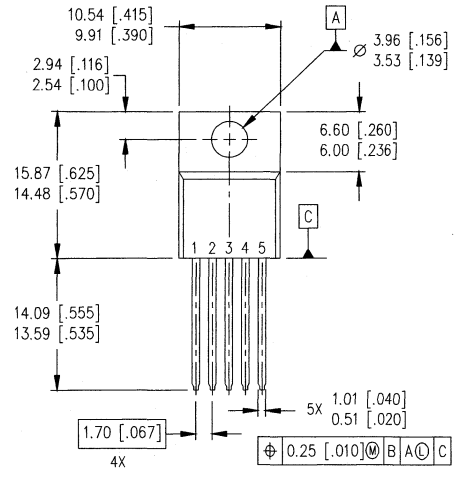
1 - Ground
2 - In
3 - Vcc
4 - DG
5 - Out

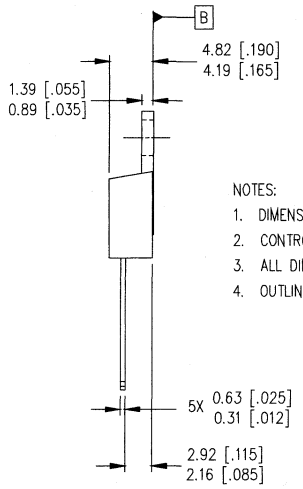


5 Lead - D²PAK (SMD220)

IR6226	IR6226S
Part Number	

Case Outline 5 Lead - TO-220

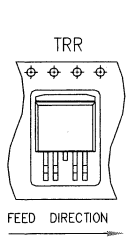


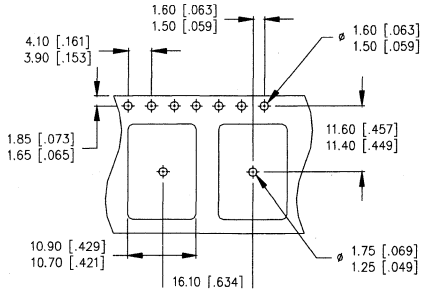


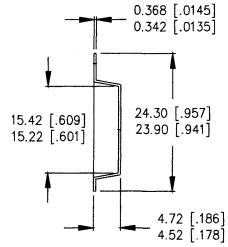
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TS-001.

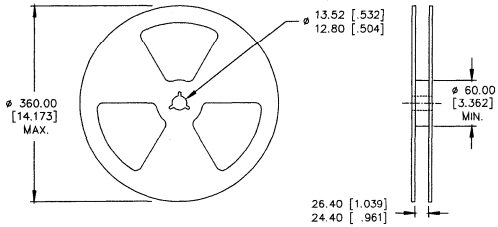
IRGB 01-3042 01

Tape & Reel 5 Lead - D²PAK (SMD220)









NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

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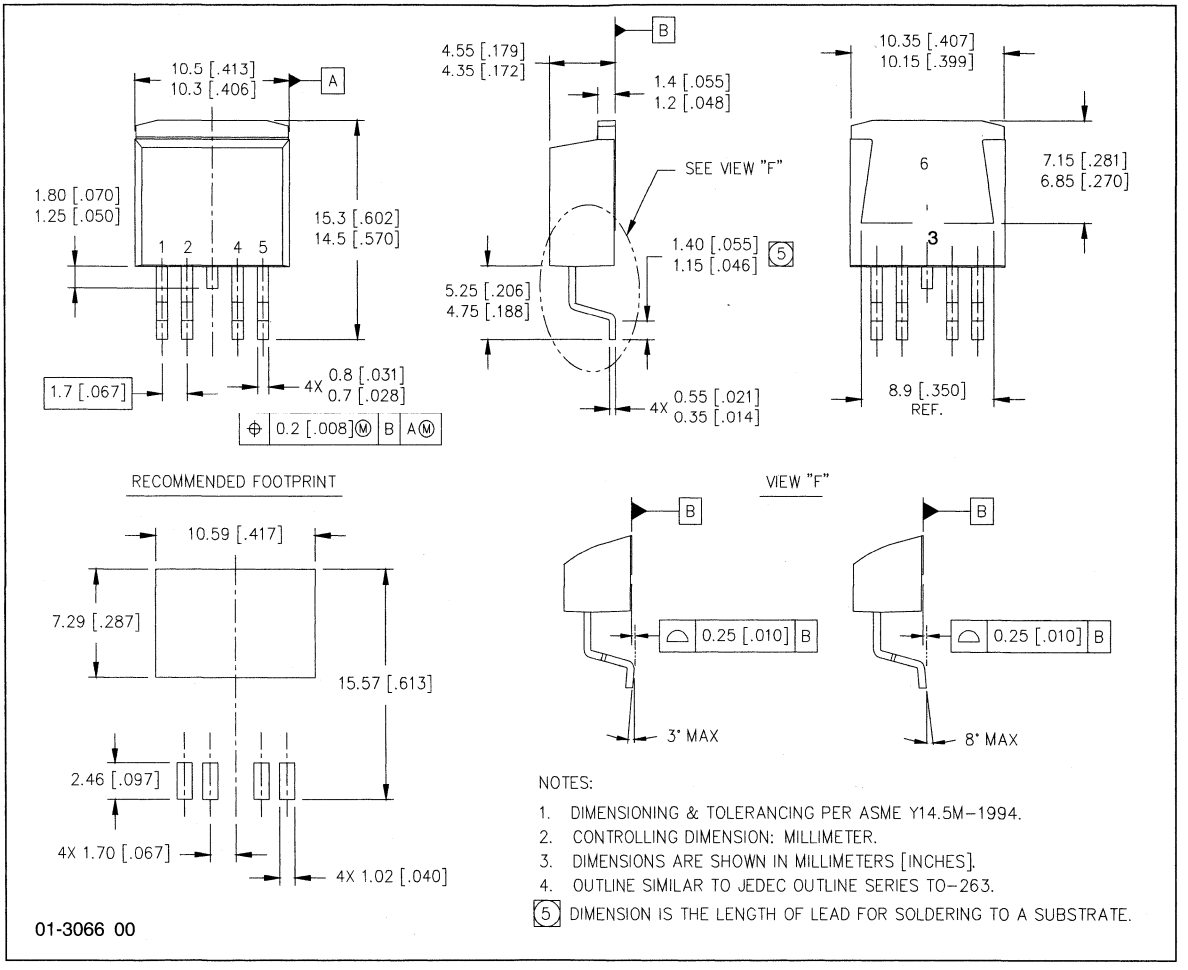
Case Outline 5 Lead - SMD220 (D^2PAK)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO–263.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

International
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Gate Driver IC
DATA SHEETS

GATE DRIVER IC

GATE DRIVER IC

Preliminary Data Sheet No. PD60162-K

IR2106/IR21064
IR2186

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V (IR2106(4)) or 5 to 20V (IR2186)
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IR2106/IR2186)

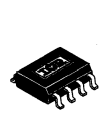
Product Summary

V_{OFFSET}	600V max.	
I_{O}+/-	120 mA / 250 mA	
V_{OUT}	10 - 20V (IR2106(4))	5 - 20V (IR2186)
$t_{on/off}$ (typ.)	180 ns	
Delay matching	50 ns	

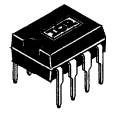
Description

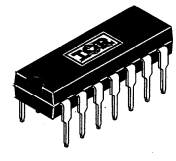
The IR2106/IR2186 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages

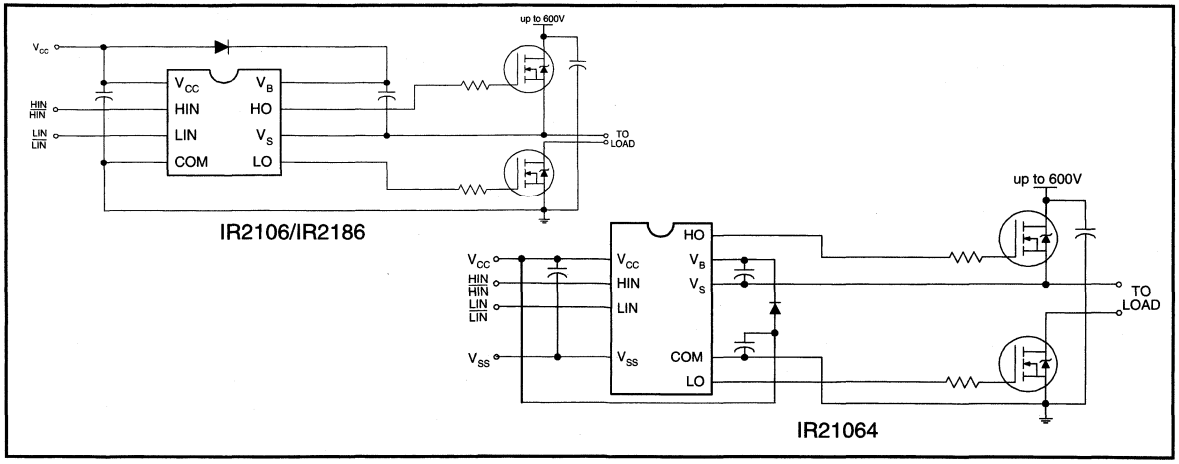

8 Lead SOIC


14 Lead SOIC


8 Lead PDIP


14 Lead PDIP

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21064 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
$RthJA$	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition		Min.	Max.	Units
VB	High side floating supply absolute voltage				V
		IR2106(4)	V_S + 10	V_S + 20	
		IR2186	V_S + 5	V_S + 20	
V_S	High side floating supply offset voltage		Note 1	600	
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage				
		IR2106(4)	10	20	
		IR2186	5	20	
V_{LO}	Low side output voltage		0	V_{CC}	
V_{IN}	Logic input voltage		V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21064 only)		-5	5	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

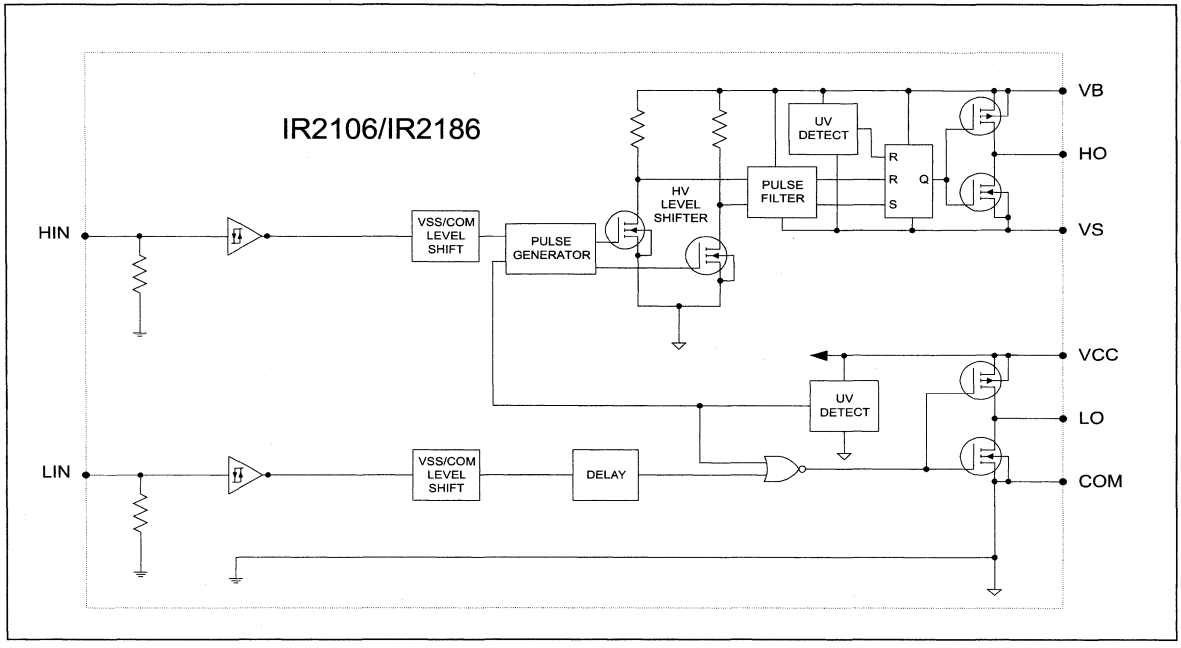
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	170	250		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V

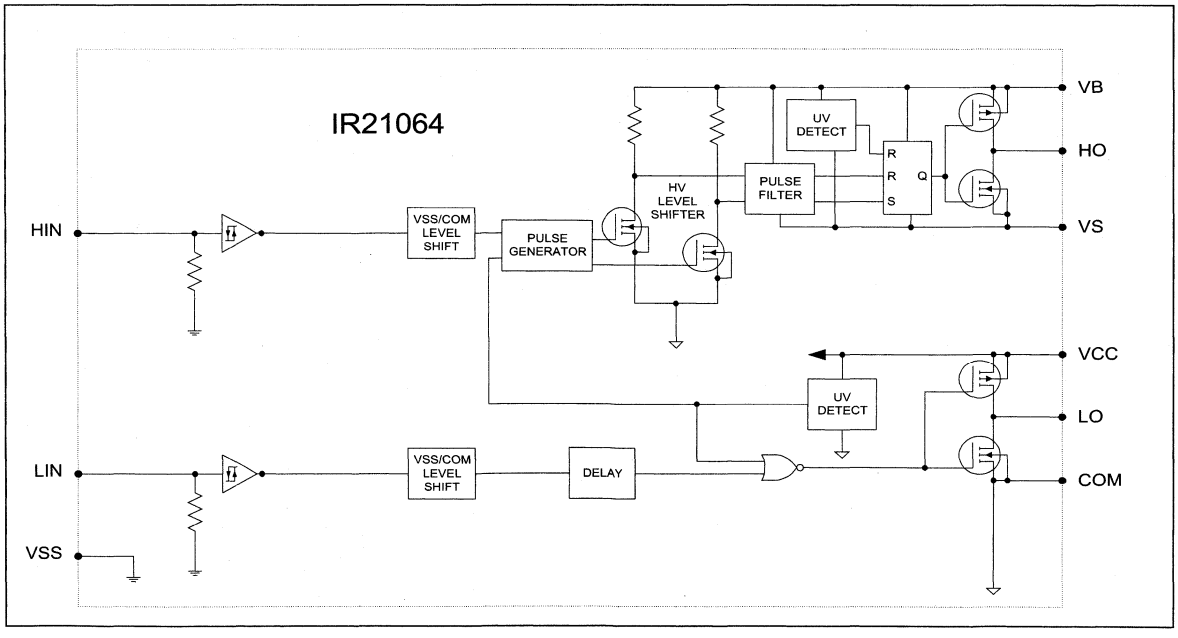
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage (IR2106(4)/IR2186)	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage (IR2106(4)/IR2186)	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current V_{IN} = 5V (IR2106(4)/IR2186)	—	5	20		
I_{IN-}	Logic "0" input bias current V_{IN} = 0V (IR2106(4)/IR2186)	—	1	2		
V_{CCUV+} / V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold (IR2106(4))	8.0	8.9	9.8	V	
	(IR2186)	3.8	4.4	5.0		
V_{CCUV-} / V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold (IR2106(4))	7.4	8.2	9.0		
	(IR2186)	3.5	4.1	4.7		
V_{CCUVH} / V_{BSUVH}	Hysteresis (IR2106(4))	0.3	0.7	—		
	(IR2186)	0.1	0.3	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagrams

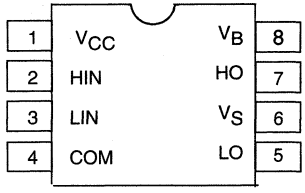




Lead Definitions

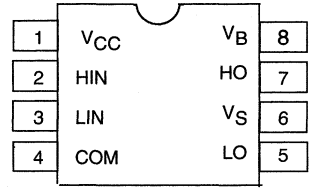
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2106(4)/IR2186)
LIN	Logic input for low side gate driver output (LO), in phase (IR2106(4)/IR2186)
VSS	Logic Ground (IR21064 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



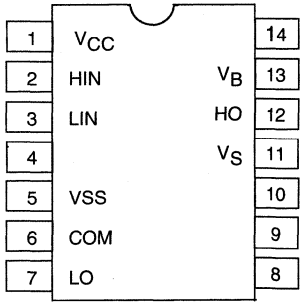
8 Lead PDIP

IR2106/IR2186



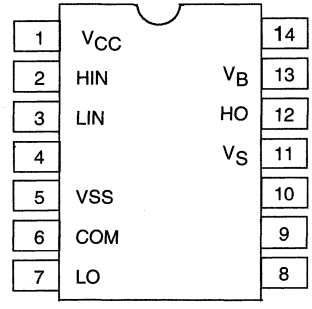
8 Lead SOIC

IR2106S/IR2186S



14 Lead PDIP

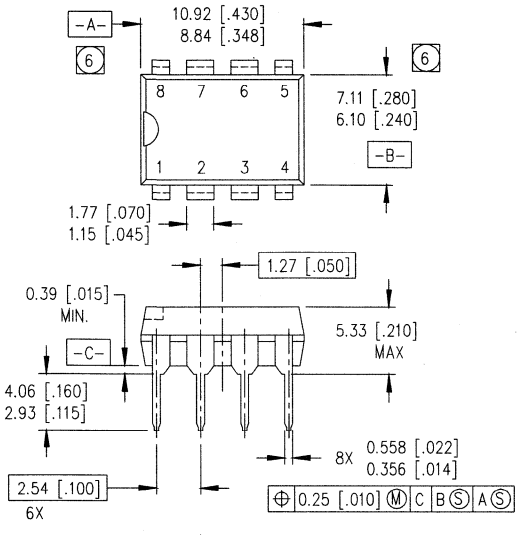
IR21064



14 Lead SOIC

IR21064S

Case Outlines

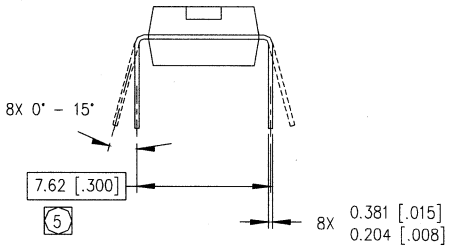


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

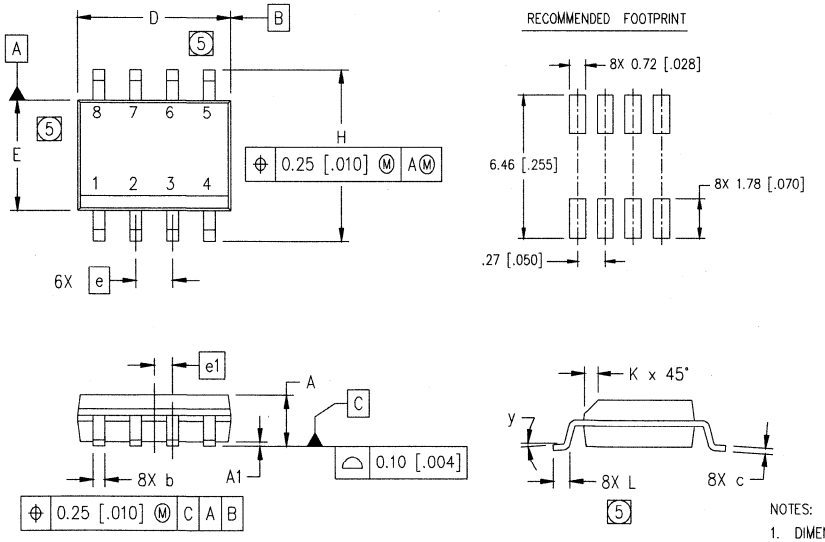
5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-3003 01



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

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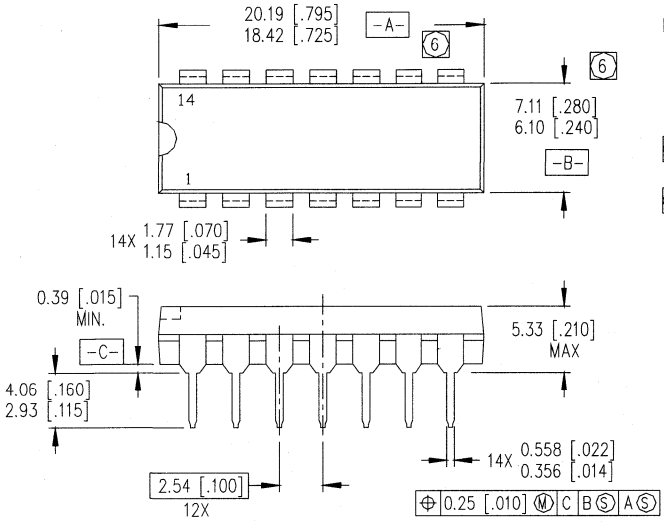
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

6 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

8 Lead SOIC



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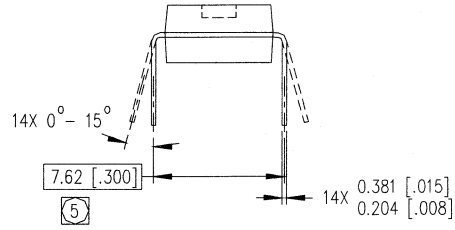
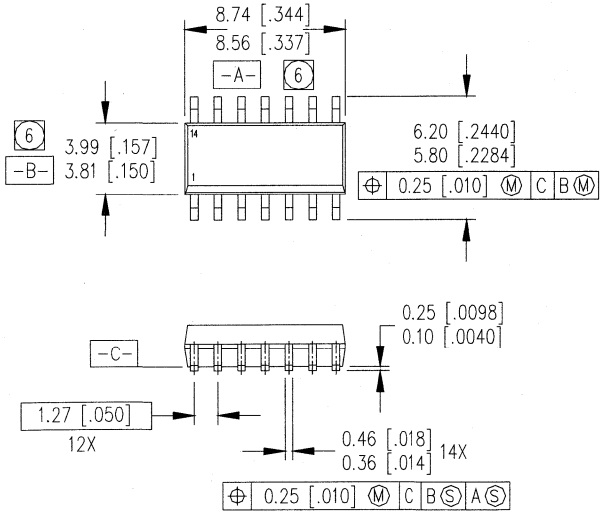


14 Lead PDIP

01-3002 03



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3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
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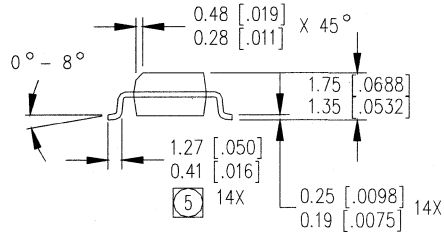


14 Lead SOIC (narrow body)

01-3063 00

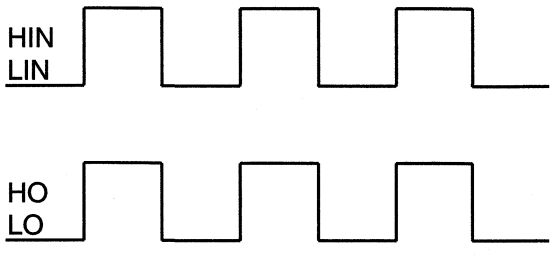


Figure 1. Input/Output Timing Diagram

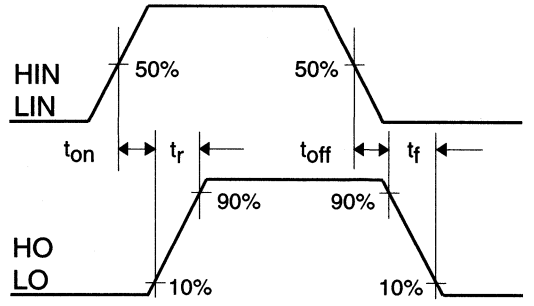


Figure 2. Switching Time Waveform Definitions

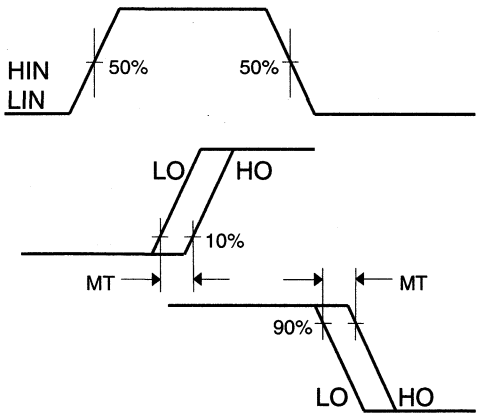


Figure 3. Delay Matching Waveform Definitions

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Data and specifications subject to change without notice. 4/17/2000

Preliminary Data Sheet No. PD60163-K

IR2109/IR21094
IR2189

HIGH AND LOW SIDE DRIVER

Features

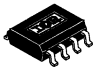
- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V (IR2109(4)) or 5 - 20V (2189)
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 500ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21094)
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels.

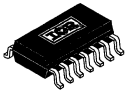
Product Summary

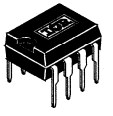
V_{OFFSET}	600V max.	
I_{O}+/-	120 mA / 250 mA	
V_{OUT}	10 - 20V (IR2109(4))	5 - 20V (IR2189)
$t_{on/off}$ (typ.)	180 ns	
Delay matching	500 ns	

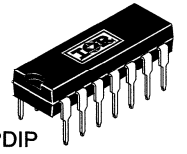
(programmable up to 5uS for IR21094)

Packages


8 Lead SOIC


14 Lead SOIC

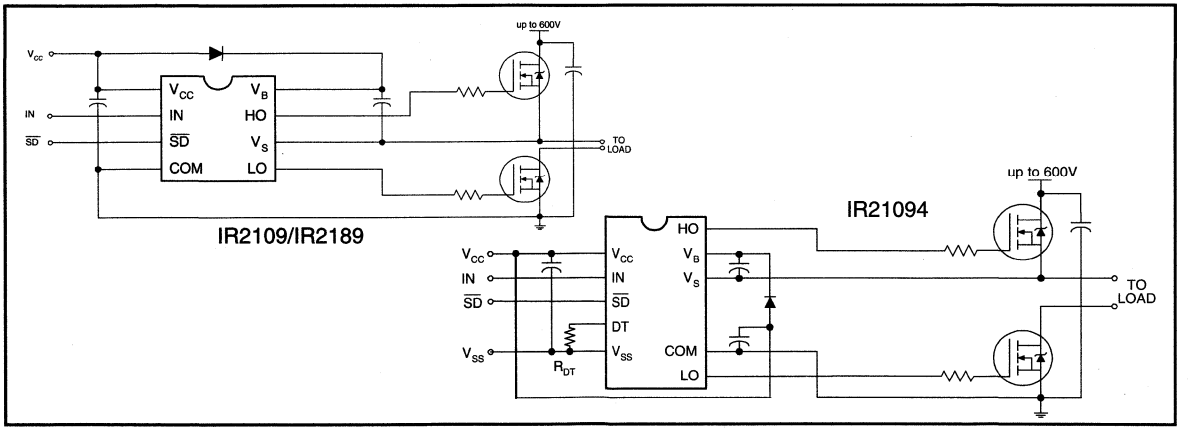

8 Lead PDIP


14 Lead PDIP

Description

The IR2109(4)/IR2189 are high voltage, high speed power MOSFET and IGBT drivers with dependant high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21094 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21094/IR21894 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition		Min.	Max.	Units
VB	High side floating supply absolute voltage				V
		IR2109(4)	V_S + 10	V_S + 20	
		IR2189	V_S + 5	V_S + 20	
V_S	High side floating supply offset voltage		Note 1	600	
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage				
		IR2109(4)	10	20	
		IR2189	5	20	
V_{LO}	Low side output voltage		0	V_{CC}	°C
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS}	V_{CC}	
DT	Programmable dead-time pin voltage (IR21094 only)		V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21094 only)		-5	5	
T_A	Ambient temperature		-40	125	

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

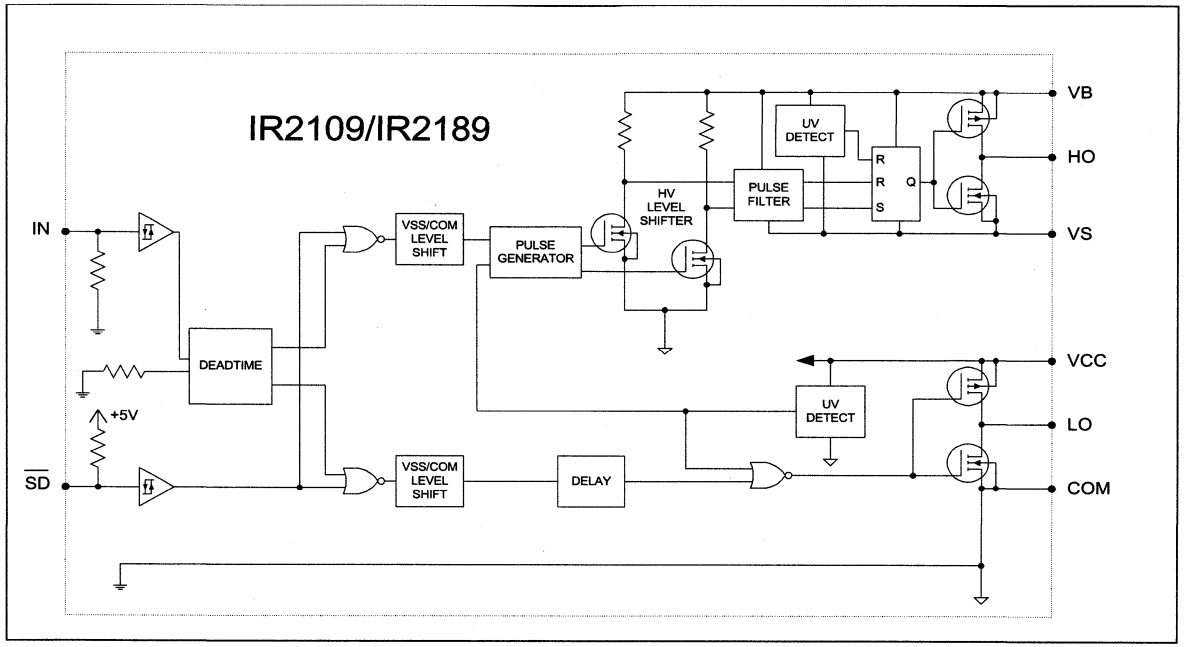
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	900	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	170	250		V_S = 0V or 600V
t_{sd}	Shut-down propagation delay	—	180	270		
MT	Delay matching, HS & LS turn-on/off	—	0	—		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO})	380	500	620		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	usec	RDT = 200k (IR21094)
MDT	Deadtime matching = DT_{LO-HO} - DT_{HO-LO}	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21094)

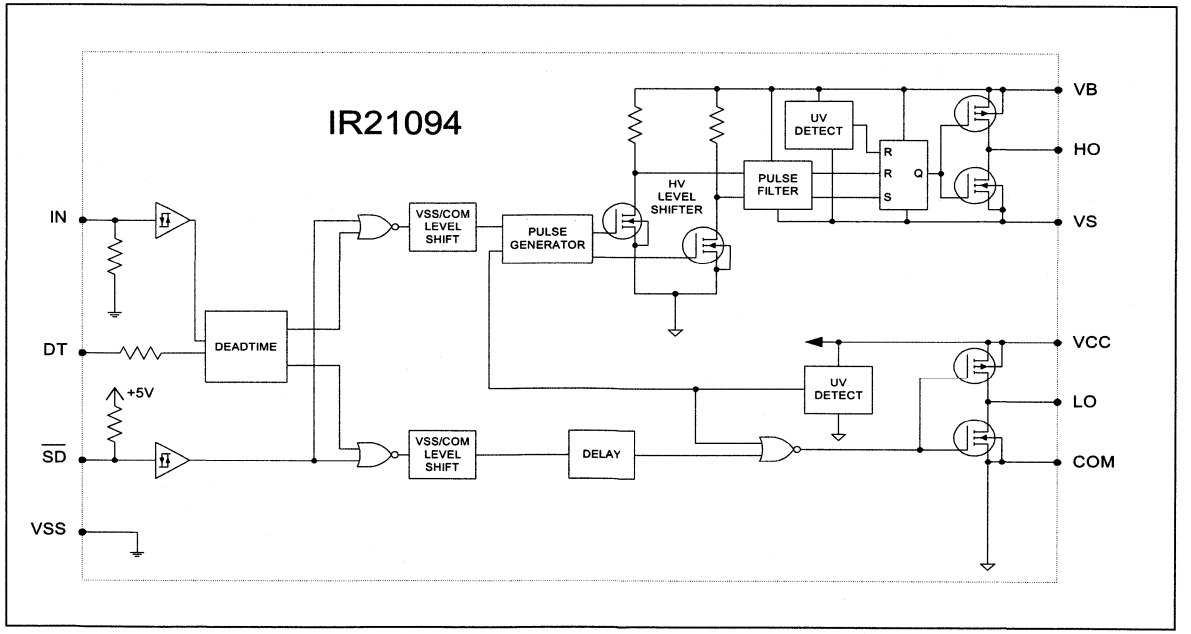
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO		2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO		—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold		2.7	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold		—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O		—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O		—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current		—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current		20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current		0.4	1.0	1.6	mA	V_{IN} = 0V or 5V RDT = 0
I_{IN+}	Logic "1" input bias current		—	5	20	µA	IN = 5V, $\overline{SD}$ = 0V
I_{IN-}	Logic "0" input bias current		—	1	2		IN = 0V, SD = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	IR2109(4)	8.0	8.9	9.8	V	
		IR2189	3.8	4.4	5.0		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} dupply undervoltage negative going threshold	IR2109(4)	7.4	8.2	9.0		
		IR2189	3.5	4.1	4.7		
V_{CCUVH} V_{BSUVH}	Hysteresis	IR2109(4)	0.3	0.7	—		
		IR2189	0.1	0.3	—		
I_{O+}	Output high short circuit pulsed vurrent		120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current		250	350	—		V_O = 15V,PW ≤ 10 µs

Functional Block Diagrams

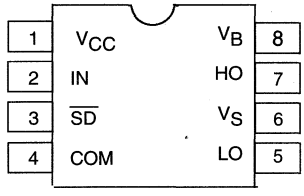




Lead Definitions

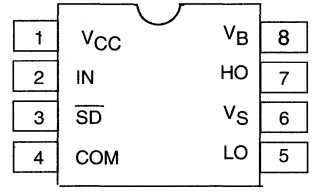
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2109/IR2189 and VSS for IR21094)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IR2109/IR2189 and VSS for IR21094)
DT	Programmable dead-time lead, referenced to VSS. (IR21094 only)
VSS	Logic Ground (21094 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



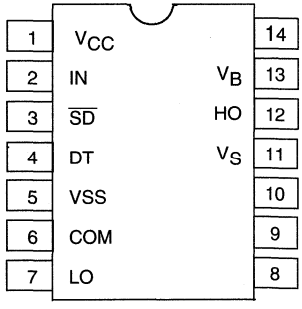
8 Lead PDIP

IR2109/IR2189



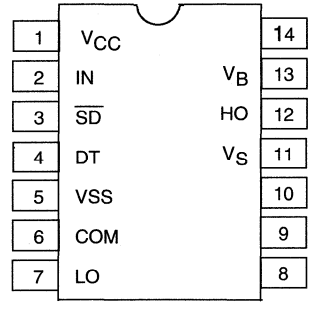
8 Lead SOIC

IR2109S/IR2189S



14 Lead PDIP

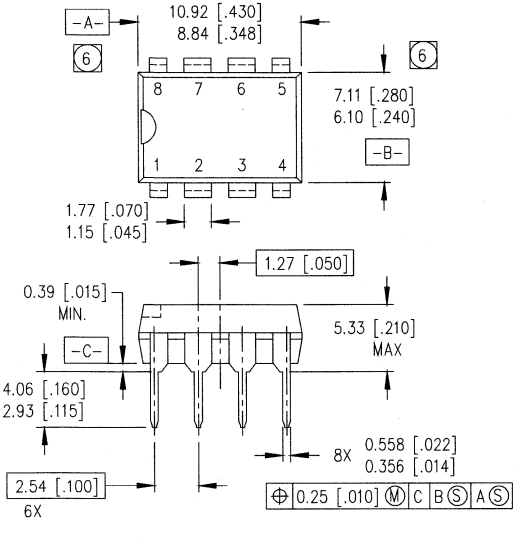
IR21094



14 Lead SOIC

IR21094S

Case Outlines



NOTES:

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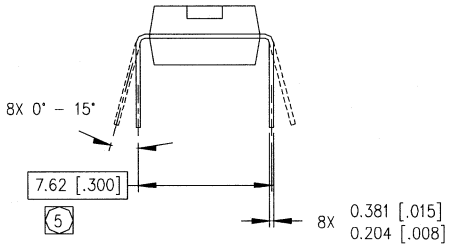
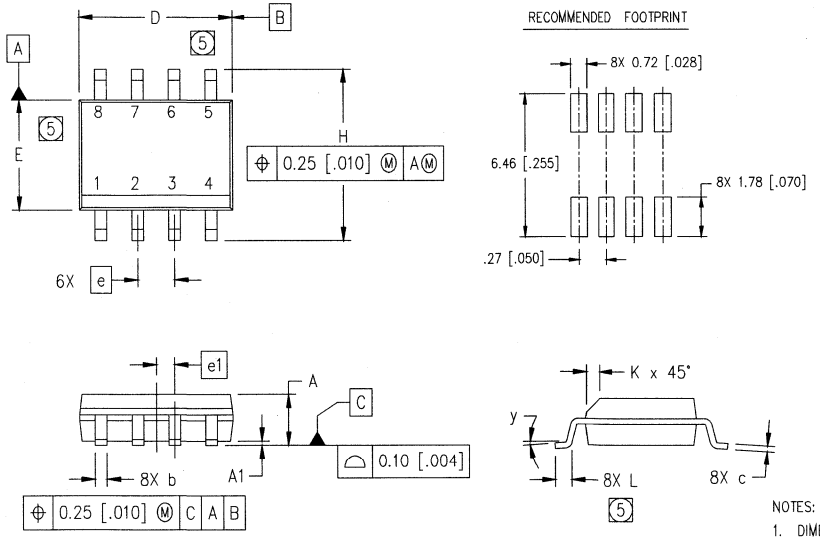


8 Lead PDIP

01-3003 01



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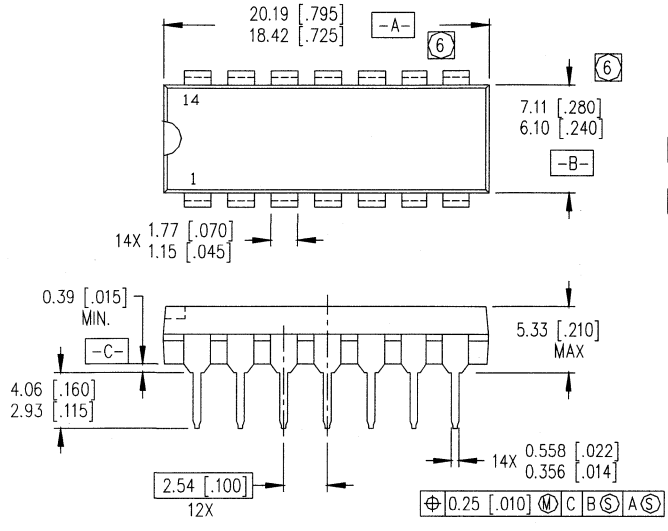
b	.011	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

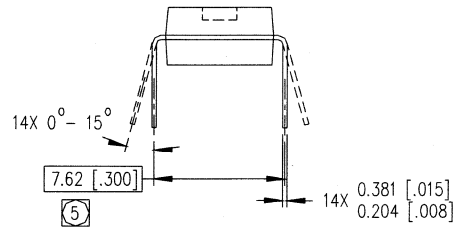
8 Lead SOIC



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.

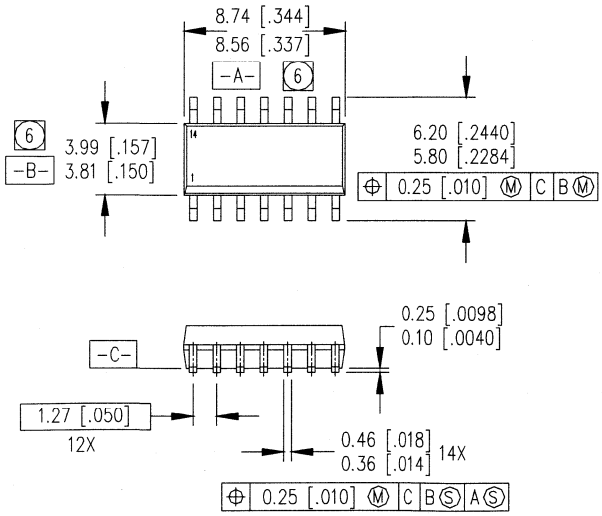
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



14 Lead PDIP

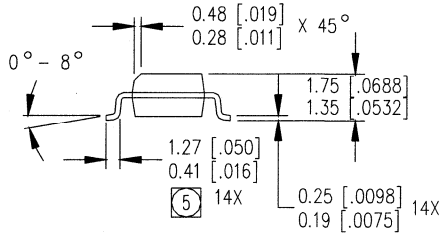
01-3002 03



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

01-3063 00

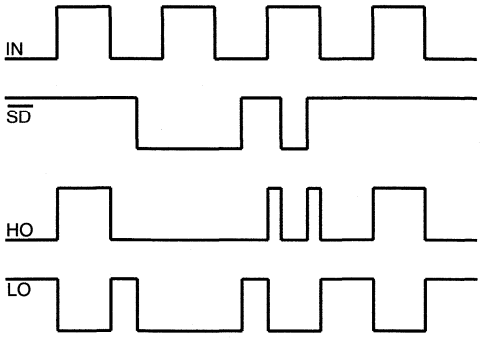


Figure 1. Input/Output Timing Diagram

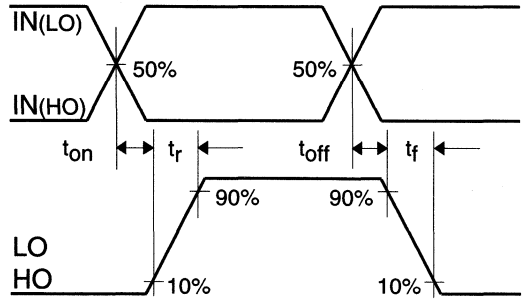


Figure 2. Switching Time Waveform Definitions

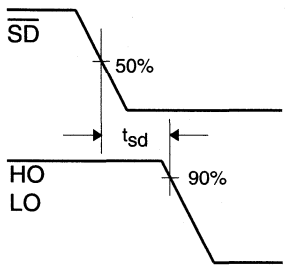


Figure 3. Shutdown Waveform Definitions

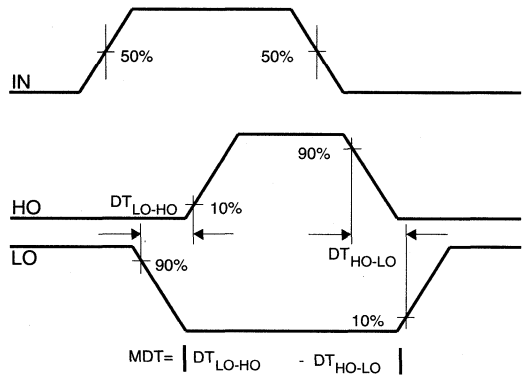


Figure 4. Deadtime Waveform Definitions

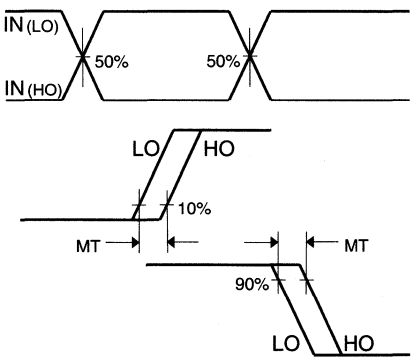


Figure 5. Delay Matching Waveform Definitions

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

International
IOR Rectifier

Data Sheet No. PD60143-L

IR2127/IR2128
IR21271

CURRENT SENSING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage dV/dt immune
- Application- specific gate drive range:
  Motor Drive: 12 to 20V (IR2127/IR2128)
  Automotive: 9 to 20V (IR21271)
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- $\overline{\text{FAULT}}$ lead indicates shutdown has occured
- Output in phase with input (IR2127/IR21271)
- Output out of phase with input (IR2128)

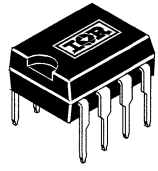
Description

The IR2127/IR2128/IR21271 is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 600 volts.

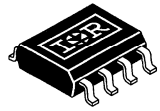
Product Summary

V_{OFFSET}	600V max.	
I_O+/-	200 mA / 420 mA	
V_{OUT}	12 - 20V (IR2127/IR2128)	9 - 20V (IR21271)
V_{CSth}	250 mV or 1.8V	
$t_{on/off}$ (typ.)	200 & 150 ns	

Packages

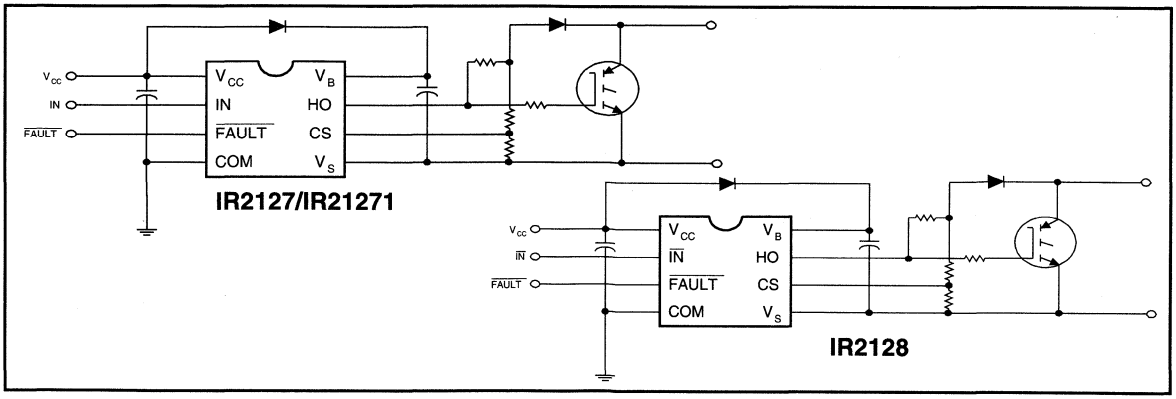


8 Lead PDIP



8 Lead SOIC

Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Logic Supply Voltage	-0.3	25	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_B + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
Rth_{JA}	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage (IR2127/IR2128)	V_S + 12	V_S + 20	V
	(IR21271)	V_S + 9	V_S + 20	
V_S	High Side Floating Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Logic Supply Voltage	10	20	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_S + 5	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

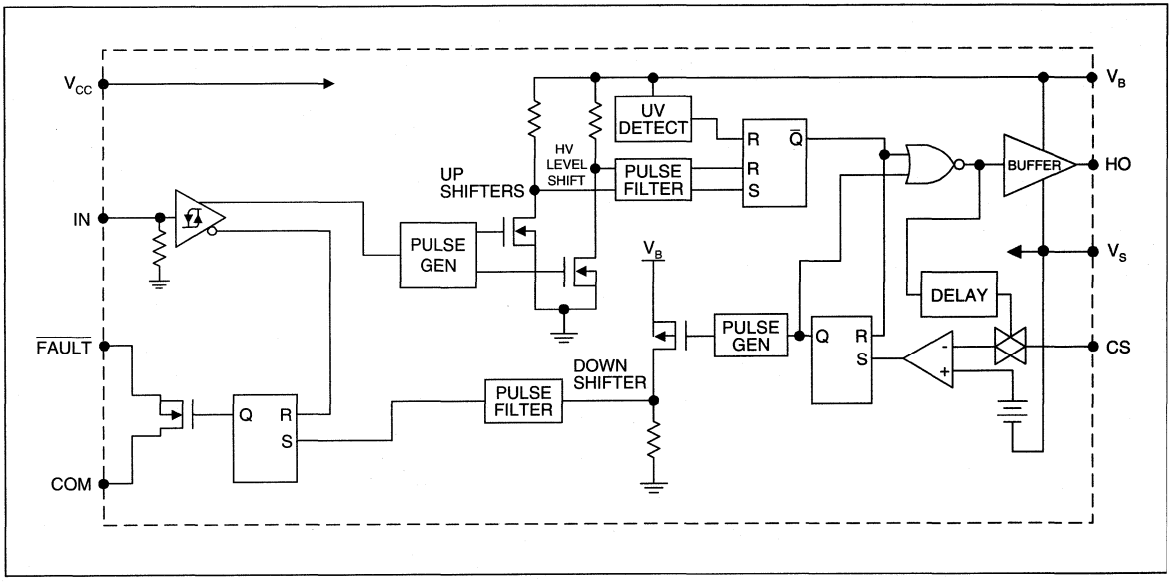
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	200	250	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	150	200		V_S = 600V
t_r	Turn-On Rise Time	—	80	130		
t_f	Turn-Off Fall Time	—	40	65		
t_{bl}	Start-Up Blanking Time	500	700	900		
t_{cs}	CS Shutdown Propagation Delay	—	240	360		
t_{flt}	CS to $\overline{FAULT}$ Pull-Up Propagation Delay	—	340	510		

Static Electrical Characteristics

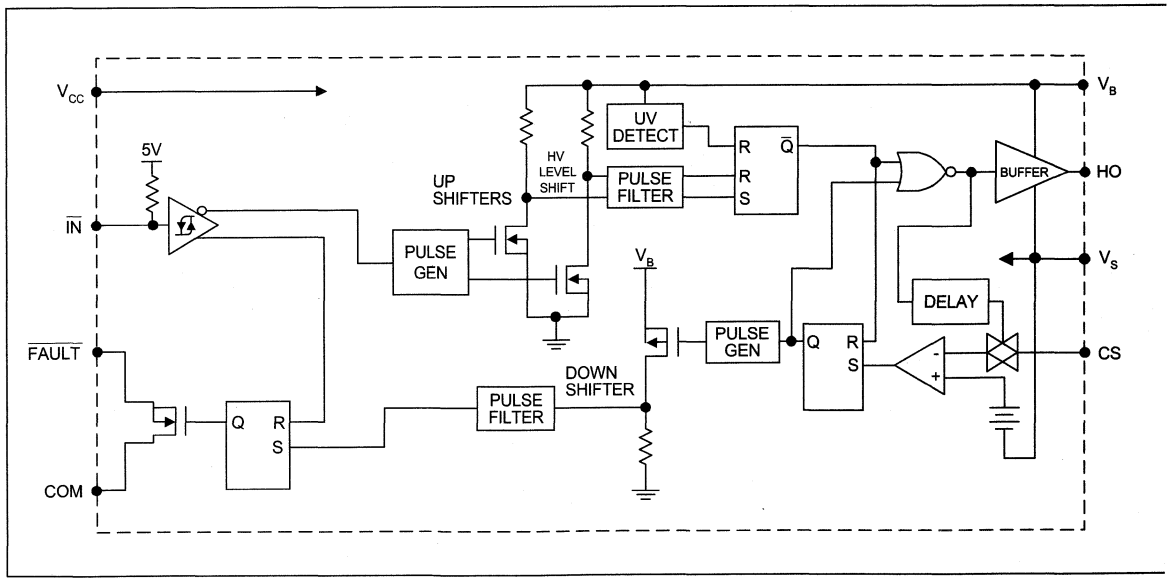
V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage Logic "0" Input Voltage	(IR2127/IR21271) (IR2128)	3.0	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" Input Voltage Logic "1" Input Voltage	(IR2127/IR21271) (IR2128)	—	—	0.8		
V_{CSTH+}	CS Input Positive	(IR2127/IR2128)	180	250	320	mV	
	Going Threshold	(IR21271)	—	1.8	—	V	
V_{OH}	High Level Output Voltage, V_{BIAS} - VO		—	—	100	mV	IO = 0A
V_{OL}	Low Level Output Voltage, VO		—	—	100		IO = 0A
I_{LK}	Offset Supply Leakage Current		—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current		—	200	400		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current		—	60	120		
I_{IN+}	Logic "1" Input Bias Current		—	7.0	15		V_{IN} = 5V
I_{IN-}	Logic "0" Input Bias Current		—	—	1.0		V_{IN} = 0V
I_{CS+}	"High" CS Bias Current		—	—	1.0		V_{CS} = 3V
I_{CS-}	"High" CS Bias Current		—	—	1.0		V_{CS} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	(IR2127/IR2128) (IR21271)	8.8 6.3	10.3 7.2	11.8 8.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	(IR2127/IR2128) (IR21271)	7.5 6.0	9.0 6.8	10.6 7.7		
I_{O+}	Output High Short Circuit Pulsed Current		200	250	—	mA	V_O = 0V, V_{IN} = 5V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current		420	500	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs
Ron, FLT	FAULT - Low on Resistance		—	125	—	Ω	

Functional Block Diagram IR2127/IR21271



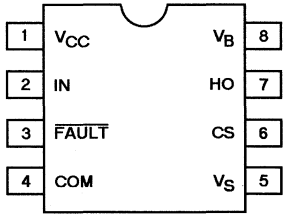
Functional Block Diagram IR2128



Lead Definitions

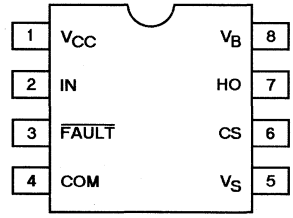
Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2127/IR21271) out of phase with HO (IR2128)
$\overline{FAULT}$	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



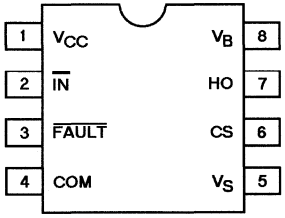
8 Lead PDIP

IR2127/IR21271



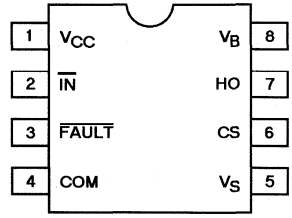
8 Lead SOIC

IR2127S/IR21271S



8 Lead PDIP

IR2128



8 Lead SOIC

IR2128S

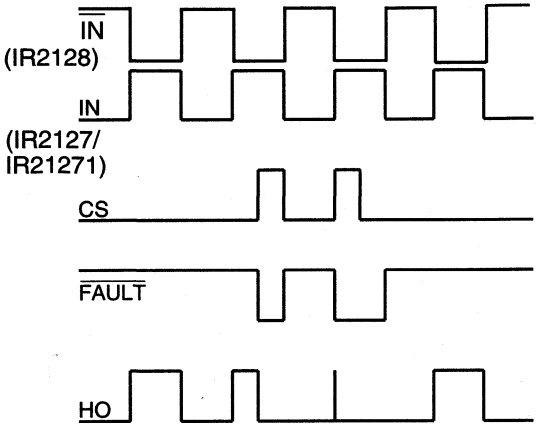


Figure 1. Input/Output Timing Diagram

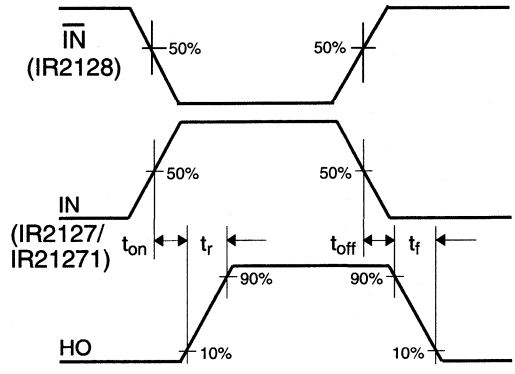


Figure 2. Switching Time Waveform Definition

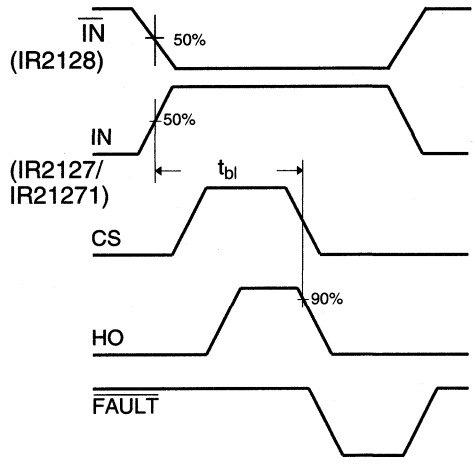


Figure 3. Start-up Blanking Time Waveform Definitions

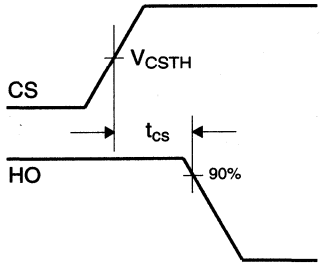


Figure 4. CS Shutdown Waveform Definitions

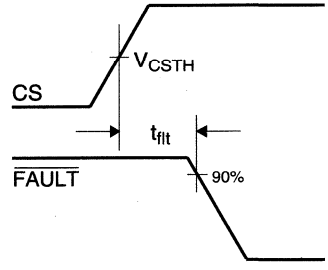


Figure 5. CS to $\overline{\text{FAULT}}$ Waveform Definitions

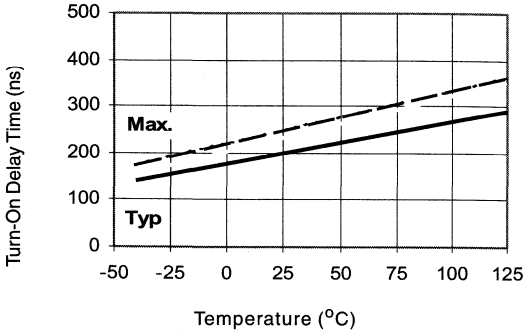


Figure 10A Turn-On Time vs. Temperature

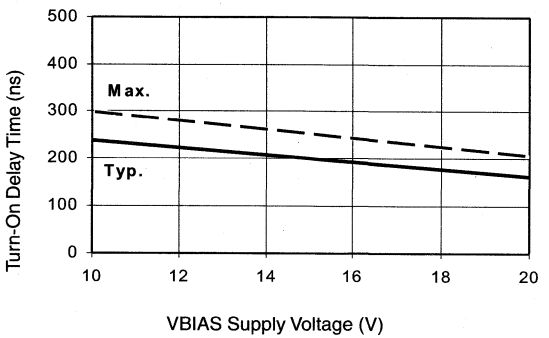


Figure 10B Turn-On Time vs. Voltage

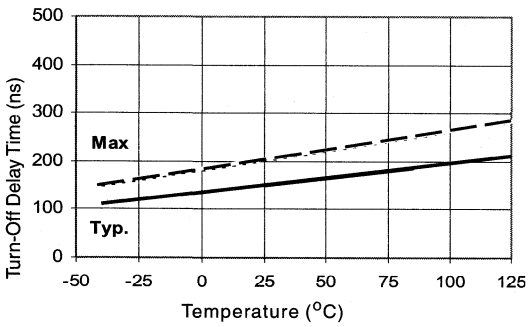


Figure 11A Turn-Off Time vs. Temperature

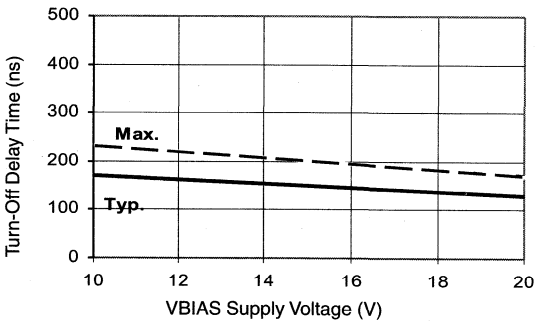


Figure 11B Turn-Off Time vs. Voltage

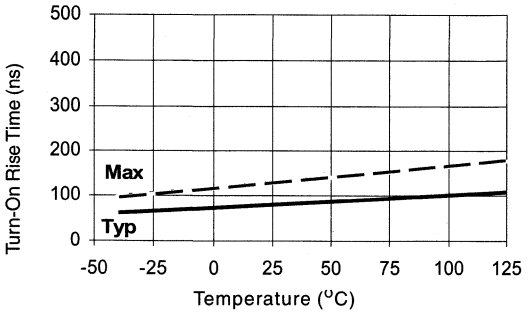


Figure 12A Turn-On Rise Time vs. Temperature

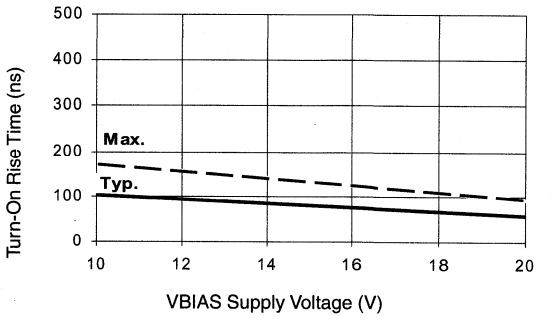


Figure 12B Turn-On Rise Time vs. Voltage

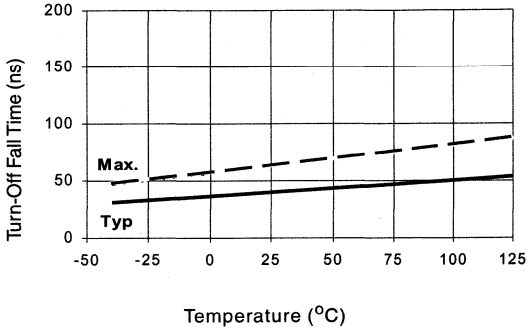


Figure 13A Turn-Off Fall Time vs. Temperature

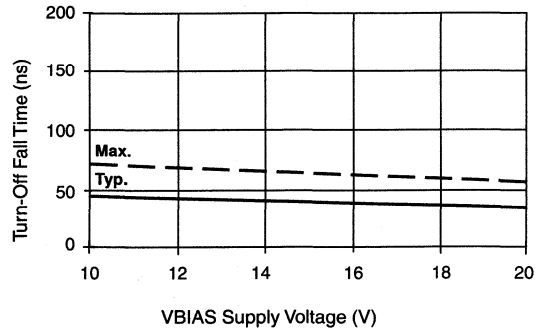


Figure 13B Turn-Off Fall Time vs. Voltage

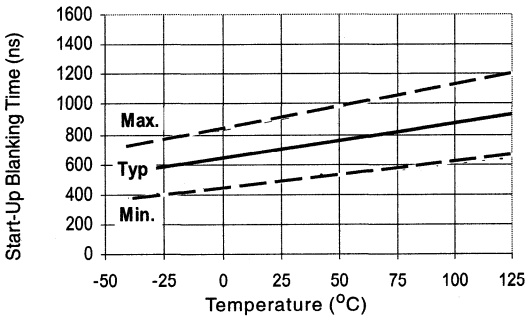


Figure 14A Start-Up Blanking Time vs. Temperature

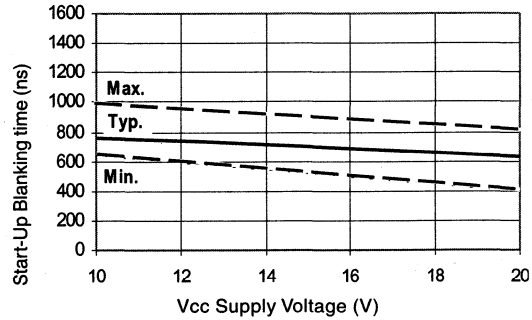


Figure 14B Start-Up Blanking Time vs Voltage

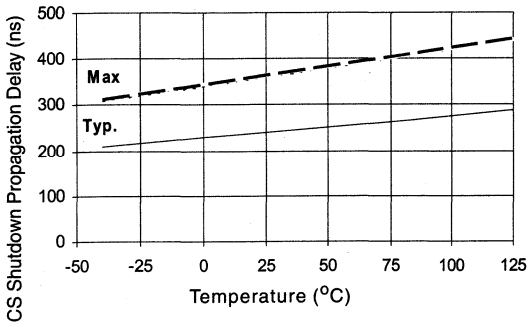


Figure 15A CS Shutdown Propagation Delay vs. Temperature

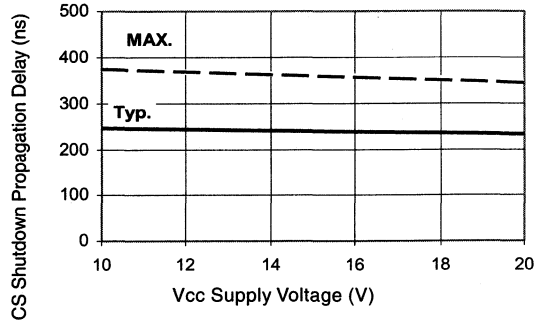


Figure 15B CS Shutdown Propagation Delay vs. Voltage

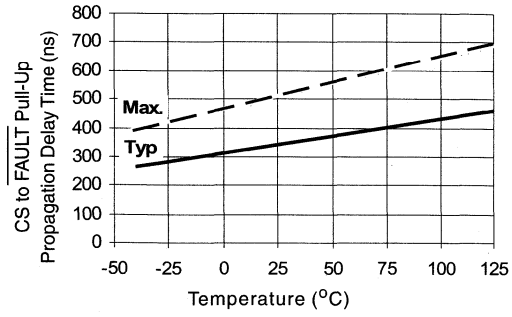


Figure 16A CS to $\overline{\text{FAULT}}$ Pull-Up Propagation Delay vs. Temperature

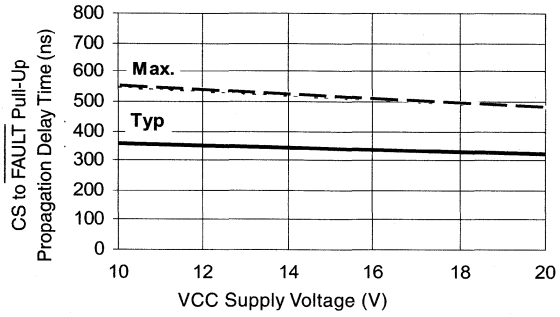


Figure 16B CS to $\overline{\text{FAULT}}$ Pull-Up Propagation Delay vs. Voltage

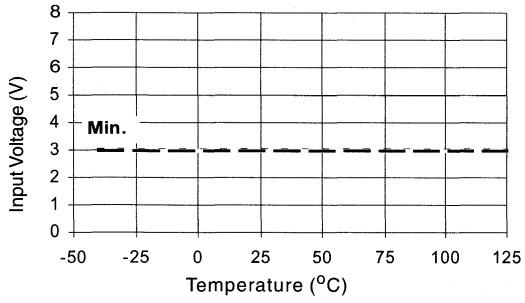


**Figure 17A Logic "1" Input Voltage (IR2127)
Logic "0" Input Voltage (IR2128)
vs Temperature**

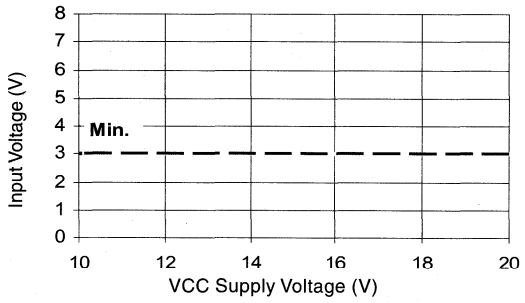


**Figure 17B Logic "1" Input Voltage (IR2127)
Logic "0" Input Voltage (IR2128)
vs Voltage**

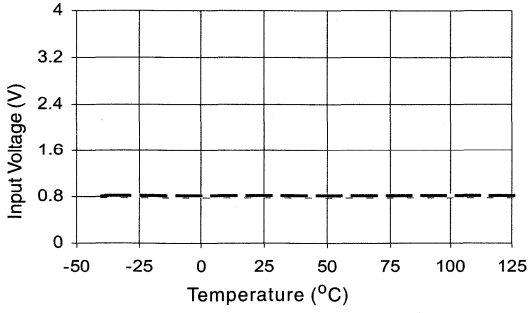


**Figure 18A Logic "0" Input Voltage (IR2127)
Logic "1" Input Voltage (IR2128)
vs Temperature**

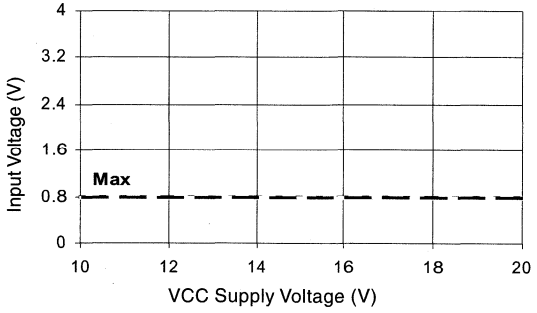


**Figure 18B Logic "0" Input Voltage (IR2127)
Logic "1" Input Voltage (IR2128)
vs Voltage**

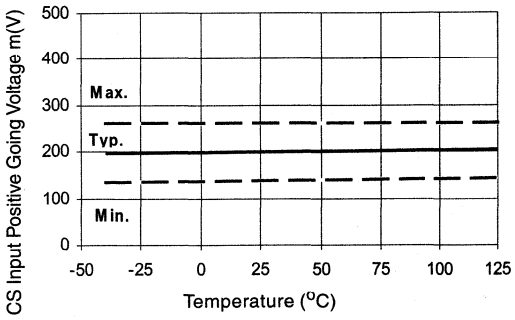


Figure 19A CS Input Positive Going Voltage vs Temperature (IR2127/IR2128)

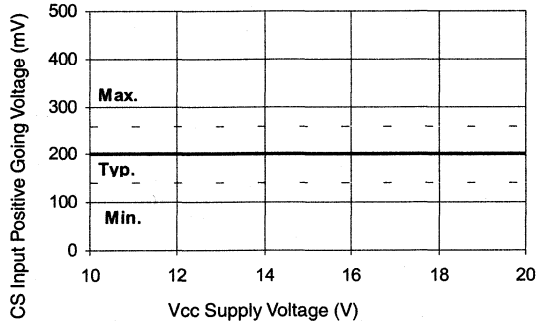


Figure 19B CS Input Positive Going Voltage vs Voltage (IR2127/IR2128)

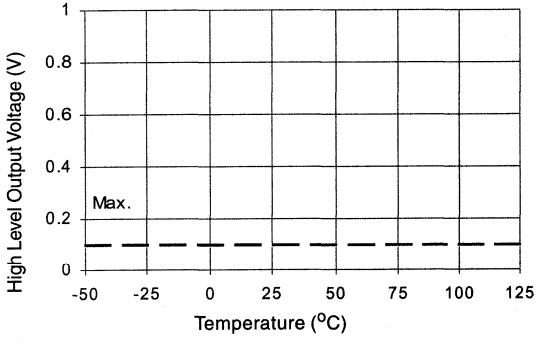


Figure 20A High Level Output vs Temperature

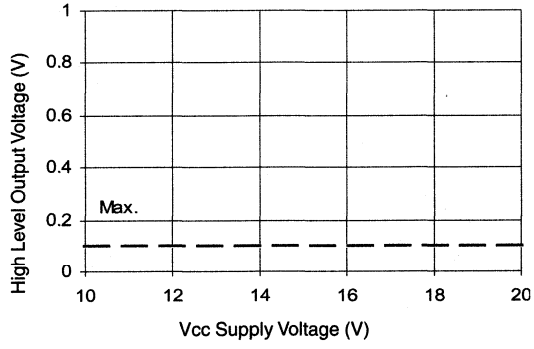


Figure 20B High Level Output vs Voltage

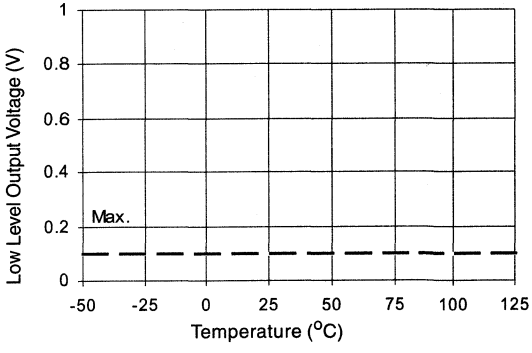


Figure 21A Low Level Output vs Temperature

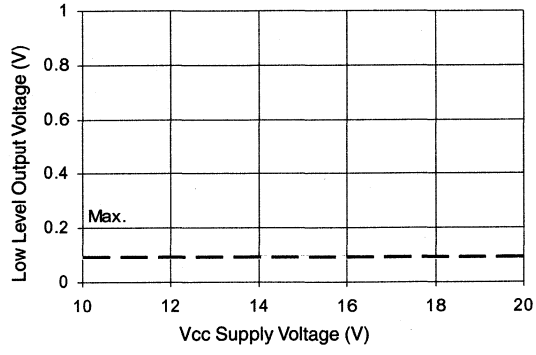


Figure 21B Low Level Output vs Voltage

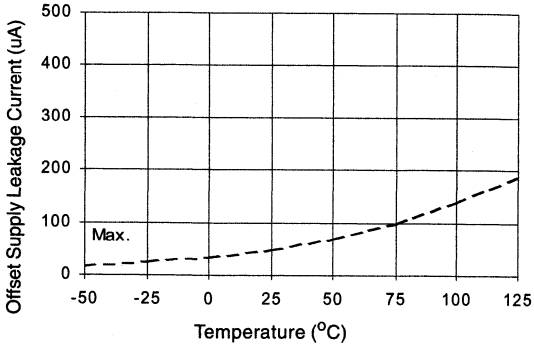


Figure 22A Offset Supply Current vs Temperature

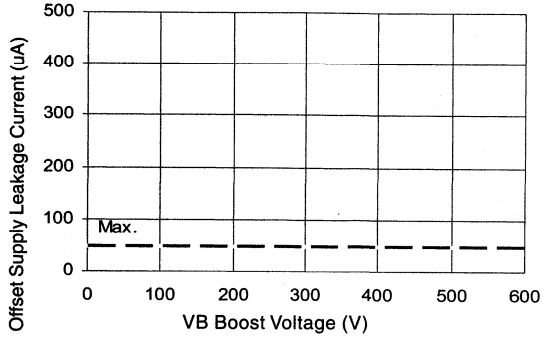


Figure 22B Offset Supply Current vs Voltage

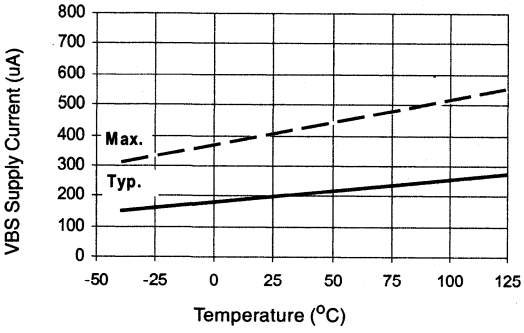


Figure 23A VBS Supply Current vs Temperature

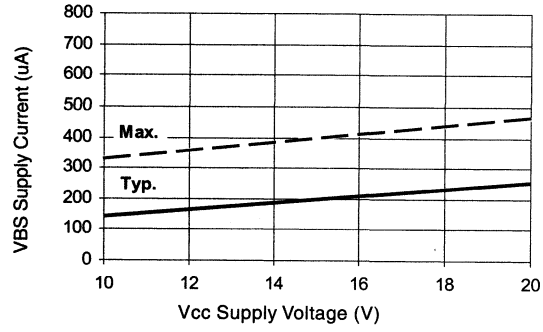


Figure 23B VBS Supply Current vs Voltage

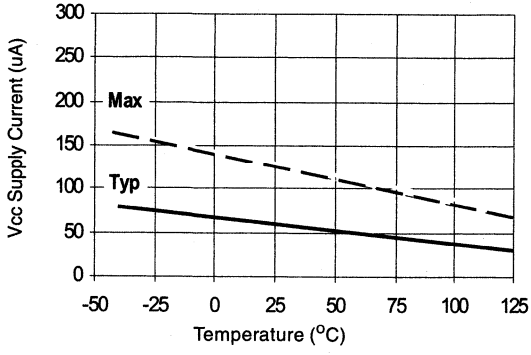


Figure 24A Vcc Supply Current vs Temperature

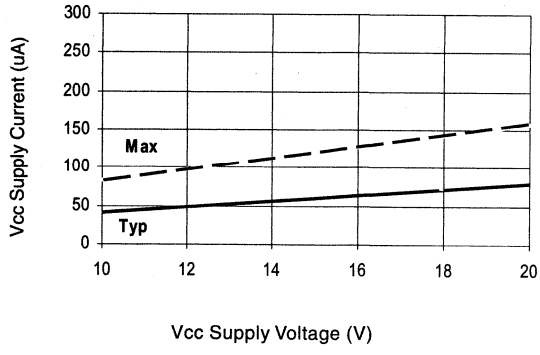


Figure 24B Vcc Supply Current vs Voltage

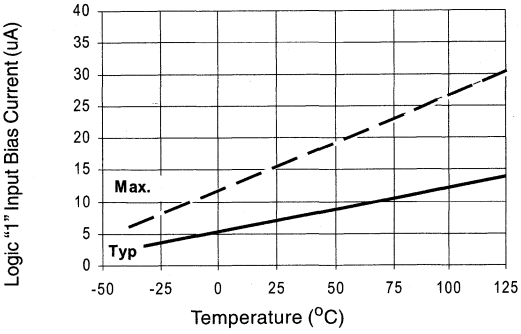


Figure 25A Logic "1" Input Current vs Temperature

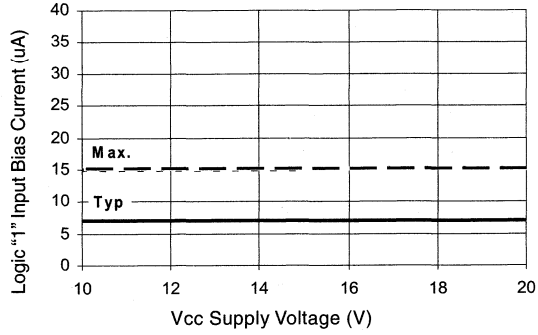


Figure 25B Logic "1" Input Current vs Voltage

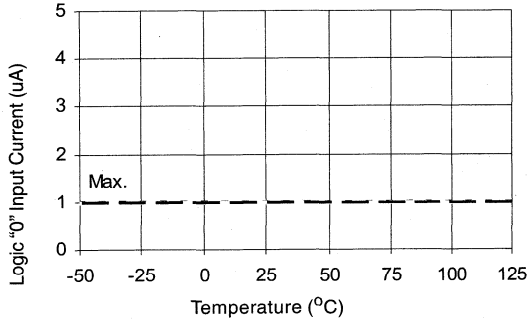


Figure 26A Logic "0" Input Current vs Temperature

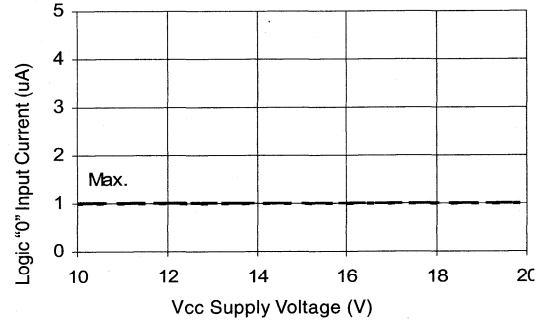


Figure 26B Logic "0" Input Current vs Voltage

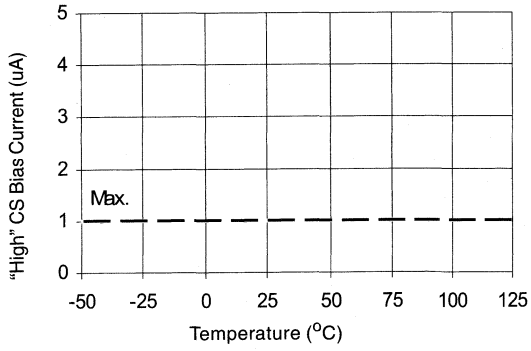


Figure 27A "High" CS Bias Current vs Temperature

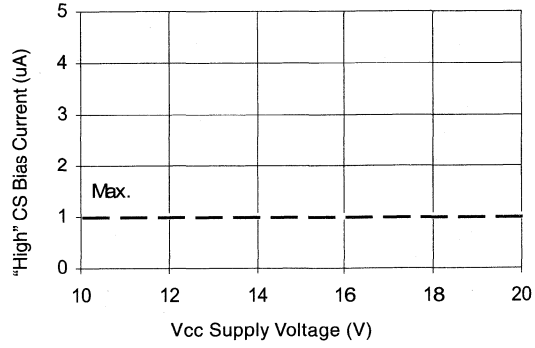


Figure 27B "High" CS Bias Current vs Voltage

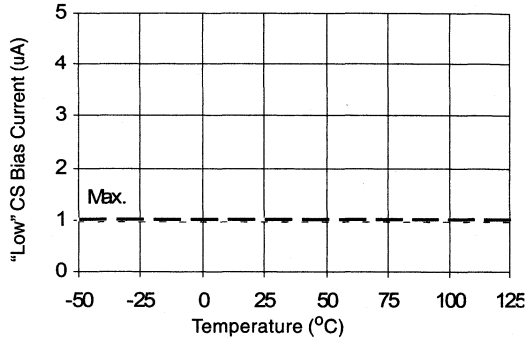


Figure 28A "Low" CS Bias Current vs Temperature

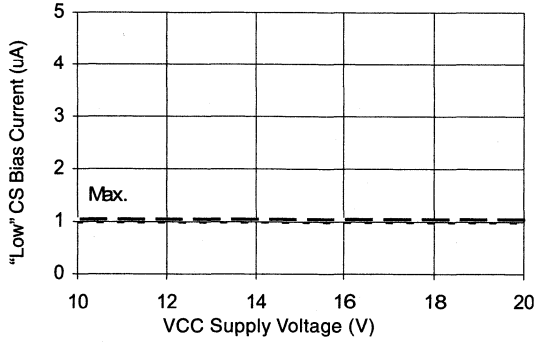


Figure 28B "Low" CS Bias Current vs Voltage

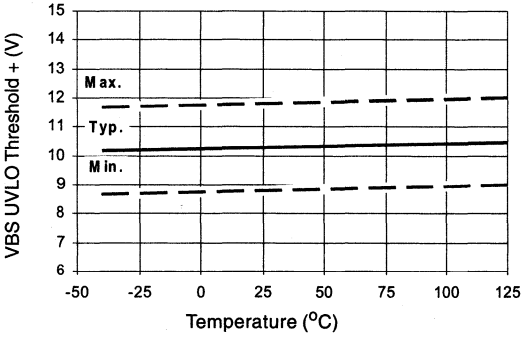


Figure 29A VBS Undervoltage Threshold (+) vs Temperature (IR2127/IR2128)

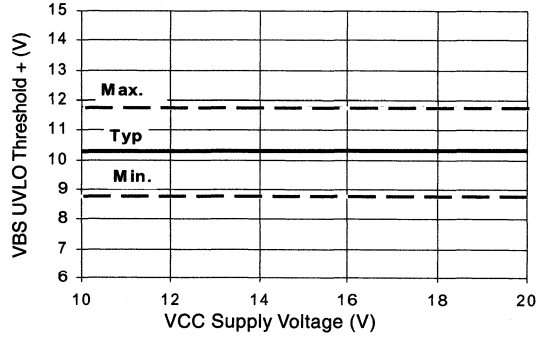


Figure 29B VBS Undervoltage Threshold (+) vs Voltage (IR2127/IR2128)

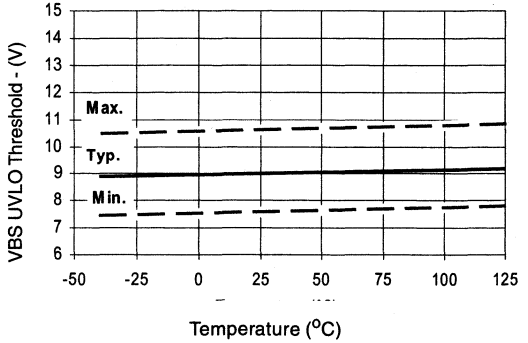


Figure 30A VBS Undervoltage Threshold (-) vs Temperature (IR2127/IR2128)

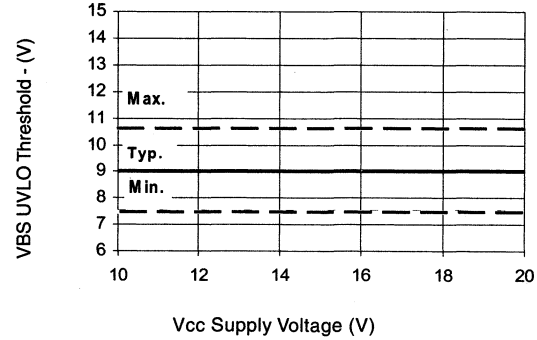


Figure 30B VBS Undervoltage Threshold (-) vs Voltage (IR2127/IR2128)

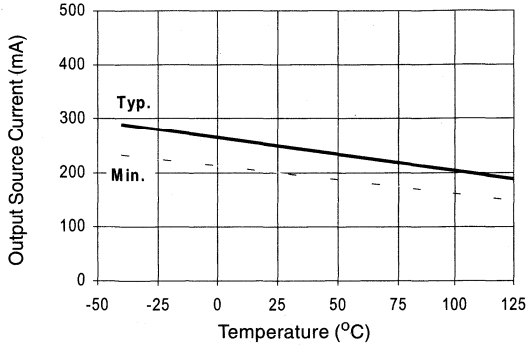


Figure 31A Output Source Current vs Temperature

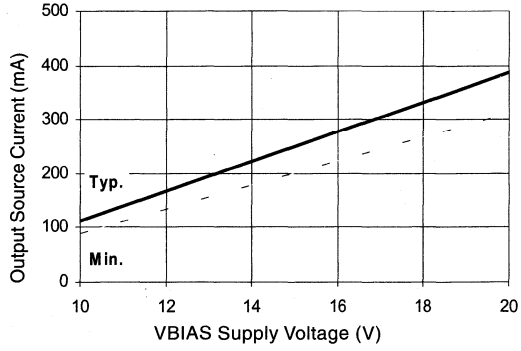


Figure 31B Output Source Current vs Voltage

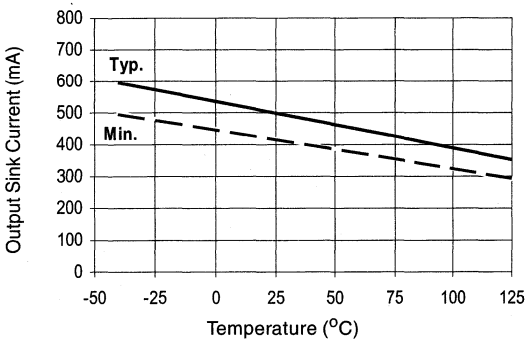


Figure 32A Output Sink Current vs Temperature

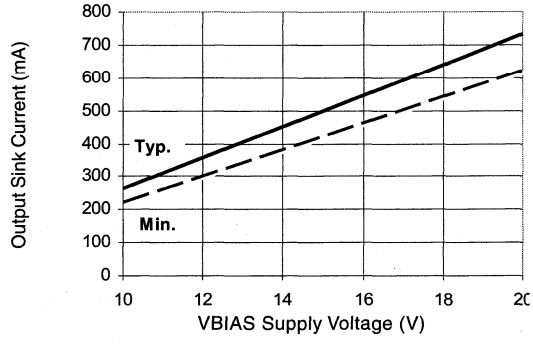
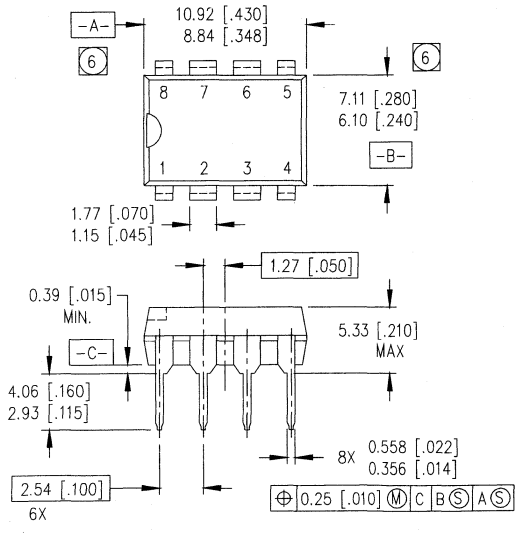


Figure 32B Output Sink Current vs Voltage

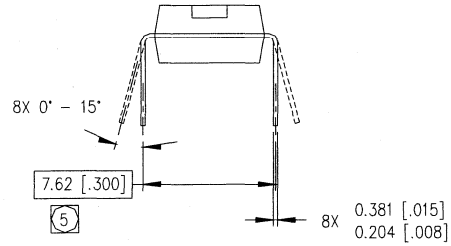


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

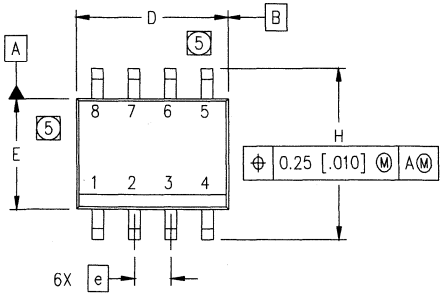
(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

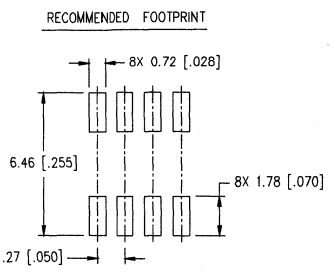


8 Lead PDIP

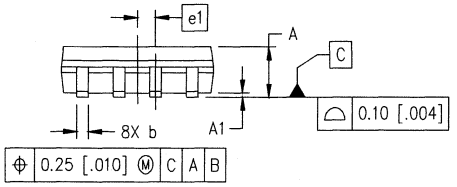
01-3003 01

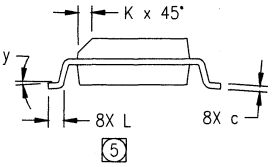
Case Outline - 8 Lead SOIC





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°





NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

IR2181/IR21814

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IR2181/IR21814)

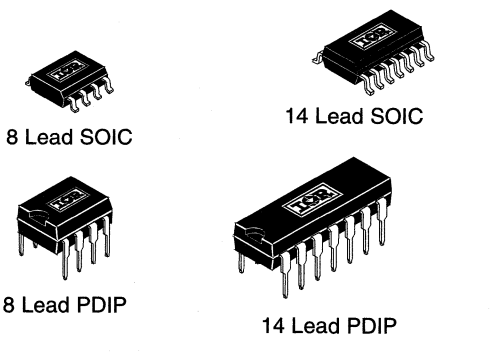
Product Summary

V_{OFFSET}	600V max.
$I_{O+/-}$	1.7 A / 1.7 A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	180 ns
Delay matching	50 ns

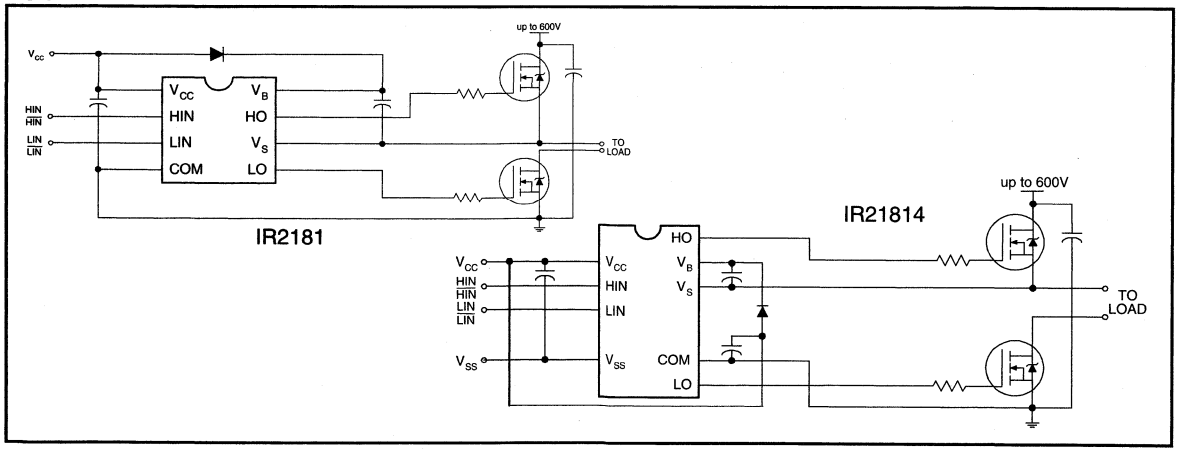
Description

The IR2181/IR21814 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages



Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21814 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21814/IR21824 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

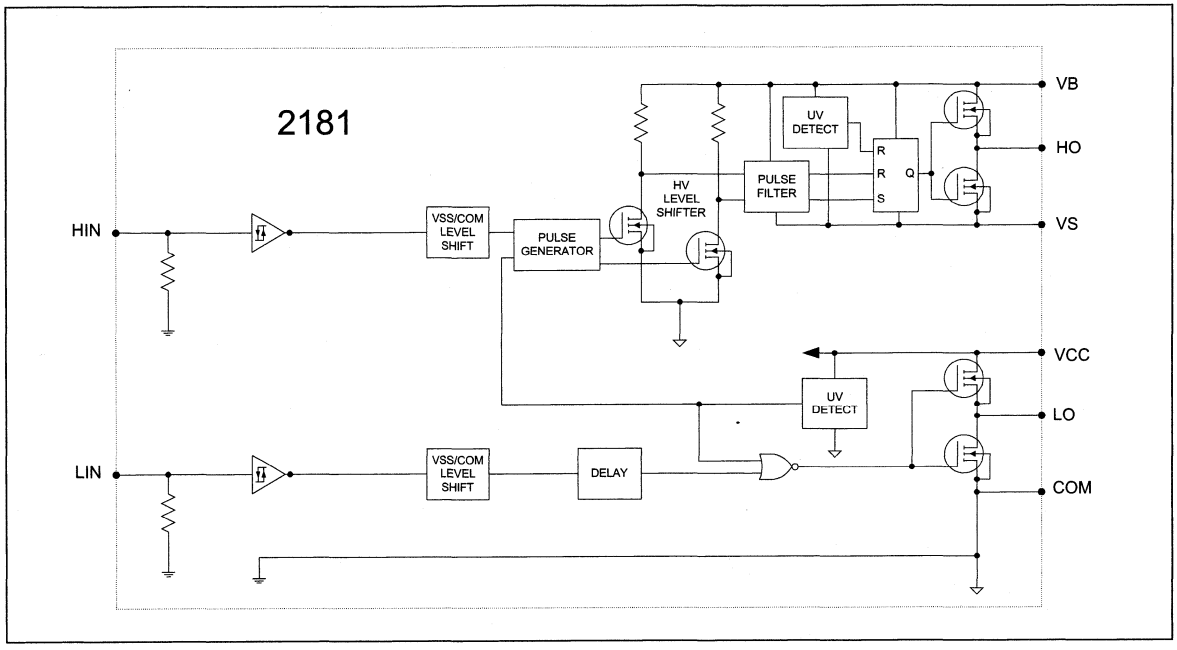
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	170	250		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	40	60		V_S = 0V
t_f	Turn-off fall time	—	20	30		V_S = 0V

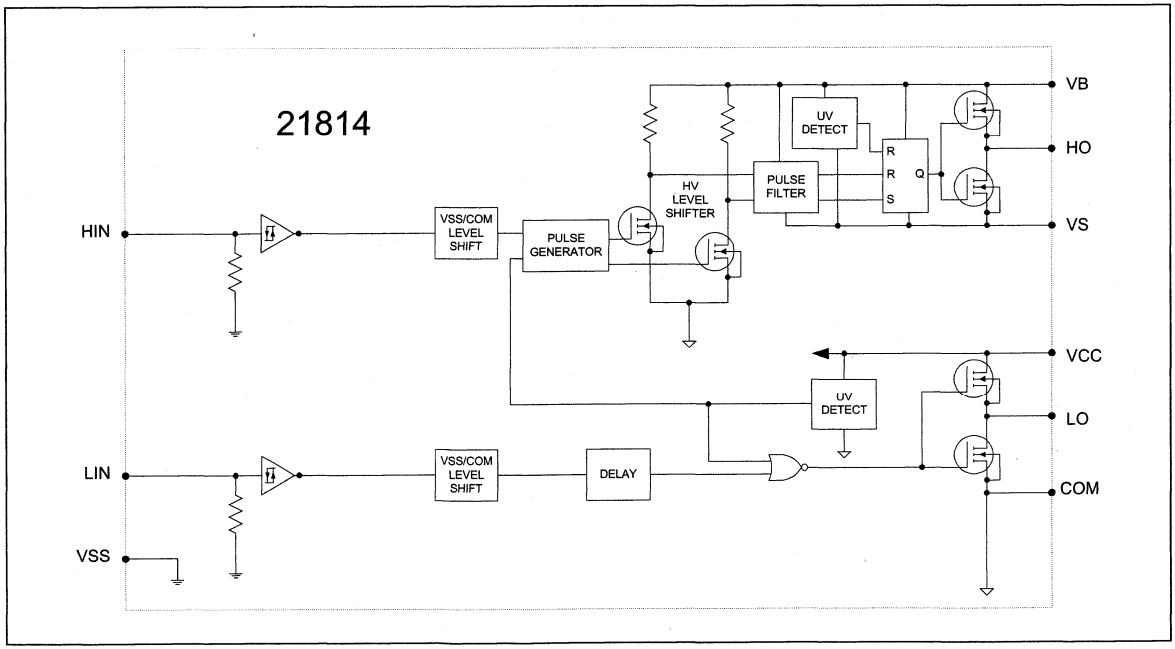
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and LIN (IR2181/IR21814) and $\overline{HIN}$ and $\overline{LIN}$ (IR2182/IR21824). The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage (IR2181/IR21814)	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage (IR2181/IR21814)	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current	—	20	40		V_{IN} = 5V (IR2181(4))
I_{IN-}	Logic "0" input bias current	—	—	1.0	V	V_{IN} = 0V (IR2181(4))
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.7	2	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.7	2	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagram

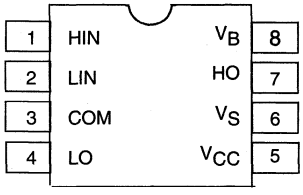




Lead Definitions

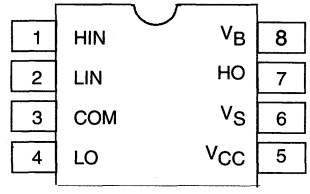
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2181/IR21814)
LIN	Logic input for low side gate driver output (LO), in phase (IR2181/IR21814)
VSS	Logic Ground (IR21814 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



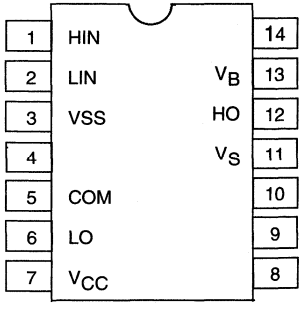
8 Lead PDIP

IR2181



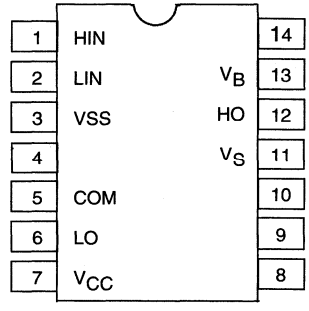
8 Lead SOIC

IR2181S



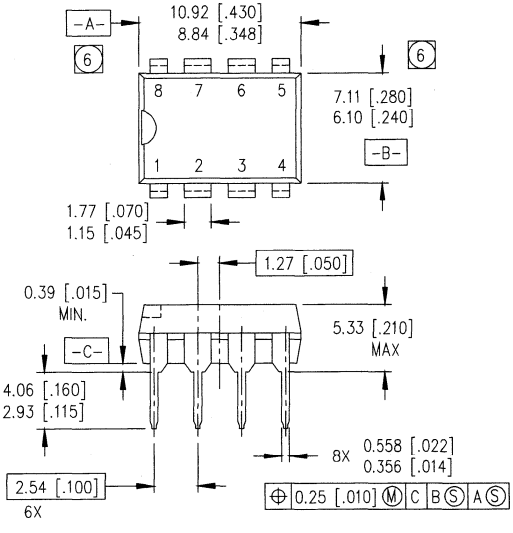
14 Lead PDIP

IR21814



14 Lead SOIC

IR21814S

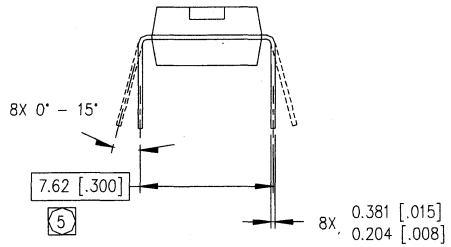


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.

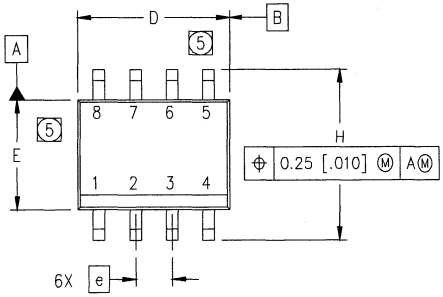
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

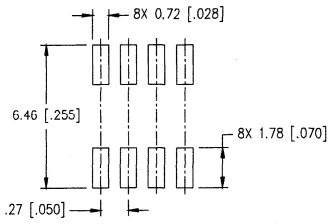


8 Lead PDIP

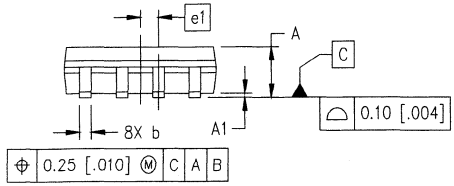
01-3003 01

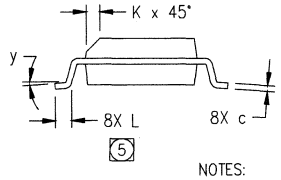


RECOMMENDED FOOTPRINT



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°





NOTES:

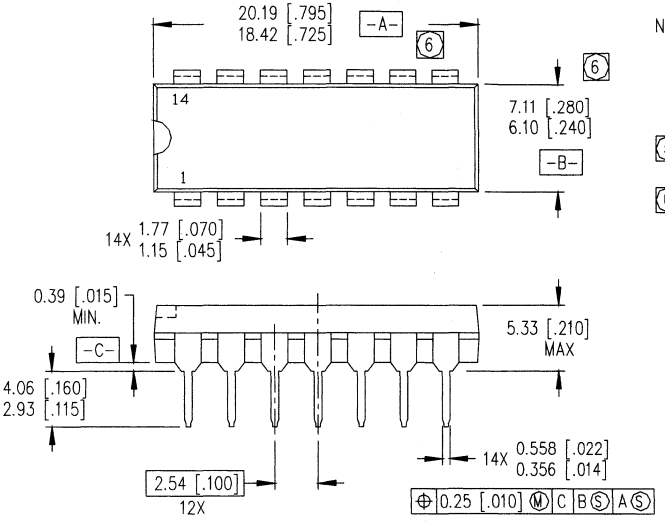
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

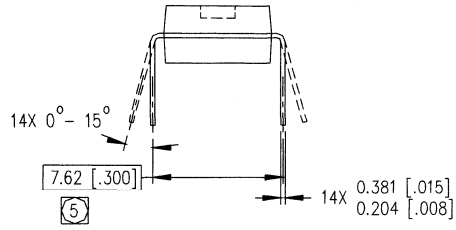
(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

8 Lead SOIC

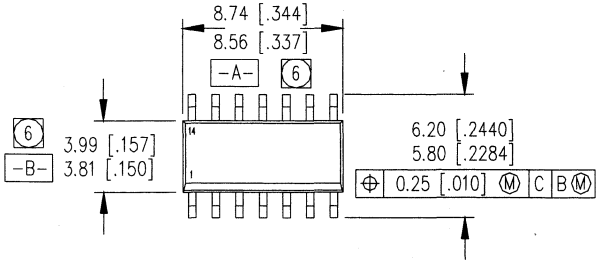


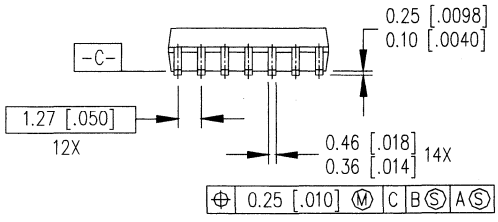
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



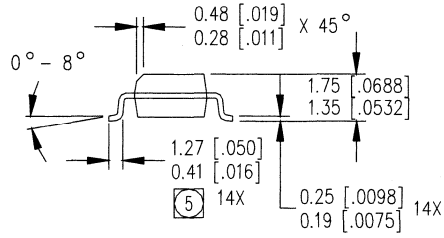
14 Lead PDIP

01-3002 03





NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

01-3063 00

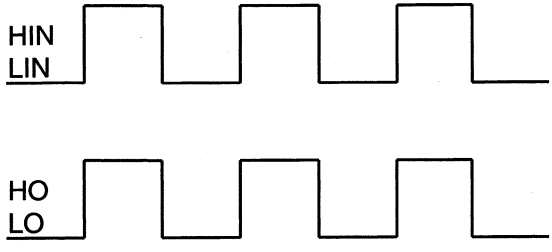


Figure 1. Input/Output Timing Diagram

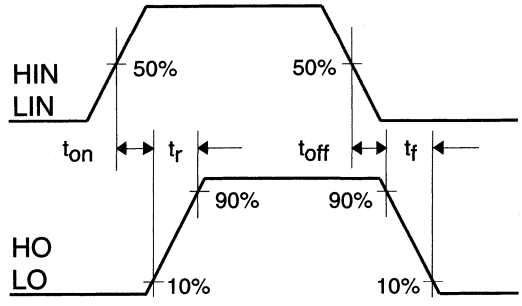


Figure 2. Switching Time Waveform Definitions

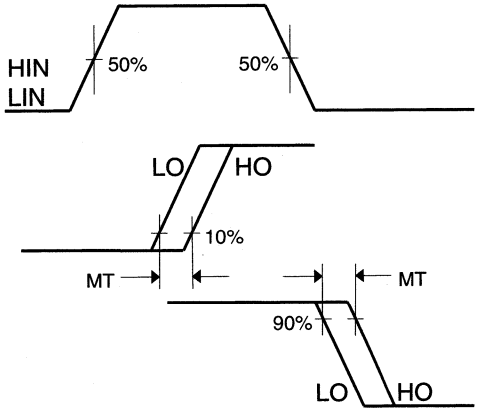


Figure 3. Delay Matching Waveform Definitions

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Preliminary Data Sheet No. PD-60173-A

IR2183/IR21834

HIGH AND LOW SIDE DRIVER

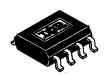
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with HIN input
- Low side output out of phase with $\overline{\text{LIN}}$ input
- Logic and power ground +/- 5V offset.
- Internal 500ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21834)
- Lower di/dt gate driver for better noise immunity

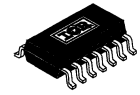
Product Summary

V_{OFFSET}	600V max.
I_{O}+/-	1.7A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	180 ns
Deadtime (typ.)	500 ns
(programmable up to 5uS for IR21834)	

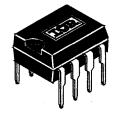
Packages



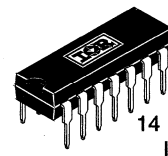
8 Lead SOIC
IR2183S



14 Lead SOIC
IR21834S



8 Lead PDIP
IR2183

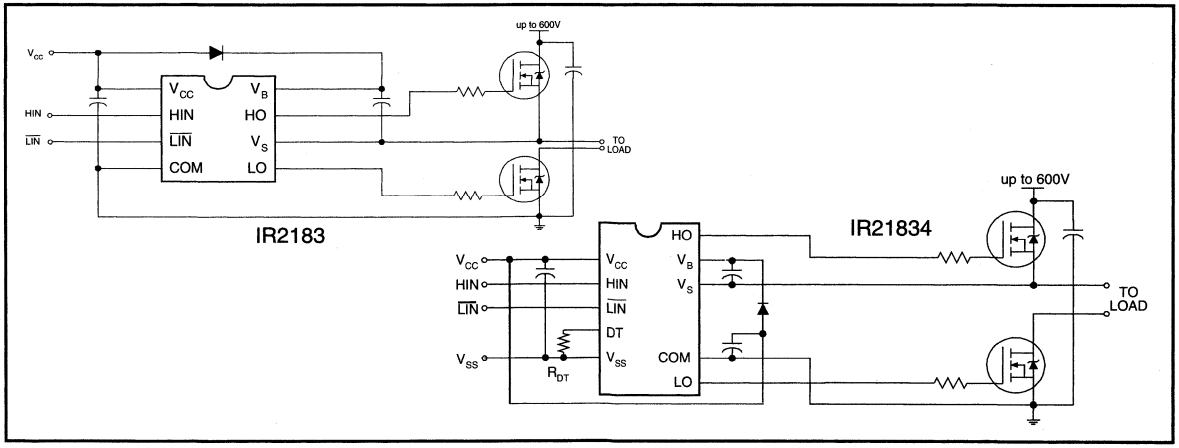


14 Lead PDIP
IR21834

Description

The IR2183/IR21834 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21384 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21834 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	V_{SS}	V_{CC}	
DT	Programmable dead-time pin voltage (IR21834 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21834 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

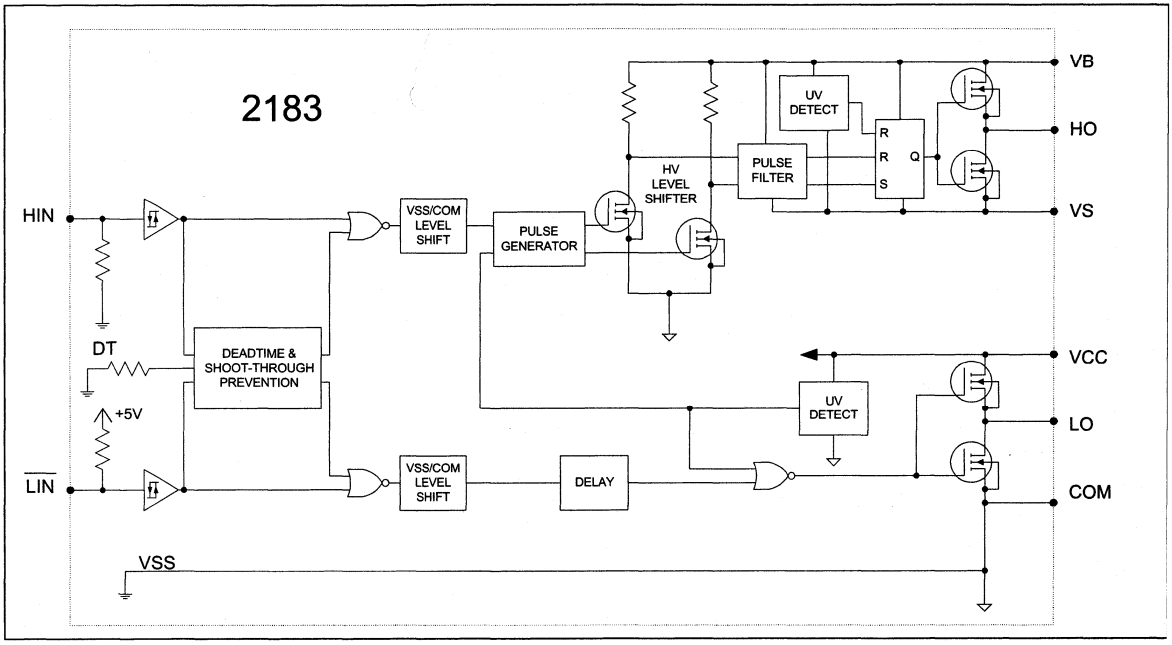
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	170	250		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	40	60		V_S = 0V
t_f	Turn-off fall time	—	20	30		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO})	380	500	620		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	usec	RDT = 200k (IR21834)
MDT	Deadtime matching = DT_{LO-HO} - DT_{HO-LO}	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21834)

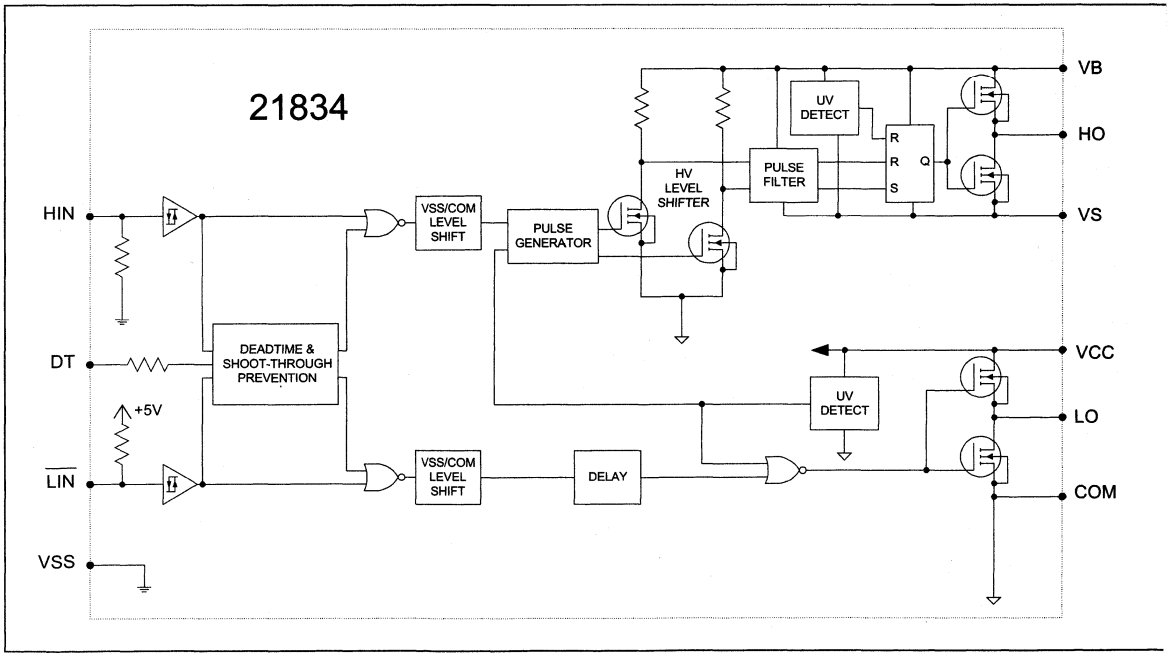
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and $\overline{LIN}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HIN & logic "0" for $\overline{LIN}$	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage for HIN & logic "1" for $\overline{LIN}$	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current	—	5	20	µA	HIN = 5V, $\overline{LIN}$ = 0V
I_{IN-}	Logic "0" input bias current	—	1	2		HIN = 0V, $\overline{LIN}$ = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.7	2	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.7	2	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagram

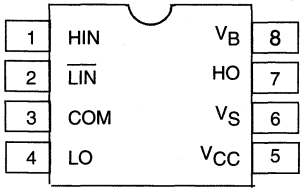




Lead Definitions

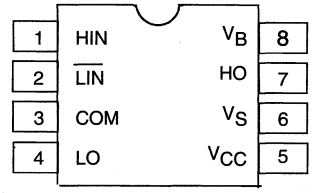
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (referenced to COM for IR2183 and VSS for IR21834)
$\overline{LIN}$	Logic input for low side gate driver output (LO), out of phase (referenced to COM for IR2183 and VSS for IR21834)
DT	Programmable dead-time lead, referenced to VSS. (IR21834 only)
VSS	Logic Ground (21834 only)
V_B	High side floating supply
HO	High side gate driver output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

Lead Assignments



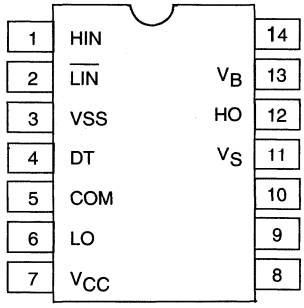
8 Lead PDIP

IR2183



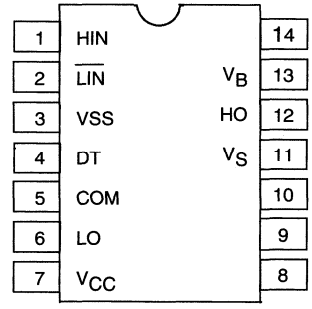
8 Lead SOIC

IR2183S



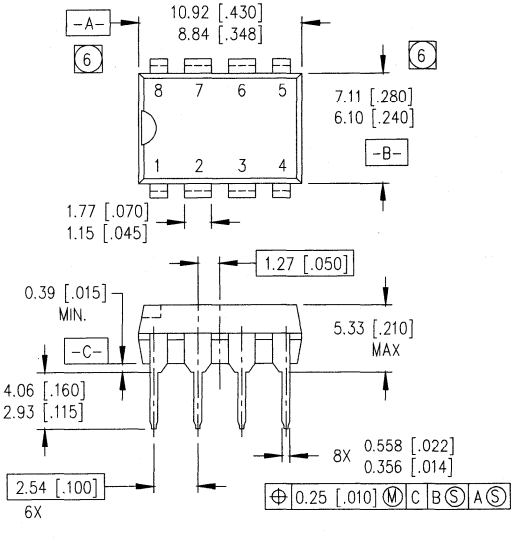
14 Lead PDIP

IR21834



14 Lead SOIC

IR21834S

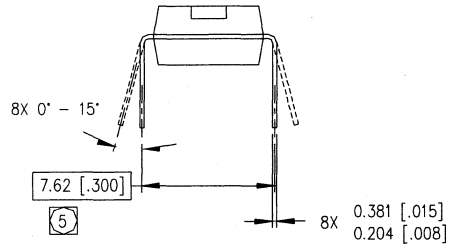


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

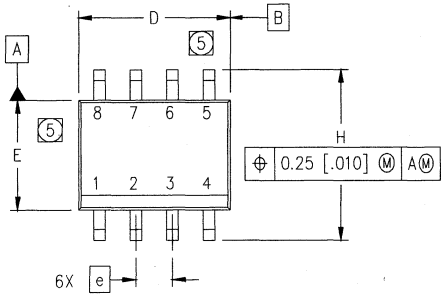
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

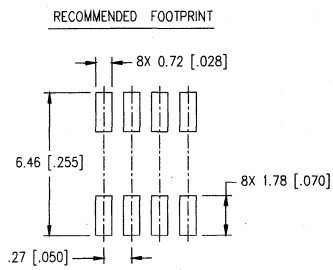
(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



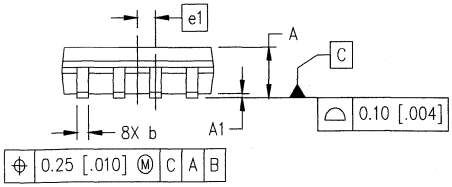
8 Lead PDIP

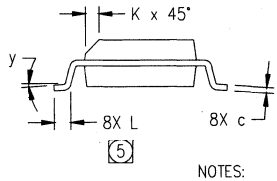
01-3003 01





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°





NOTES:

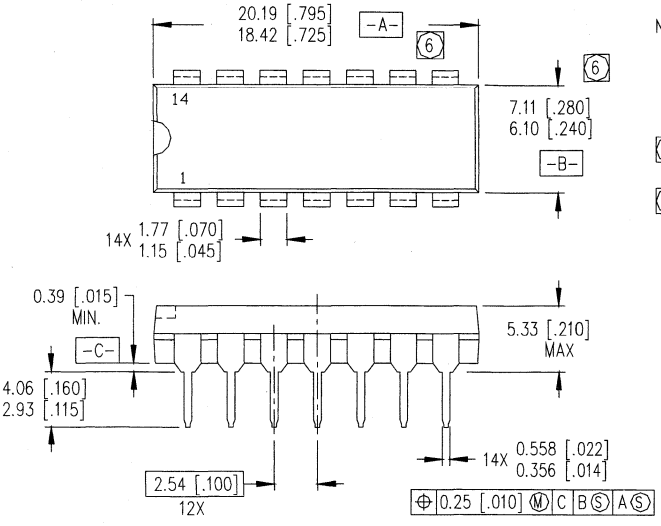
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

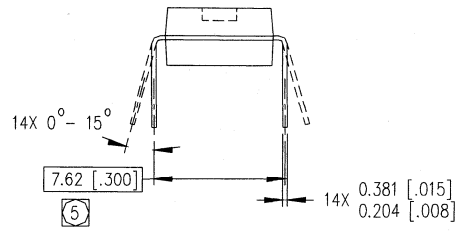
(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

8 Lead SOIC

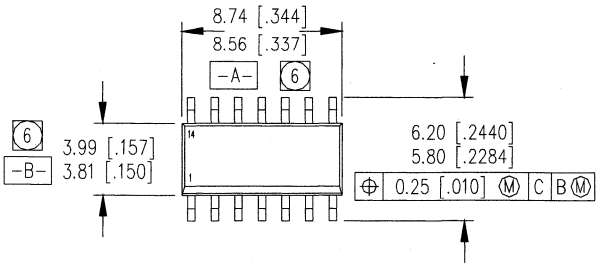


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

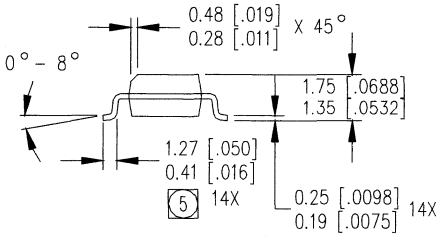


14 Lead PDIP

01-3002 03



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

01-3063 00

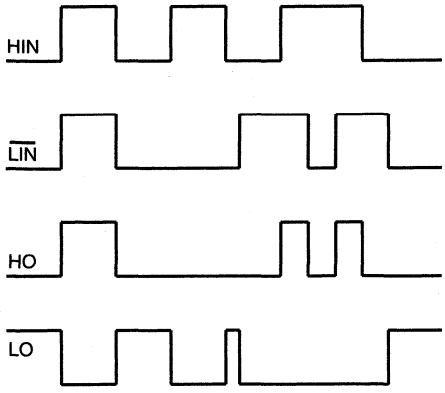


Figure 1. Input/Output Timing Diagram

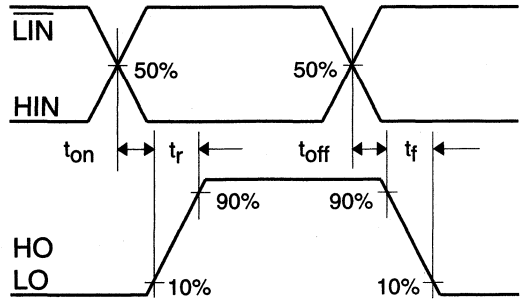


Figure 2. Switching Time Waveform Definitions

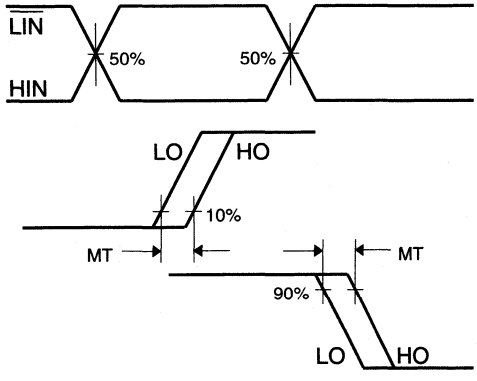


Figure 3. Delay Matching Waveform Definitions

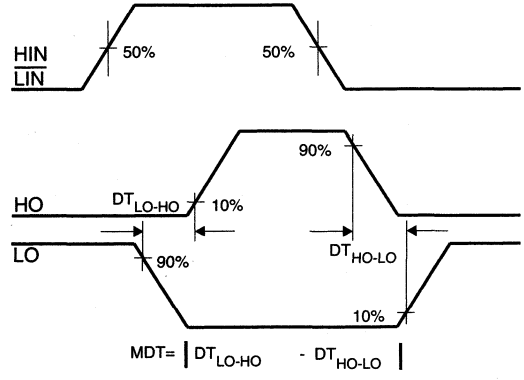


Figure 4. Deadtime Waveform Definitions

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Preliminary Data Sheet No. PD-60174-A

IR2184/IR21844

HIGH AND LOW SIDE DRIVER

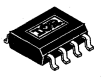
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 500ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21844)
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels.

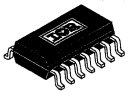
Product Summary

V_{OFFSET}	600V max.
I_O+/-	1.7A / 1.7A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	680 & 180 ns
Deadtime (typ.)	500 ns
(programmable up to 5uS for IR21844)	

Packages

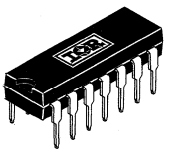


8 Lead SOIC
IR2184S



14 Lead SOIC
IR21844S

8 Lead PDIP
IR2184

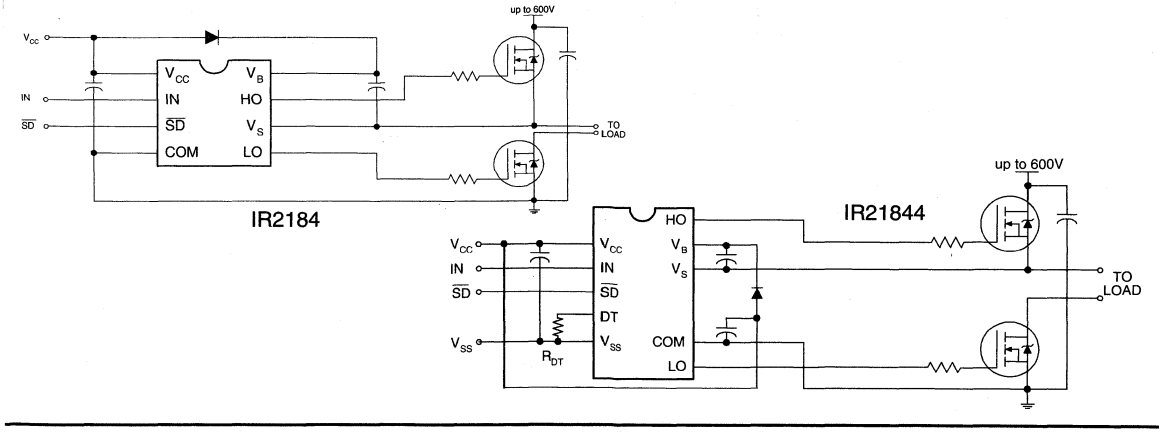


14 Lead PDIP - IR21844

Description

The IR2184/IR21844 are high voltage, high speed power MOSFET and IGBT drivers with dependant high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21844 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21844 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	V_{SS}	V_{CC}	
DT	Programmable dead-time pin voltage (IR21844 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21844 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

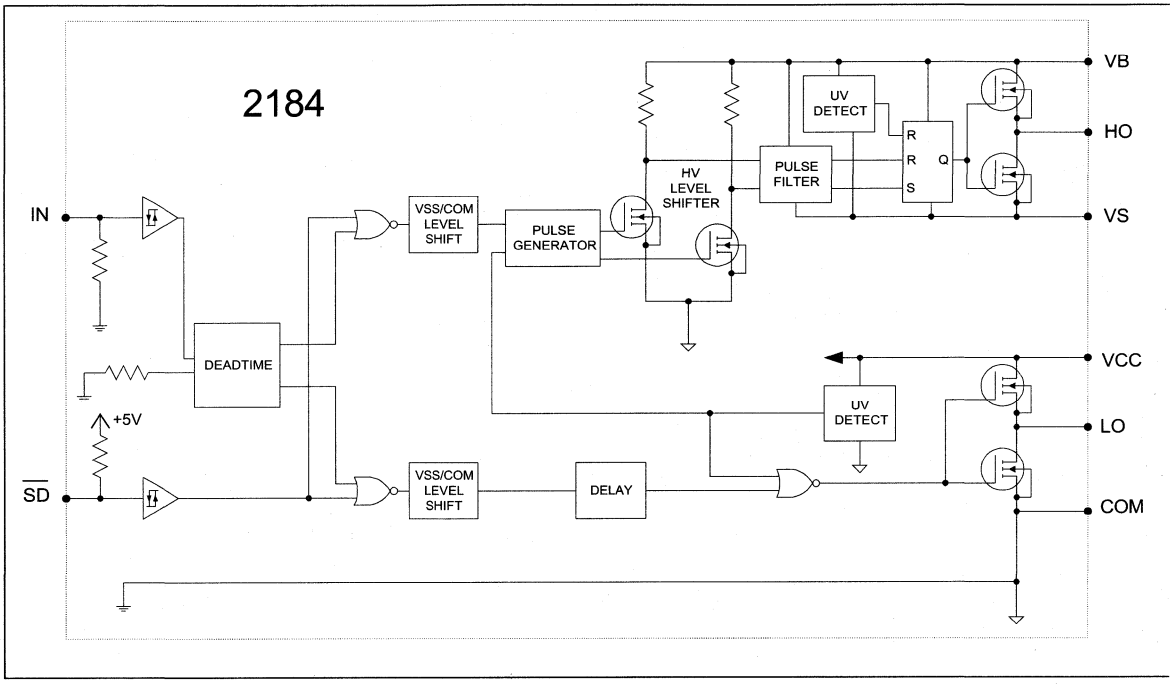
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	900	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	170	250		V_S = 0V or 600V
t_{sd}	Shut-down propagation delay	—	180	270		
MT	Delay matching, HS & LS turn-on/off	—	0	—		
t_r	Turn-on rise time	—	40	60		V_S = 0V
t_f	Turn-off fall time	—	20	30		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO})	380	500	620		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	usec	RDT = 200k (IR21094)
MDT	Deadtime matching = $DT_{LO - HO}$ - DT_{HO-LO}	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21094)

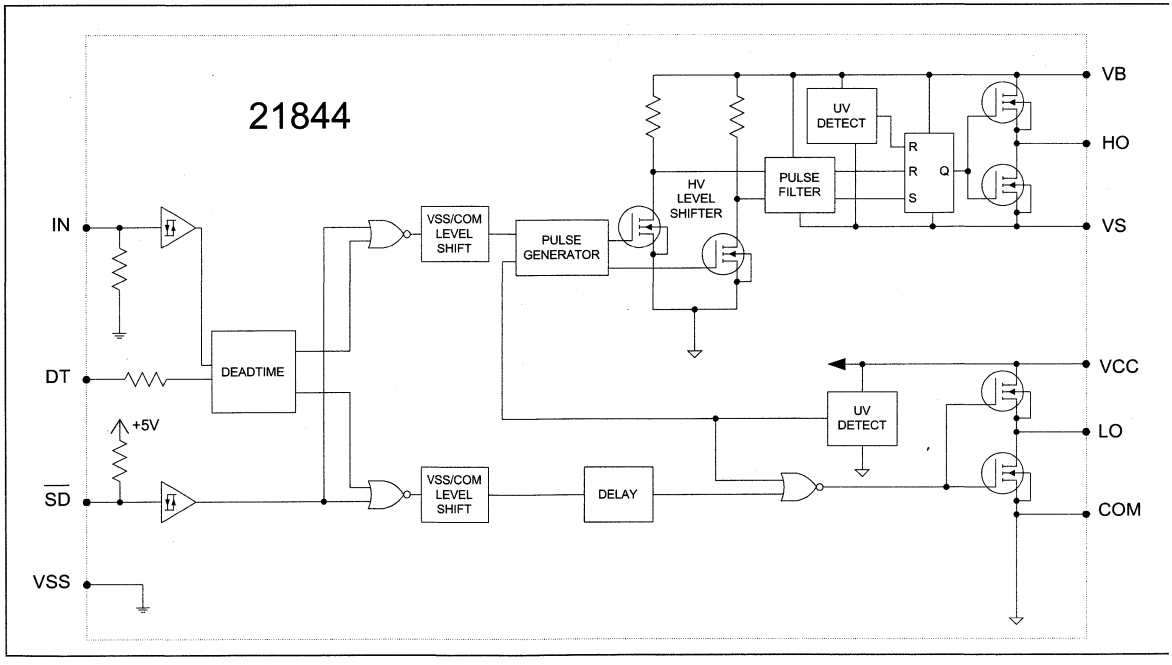
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and SD. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.7	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current	—	5	20	µA	IN = 5V, $\overline{SD}$ = 0V
I_{IN-}	Logic "0" input bias current	—	1	2		IN = 0V, $\overline{SD}$ = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} dupply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed vurrent	1.7	2	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.7	2	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagram

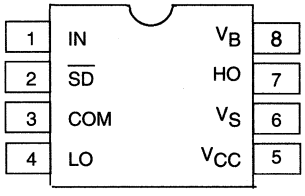




Lead Definitions

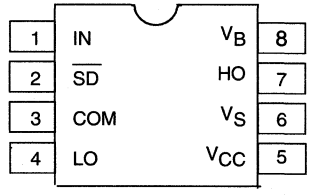
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2184 and VSS for IR21844)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IR2184 and VSS for IR21844)
DT	Programmable dead-time lead, referenced to VSS. (IR21844 only)
VSS	Logic Ground (21844 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



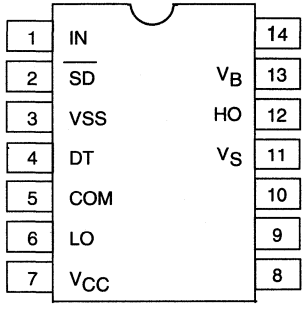
8 Lead PDIP

IR2184



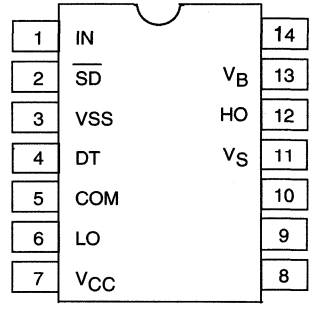
8 Lead SOIC

IR2184S



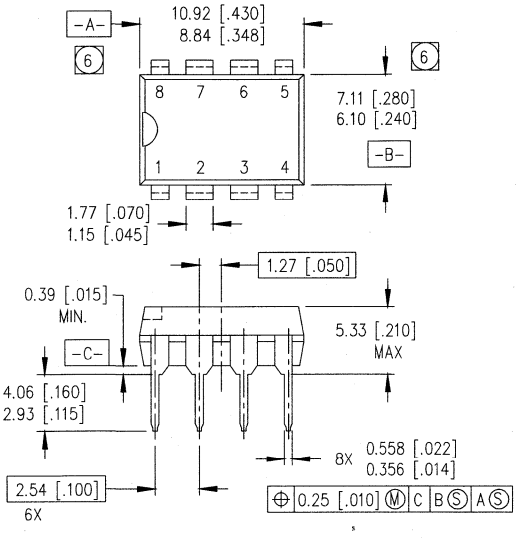
14 Lead PDIP

IR21844



14 Lead SOIC

IR21844S

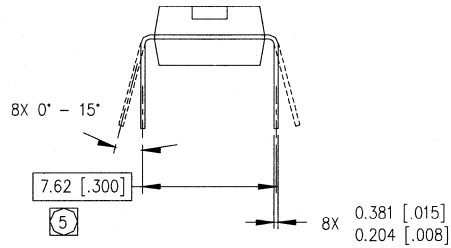


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

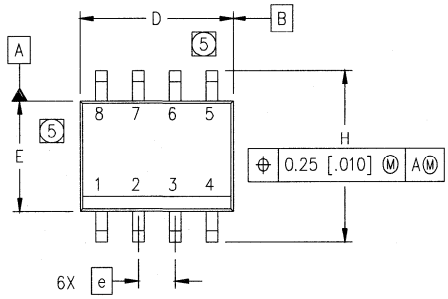
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

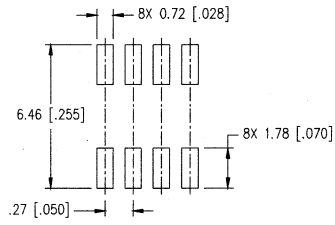


8 Lead PDIP

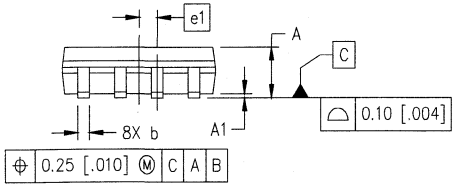
01-3003 01

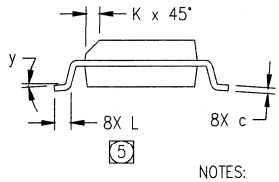


RECOMMENDED FOOTPRINT



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°





NOTES:

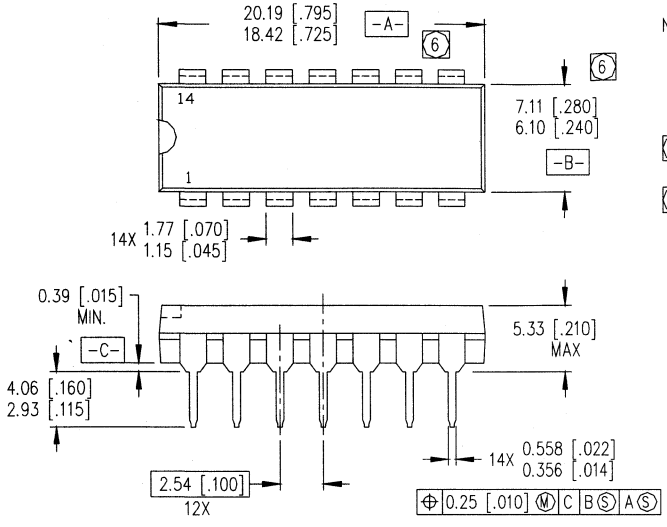
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

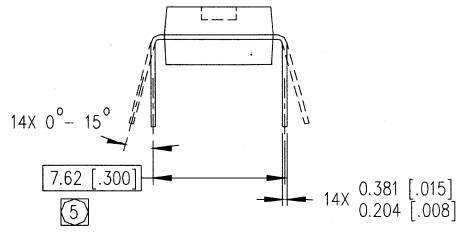
(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

8 Lead SOIC

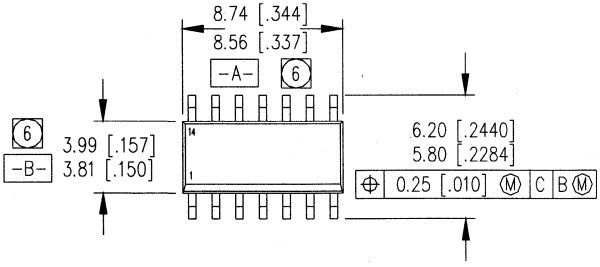


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

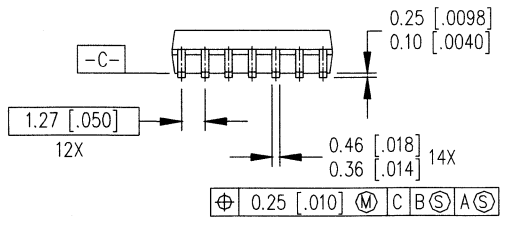


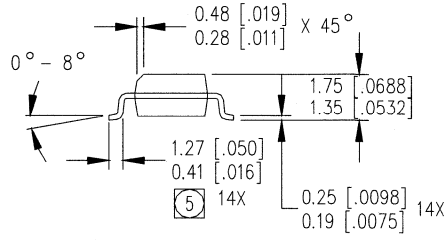
14 Lead PDIP

01-3002 03



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].





14 Lead SOIC (narrow body)

01-3063 00

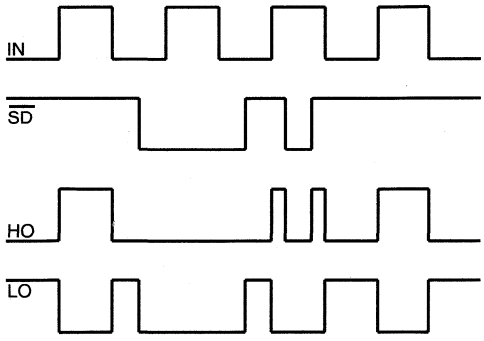


Figure 1. Input/Output Timing Diagram

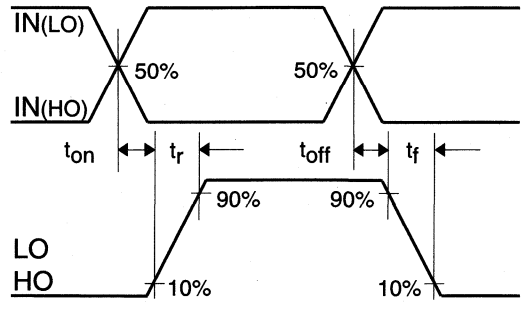


Figure 2. Switching Time Waveform Definitions

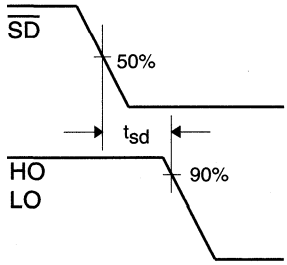


Figure 3. Shutdown Waveform Definitions

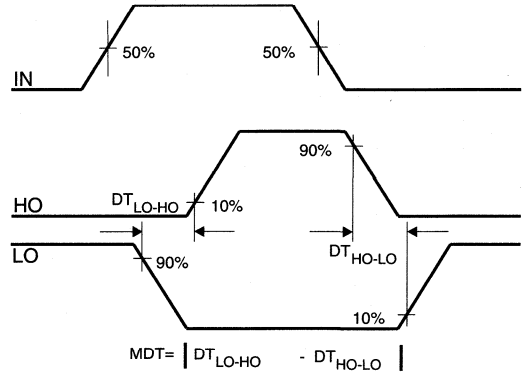


Figure 4. Deadtime Waveform Definitions

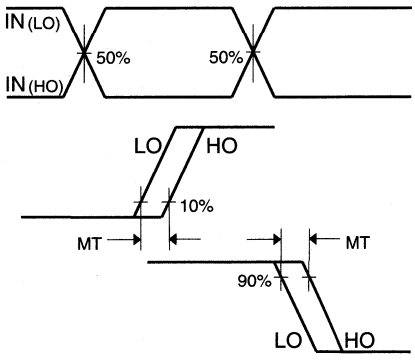


Figure 5. Delay Matching Waveform Definitions

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Data Sheet No. PD60147-L

IR2110/IR2113

HIGH AND LOW SIDE DRIVER

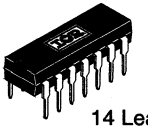
Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

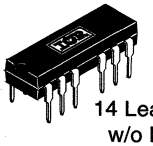
Product Summary

V_{OFFSET} (IR2110)	500V max.
(IR2113)	600V max.
$I_{O+/-}$	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns
Delay Matching	10 ns

Packages

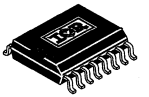


14 Lead PDIP
IR2110/IR2113



14 Lead PDIP
w/o Lead 4
IR2110-1/IR2113-1

16 Lead PDIP
w/o leads 4 & 5
IR2110-2/IR2113-2

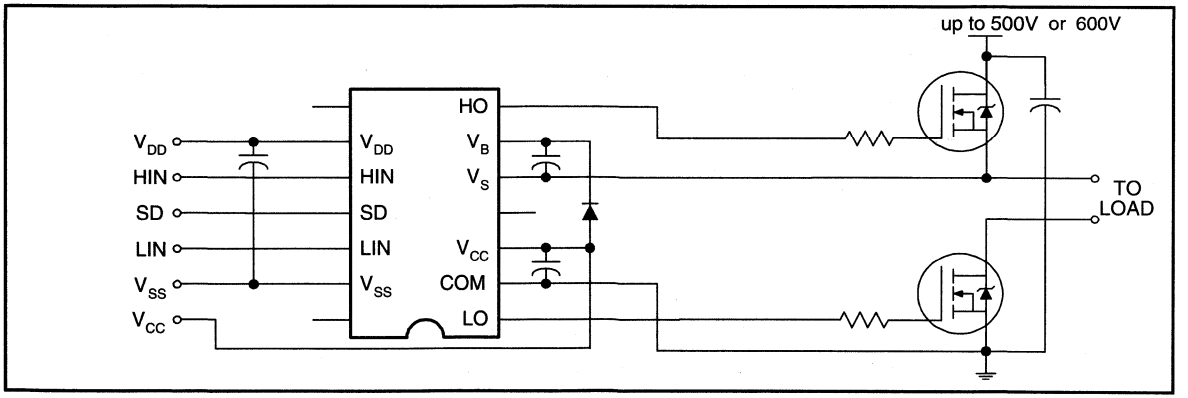


16 Lead SOIC
IR2110S/IR2113S

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage (IR2110)	-0.3	525	V
	(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage	V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS} - 0.3	V_{DD} + 0.3	
dV_s/dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$ (14 lead DIP)	—	1.6	W
	(14 lead DIP w/o lead 4)	—	1.5	
	(16 lead DIP w/o leads 4 & 5)	—	1.6	
	(16 lead SOIC)	—	1.25	
R_{THJA}	Thermal resistance, junction to ambient (14 lead DIP)	—	75	°C/W
	(14 lead DIP w/o lead 4)	—	85	
	(16 lead DIP w/o leads 4 & 5)	—	75	
	(16lLead SOIC)	—	100	
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage (IR2110)	Note 1	500	
	(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{DD}	Logic supply voltage	V_{SS} + 4.5	V_{SS} + 20	
V_{SS}	Logic supply offset voltage	-5	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

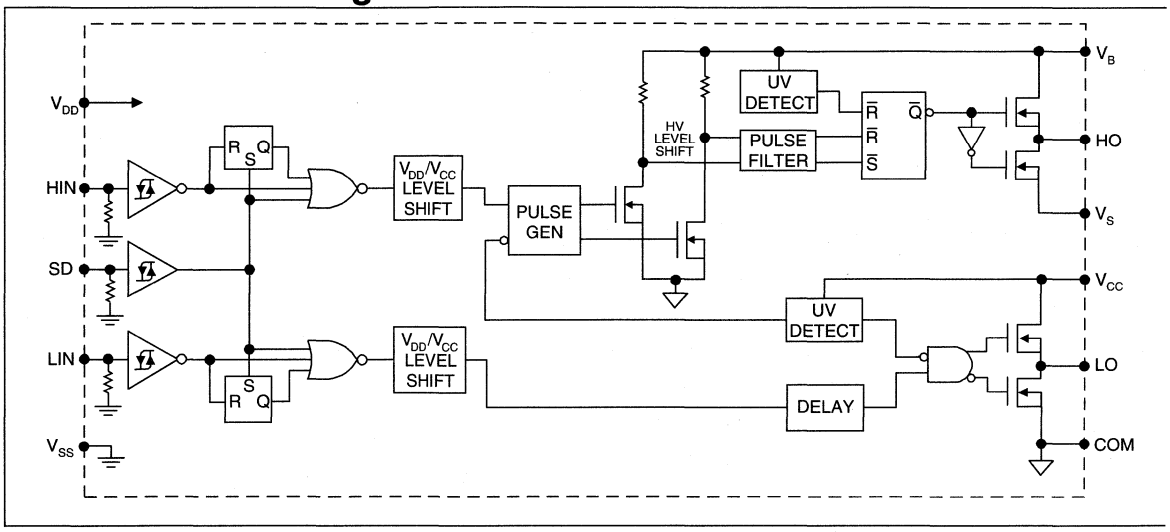
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	120	150	ns	V_S = 0V
t_{off}	Turn-off propagation delay	8	—	94	125		V_S = 500V/600V
t_{sd}	Shutdown propagation delay	9	—	110	140		V_S = 500V/600V
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off	—	—	—	10		Figure 5

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	16	—	—	50	µA	V_B=V_S = 500V/600V
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" input bias current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

Functional Block Diagram



Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

14 Lead PDIP	14 Lead PDIP w/o Lead 4	16 Lead PDIP w/o Leads 4 & 5	16 Lead SOIC (Wide Body)
IR2110/IR2113	IR2110-1/IR2113-1	IR2110-2/IR2113-2	IR2110S/IR2113S
Part Number			

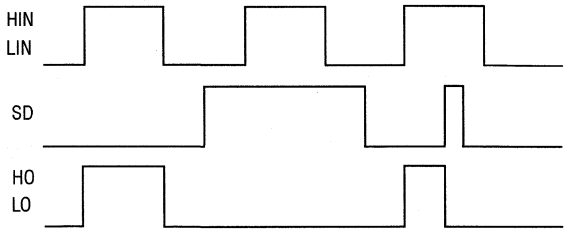


Figure 1. Input/Output Timing Diagram

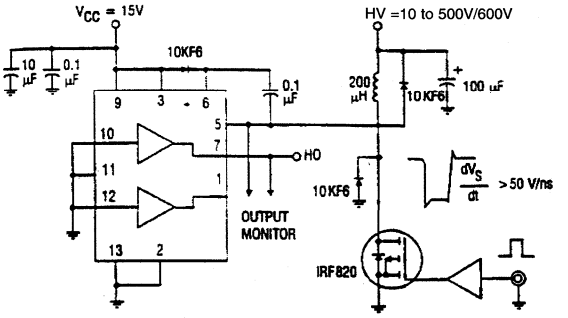


Figure 2. Floating Supply Voltage Transient Test Circuit

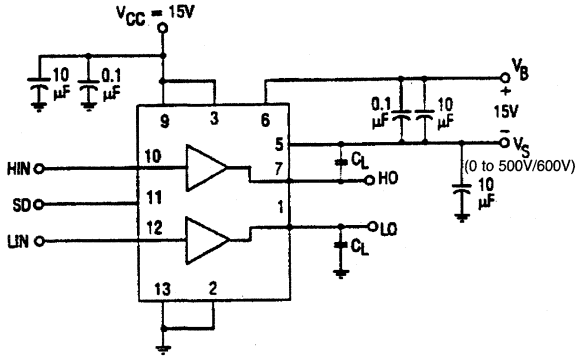


Figure 3. Switching Time Test Circuit

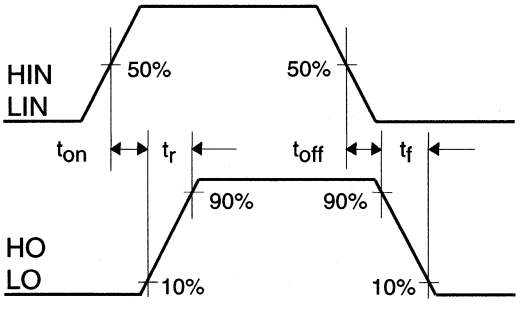


Figure 4. Switching Time Waveform Definition

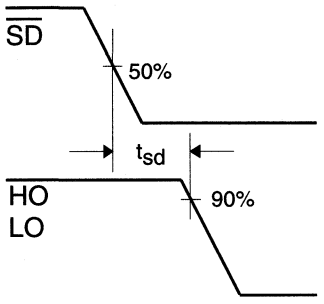


Figure 3. Shutdown Waveform Definitions

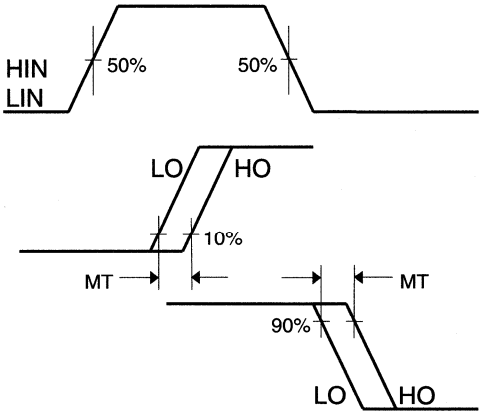


Figure 6. Delay Matching Waveform Definitions

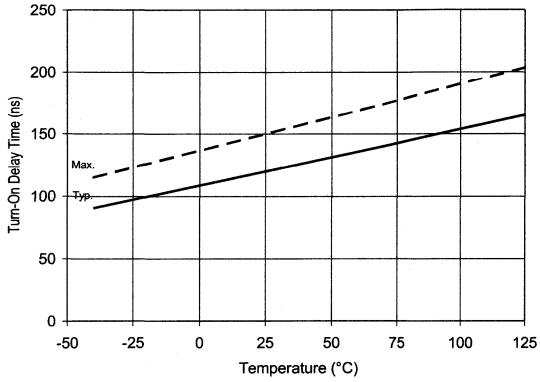


Figure 7A. Turn-On Time vs. Temperature

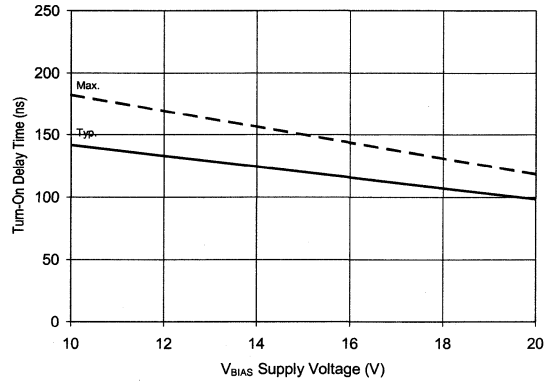


Figure 7B. Turn-On Time vs. Voltage

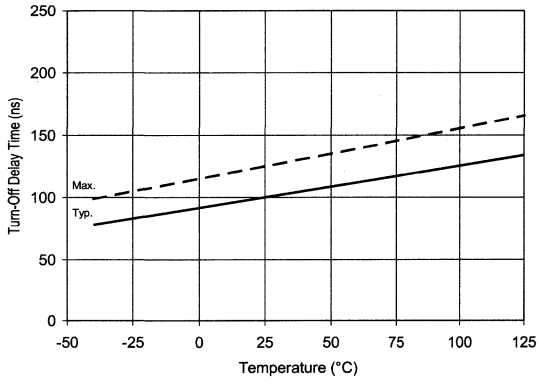


Figure 8A. Turn-Off Time vs. Temperature

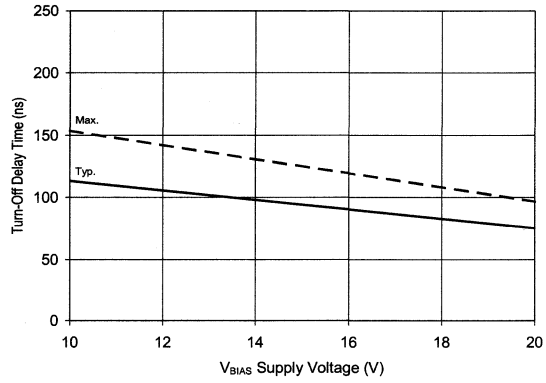


Figure 8B. Turn-Off Time vs. Voltage

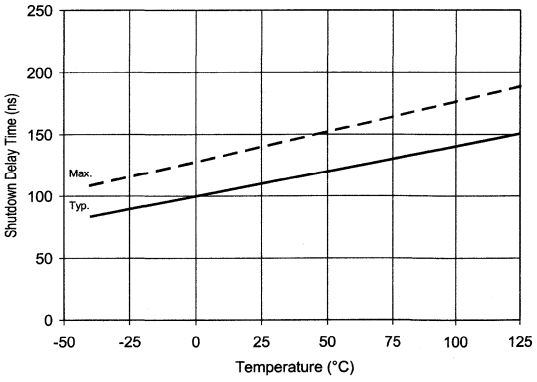


Figure 9A. Shutdown Time vs. Temperature

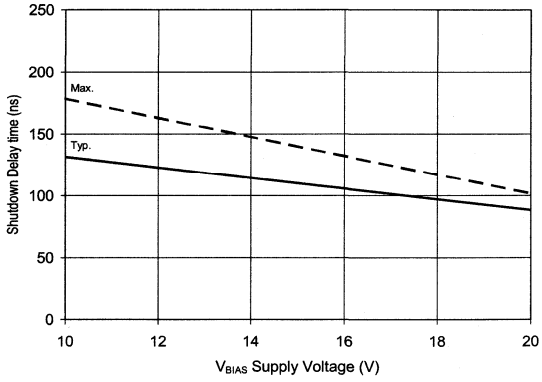


Figure 9B. Shutdown Time vs. Voltage

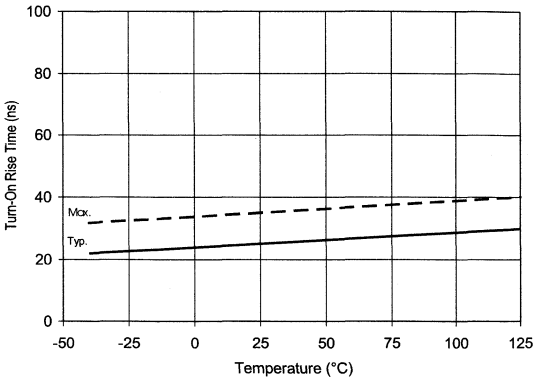


Figure 10A. Turn-On Rise Time vs. Temperature

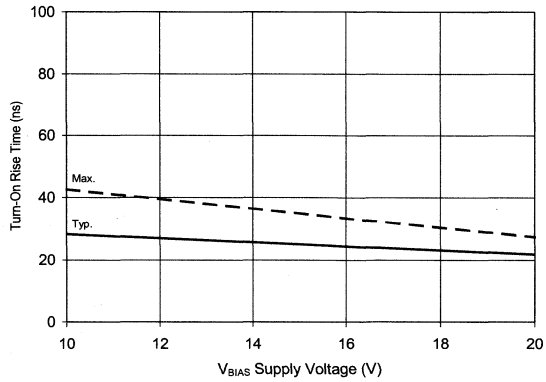


Figure 10B. Turn-On Rise Time vs. Voltage

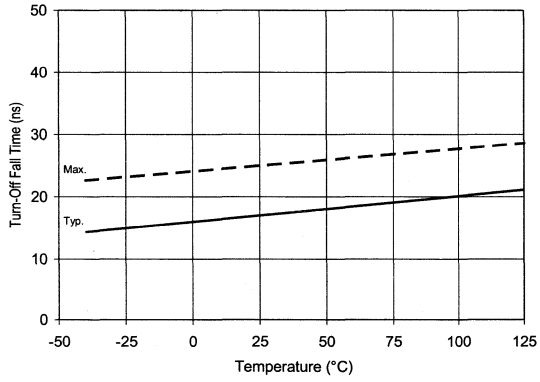


Figure 11A. Turn-Off Fall Time vs. Temperature

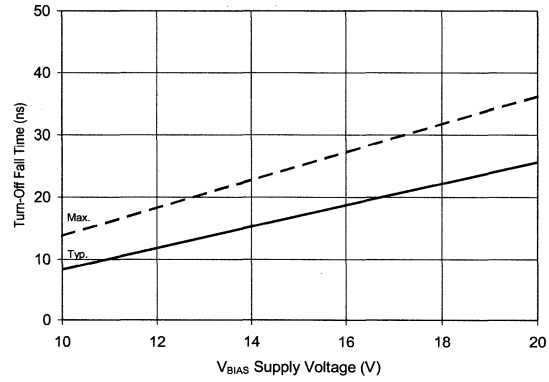


Figure 11B. Turn-Off Fall Time vs. Voltage

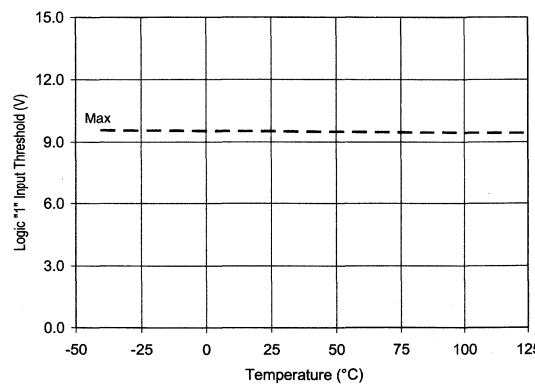


Figure 12A. Logic "1" Input Threshold vs. Temperature

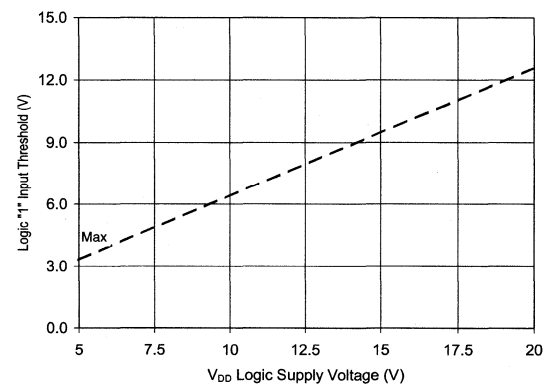


Figure 12B. Logic "1" Input Threshold vs. Voltage

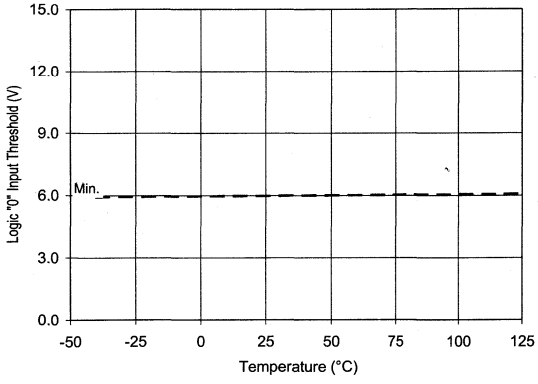


Figure 13A. Logic "0" Input Threshold vs. Temperature

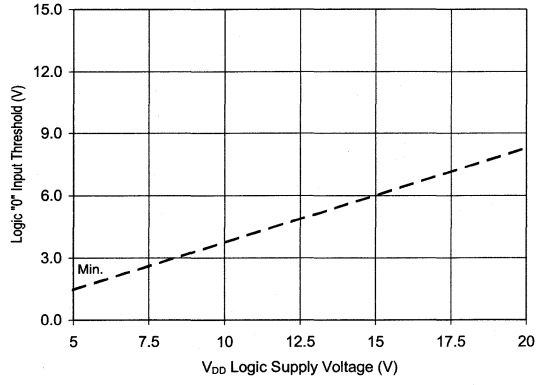


Figure 13B. Logic "0" Input Threshold vs. Voltage

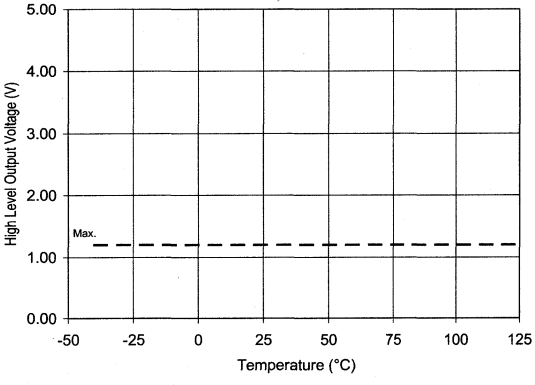


Figure 14A. High Level Output vs. Temperature

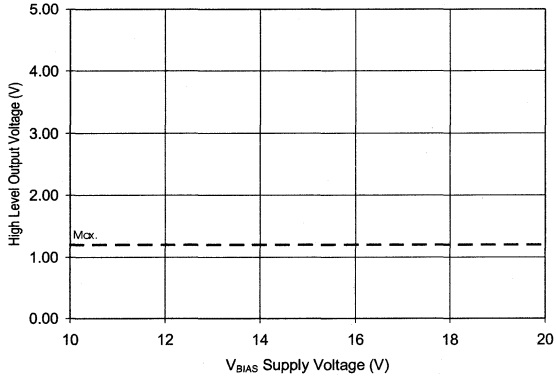


Figure 14B. High Level Output vs. Voltage

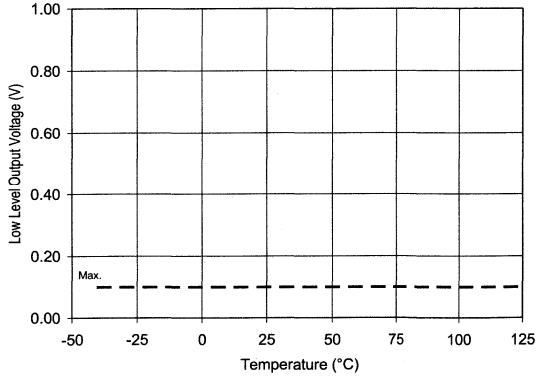


Figure 15A. Low Level Output vs. Temperature

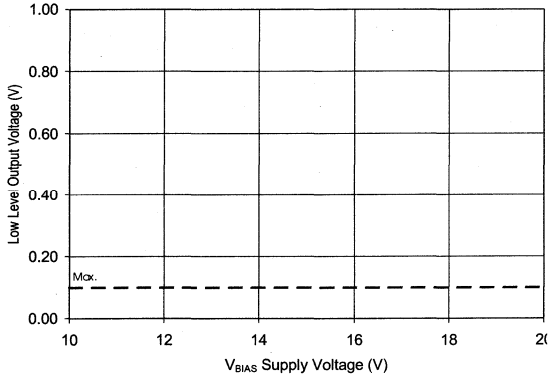


Figure 15B. Low Level Output vs. Voltage

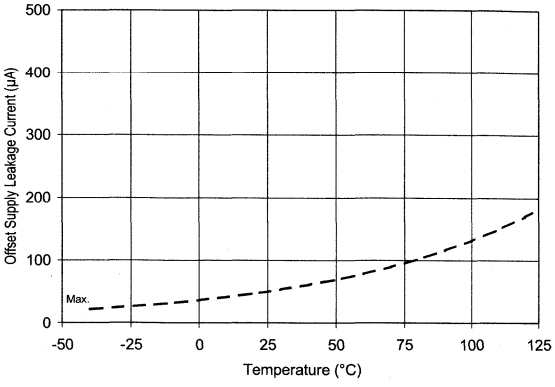


Figure 16A. Offset Supply Current vs. Temperature

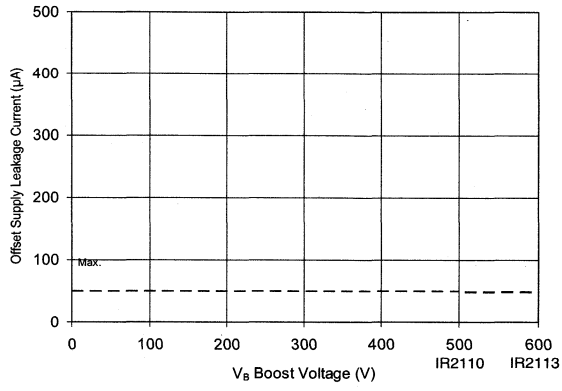


Figure 16B. Offset Supply Current vs. Voltage

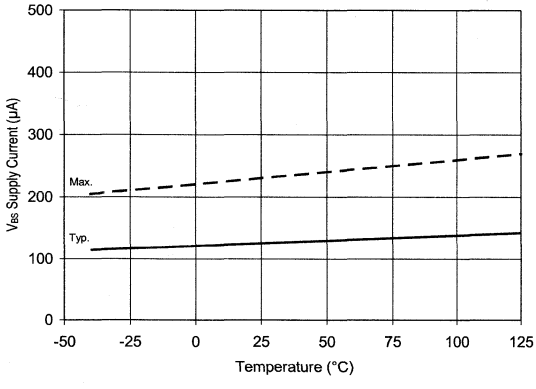


Figure 17A. V_{BS} Supply Current vs. Temperature

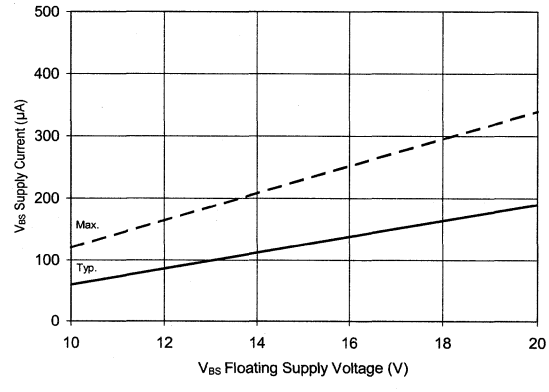


Figure 17B. V_{BS} Supply Current vs. Voltage

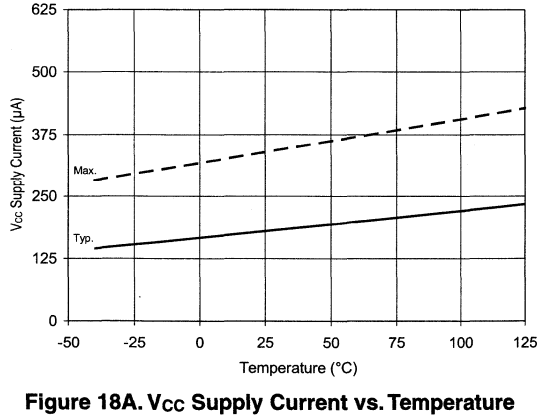


Figure 18A. V_{CC} Supply Current vs. Temperature

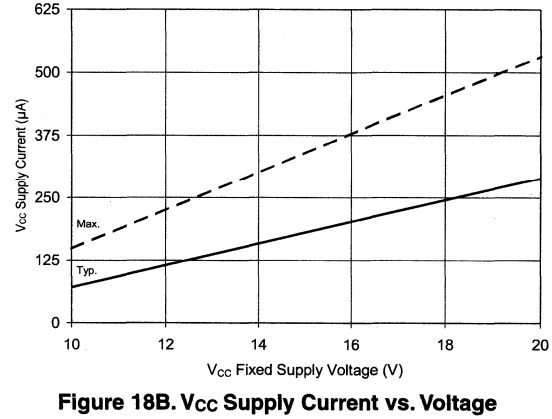


Figure 18B. V_{CC} Supply Current vs. Voltage

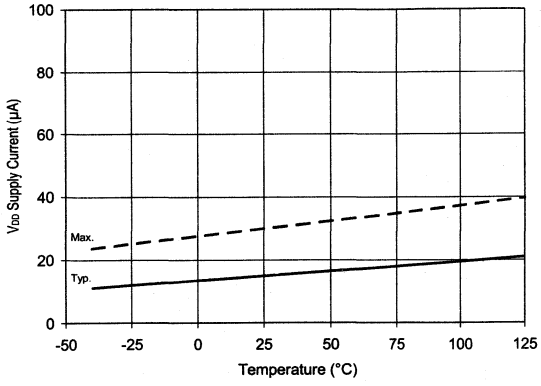


Figure 19A. V_{DD} Supply Current vs. Temperature

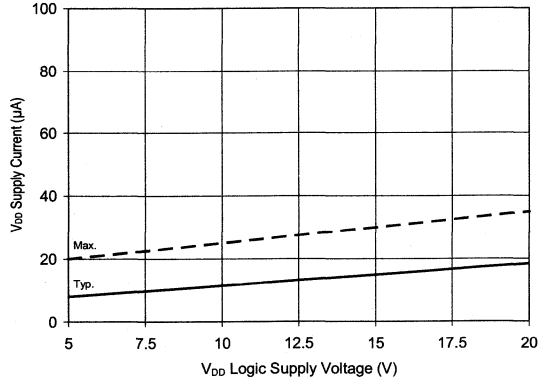


Figure 19B. V_{DD} Supply Current vs. Voltage

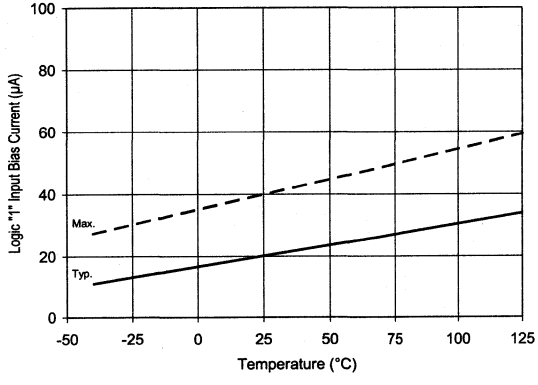


Figure 20A. Logic "1" Input Current vs. Temperature

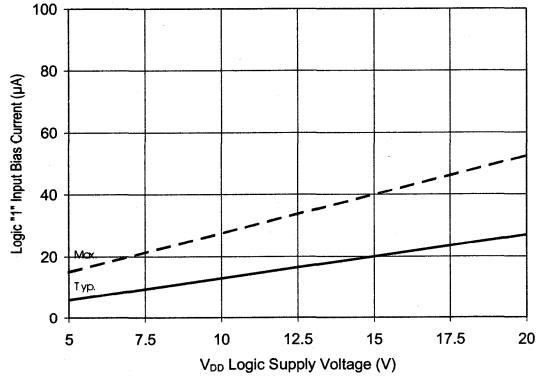


Figure 20B. Logic "1" Input Current vs. Voltage

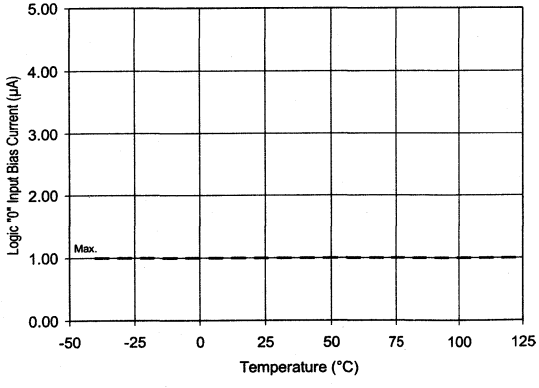


Figure 21A. Logic "0" Input Current vs. Temperature

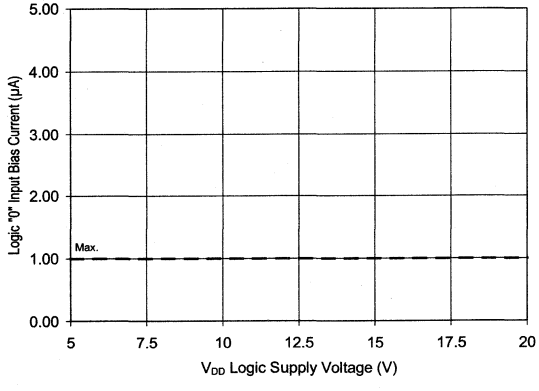


Figure 21B. Logic "0" Input Current vs. Voltage

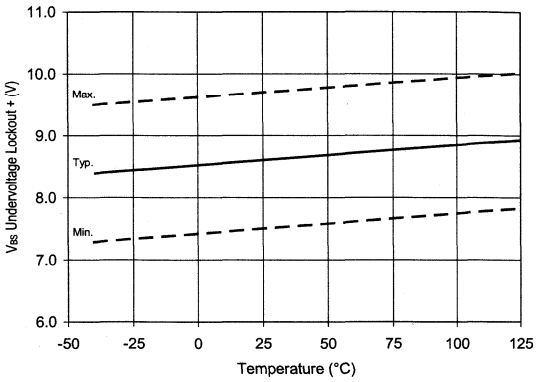


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

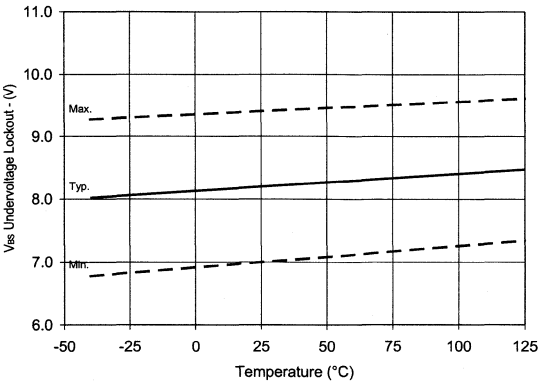


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

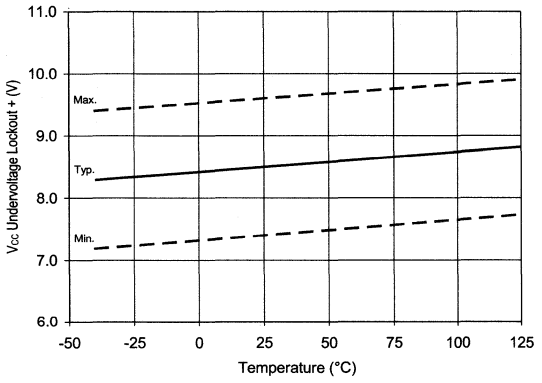


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

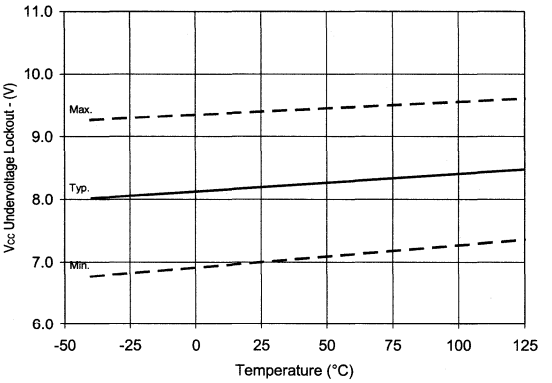


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

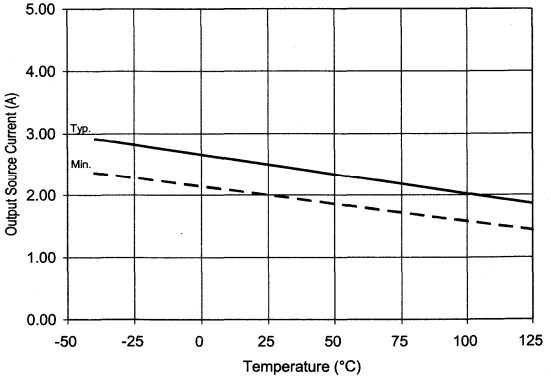


Figure 26A. Output Source Current vs. Temperature

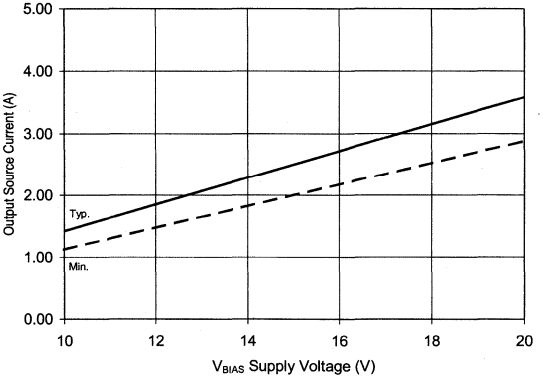


Figure 26B. Output Source Current vs. Voltage

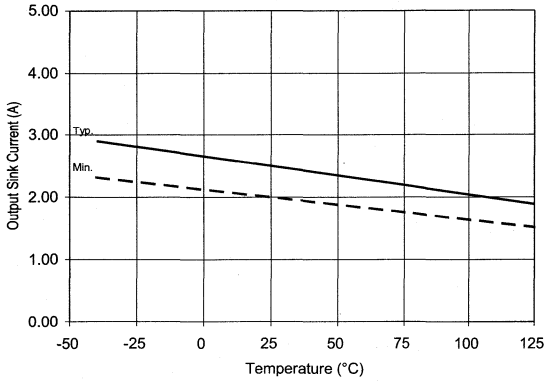


Figure 27A. Output Sink Current vs. Temperature

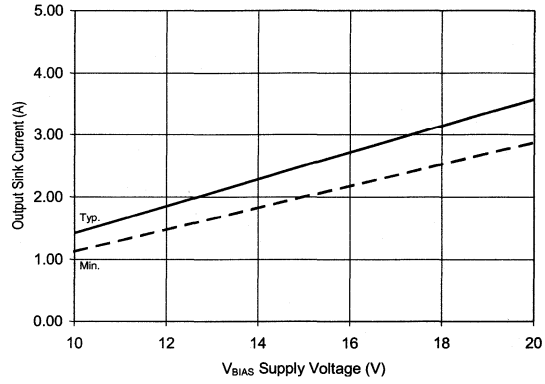


Figure 27B. Output Sink Current vs. Voltage

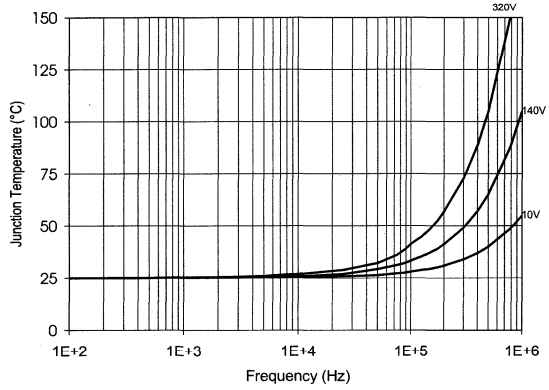


Figure 28. IR2110/IR2113 T_J vs. Frequency (IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

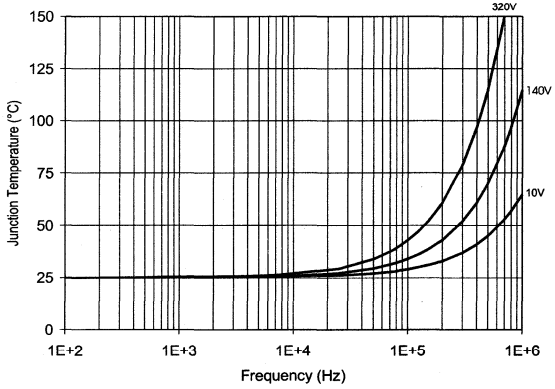


Figure 29. IR2110/IT2113 T_J vs. Frequency (IRFBC30) R_{GATE} = 22Ω, V_{CC} = 15V

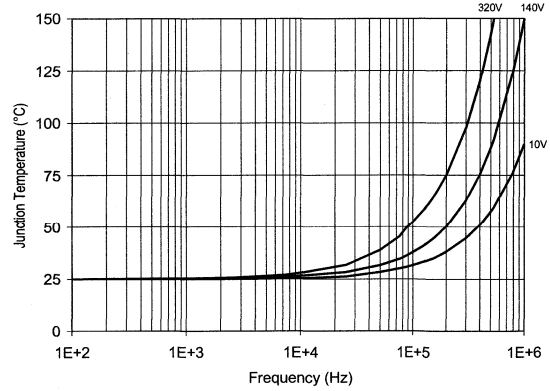


Figure 30. IR2110/IR2113 T_J vs. Frequency (IRFBC40) R_{GATE} = 15Ω, V_{CC} = 15V

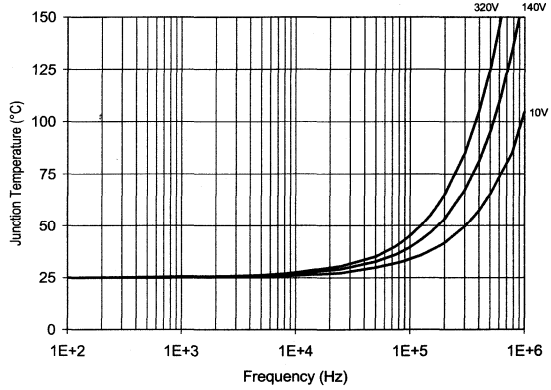


Figure 31. IR2110/IR2113 T_J vs. Frequency (IRFPE50) R_{GATE} = 10Ω, V_{CC} = 15V

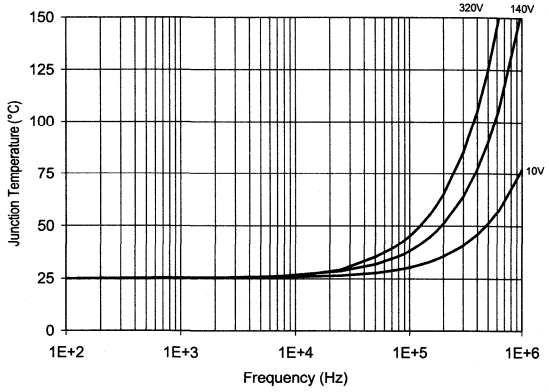


Figure 32. IR2110S/IR2113S T_J vs. Frequency (IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

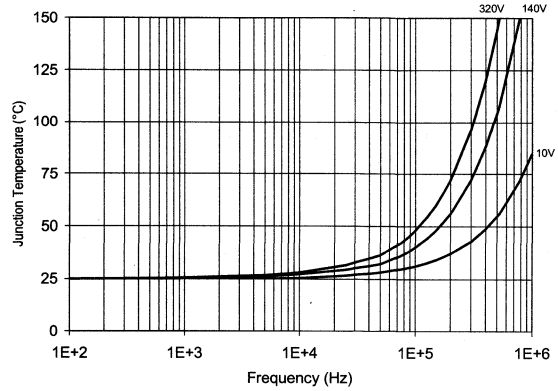


Figure 33. IR2110S/IR2113S T_J vs. Frequency (IRFBC30) R_{GATE} = 22Ω, V_{CC} = 15V

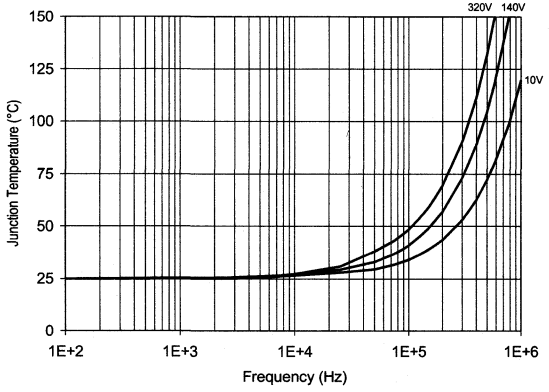


Figure 34. IR2110S/IR2113S T_J vs. Frequency (IRFBC40) R_{GATE} = 15Ω, V_{CC} = 15V

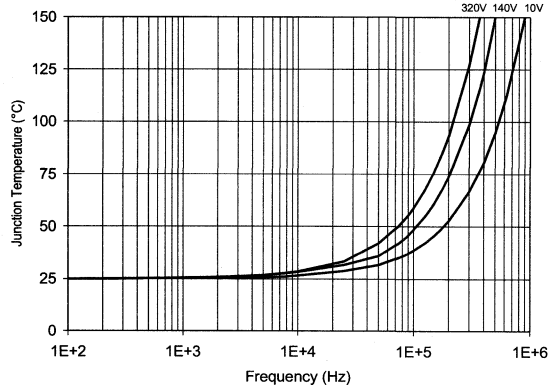


Figure 35. IR2110S/IR2113S T_J vs. Frequency (IRFPE50) R_{GATE} = 10Ω, V_{CC} = 15V

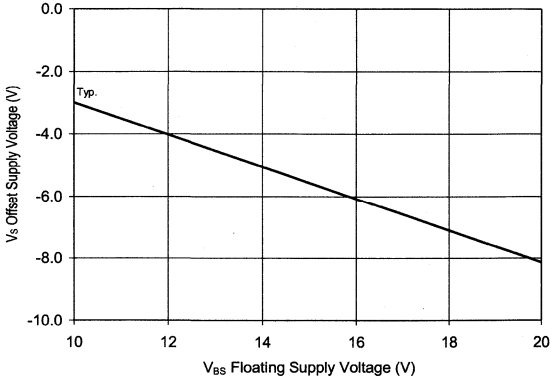


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

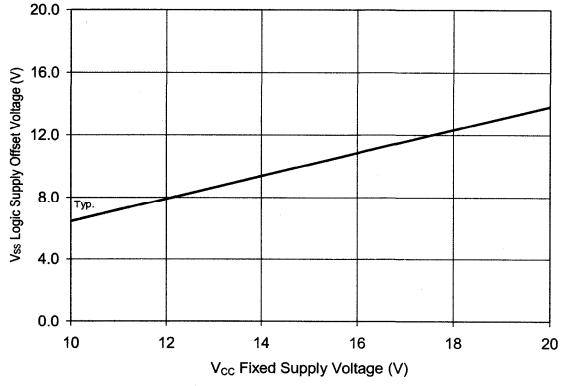
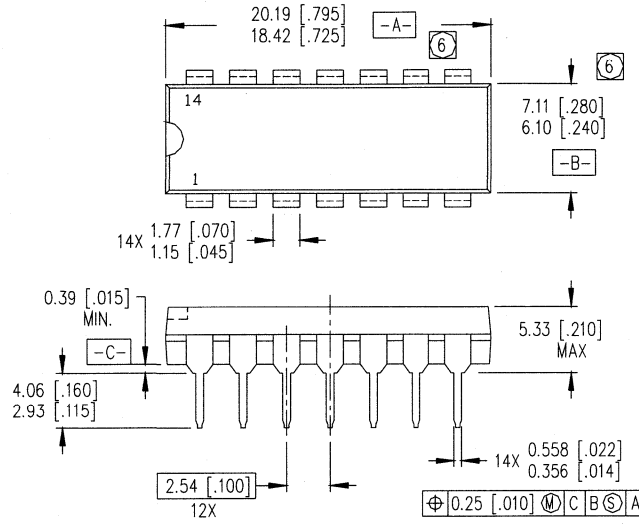


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

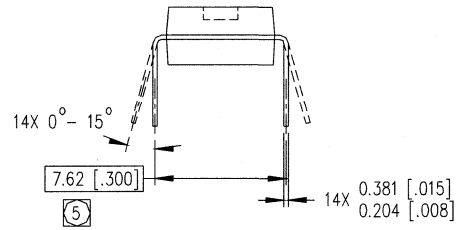
Case Outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.

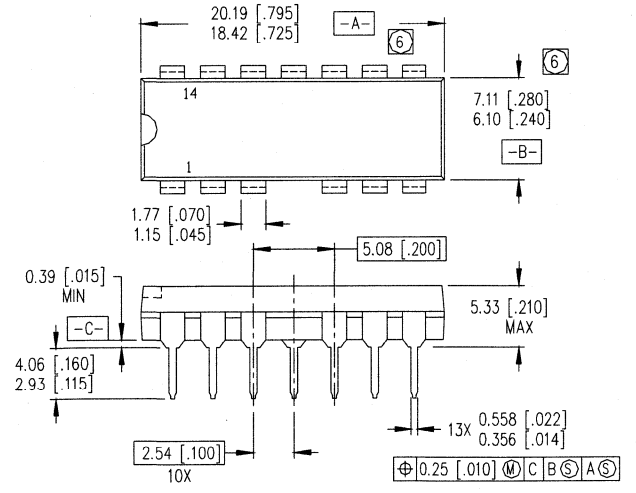
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



14 Lead PDIP

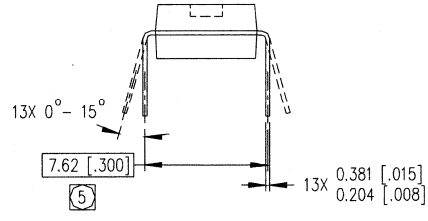
01-3002 03



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.

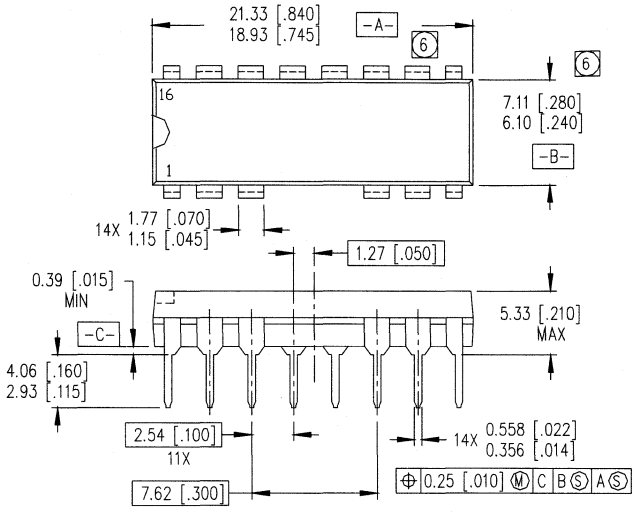
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



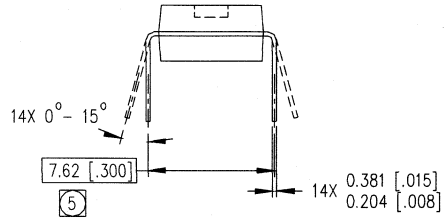
14 Lead PDIP w/o Lead 4

01-3008 02



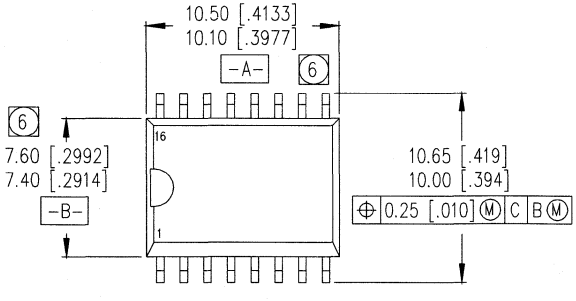
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



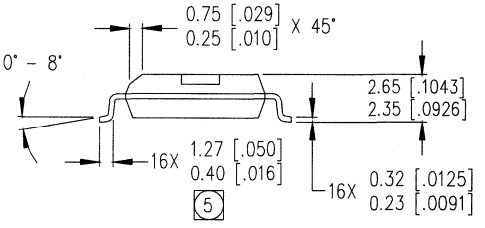
16 Lead PDIP w/o Leads 4 & 5

01-3010 02



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



16 Lead SOIC (wide body)

01-3014 03

Data Sheet No. PD60026-K

IR2112

HIGH AND LOW SIDE DRIVER

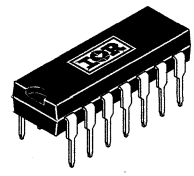
Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
- Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

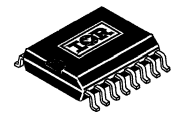
Product Summary

V_{OFFSET}	600V max.
I_{O}+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	125 & 105 ns
Delay Matching	30 ns

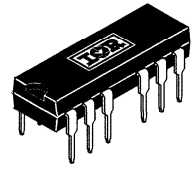
Packages



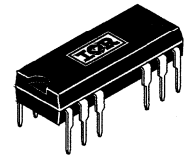
14 lead PDIP



16 lead SOIC (wide body)



14 lead PDIP w/o lead 4

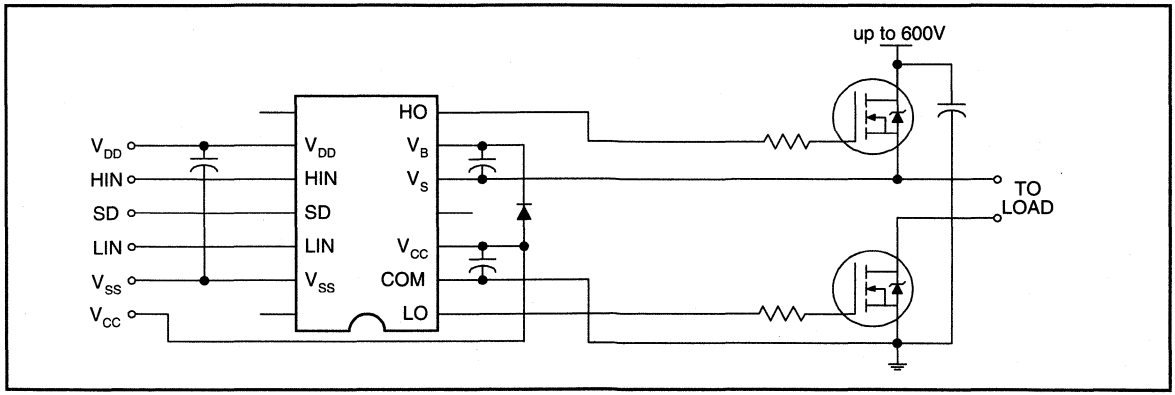


16 lead PDIP w/o leads 4 & 5

Description

The IR2112 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic Supply Voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic Supply Offset Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS} - 0.3	V_{DD} + 0.3	
dV_s/dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (14 Lead DIP)	—	1.6	W
	(14 Lead DIP w/o Lead 4)	—	1.5	
	(16 Lead DIP w/o Leads 4 & 5)	—	1.6	
	(16 Lead SOIC)	—	1.25	
R_{THJA}	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	°C/W
	(14 Lead DIP w/o Lead 4)	—	85	
	(16 Lead DIP w/o Leads 4 & 5)	—	75	
	(16 Lead SOIC)	—	100	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 4.5	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

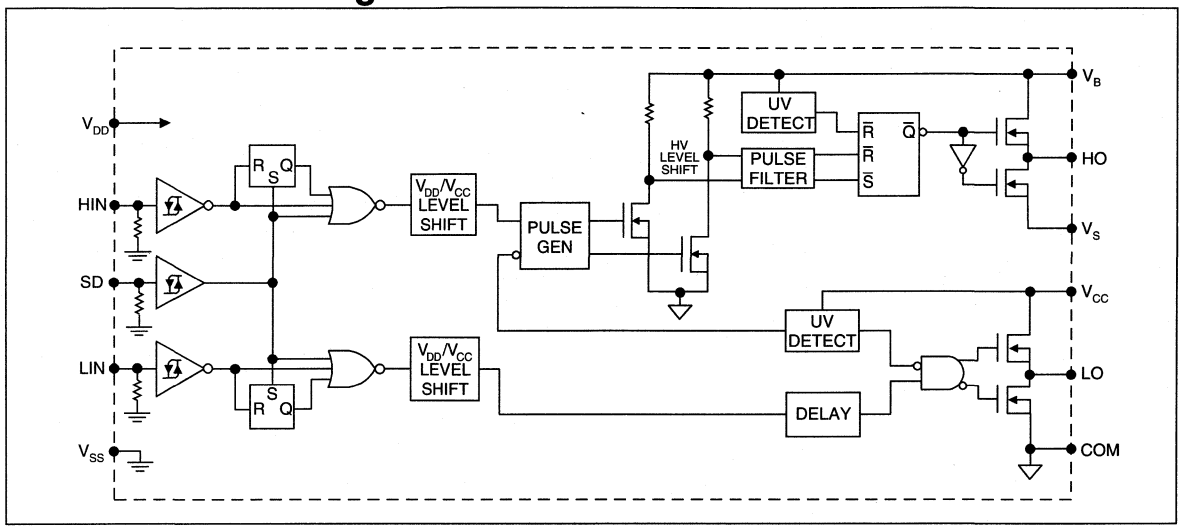
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	125	180	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	8	—	105	160		V_S = 600V
t_{sd}	Shutdown Propagation Delay	9	—	105	160		V_S = 600V
t_r	Turn-On Rise Time	10	—	80	130		
t_f	Turn-Off Fall Time	11	—	40	65		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	30		Figure 5

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	13	—	—	6.0		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	14	—	—	100	mV	I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	15	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	16	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	25	60		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	80	180		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	2.0	5.0		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" Input Bias Current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.4	8.5	9.6	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.1	9.2		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.2	8.2	9.2		
I_{O+}	Output High Short Circuit Pulsed Current	26	200	250	—	mA	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	27	420	500	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

Functional Block Diagram



Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

14 Lead DIP	14 Lead DIP w/o Lead 4	16 Lead DIP w/o Leads 4 & 5	16 Lead SOIC (Wide Body)
IR2112	IR2112-1	IR2112-2	IR2112S
Part Number			

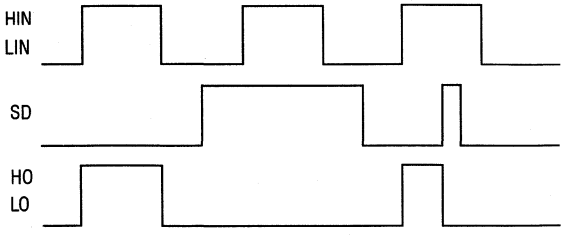


Figure 1. Input/Output Timing Diagram

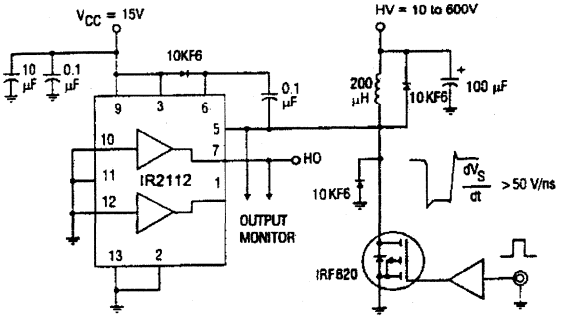


Figure 2. Floating Supply Voltage Transient Test Circuit

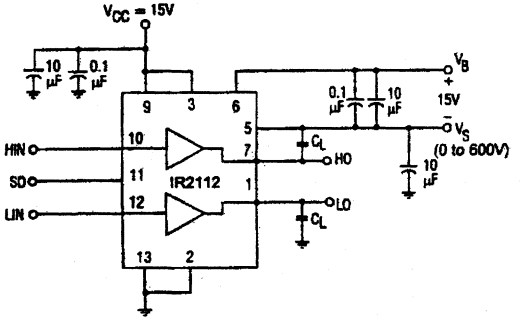


Figure 3. Switching Time Test Circuit

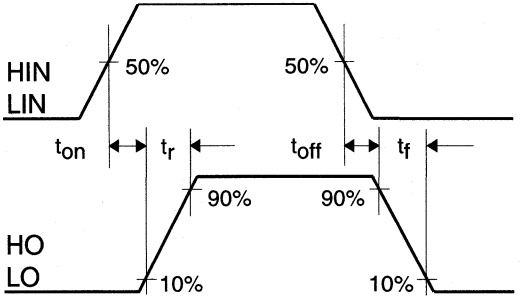


Figure 4. Switching Time Waveform Definition

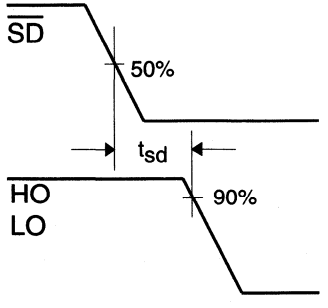


Figure 5. Shutdown Waveform Definitions

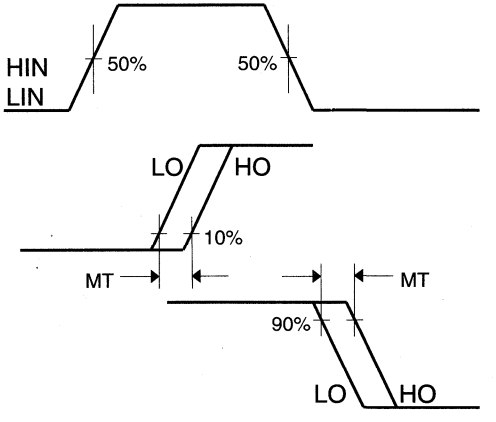


Figure 6. Delay Matching Waveform Definitions

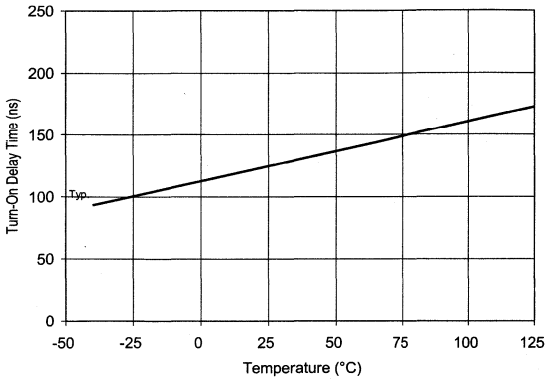


Figure 7A. Turn-On Time vs. Temperature

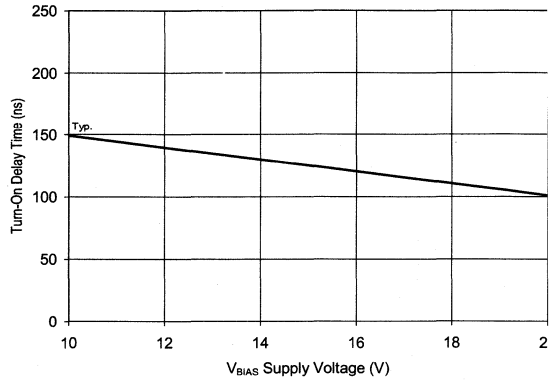


Figure 7B. Turn-On Time vs. Voltage

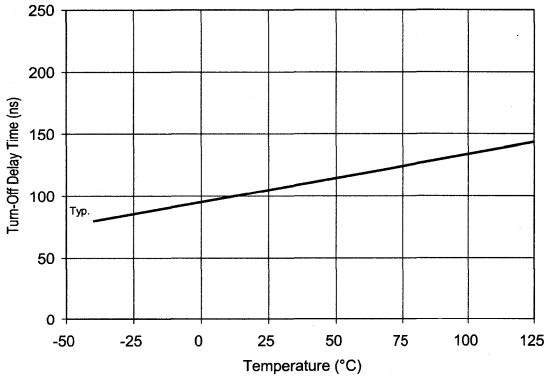


Figure 8A. Turn-Off Time vs. Temperature

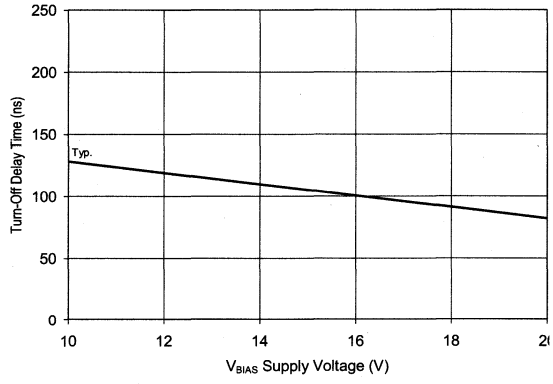


Figure 8B. Turn-Off Time vs. Voltage

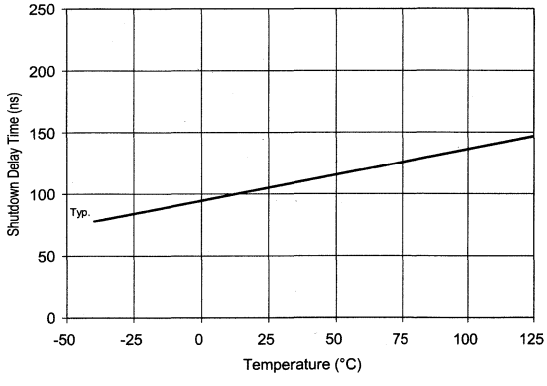


Figure 9A. Shutdown Time vs. Temperature

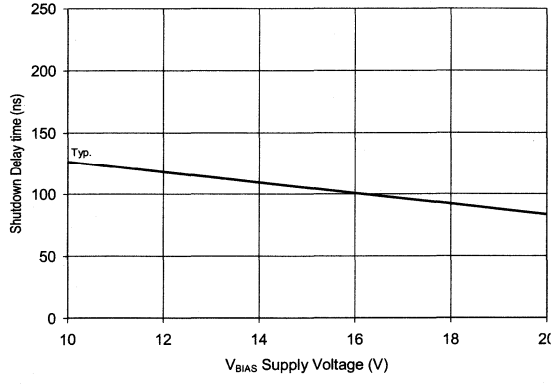


Figure 9B. Shutdown Time vs. Voltage

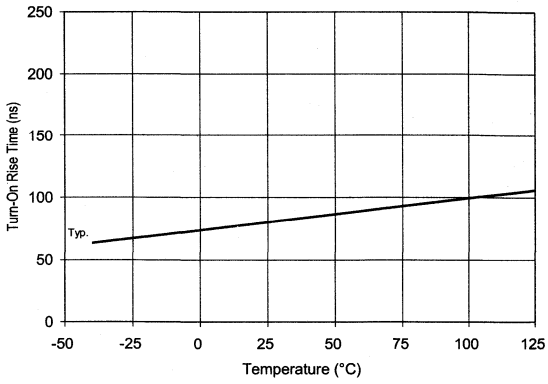


Figure 10A. Turn-On Rise Time vs. Temperature

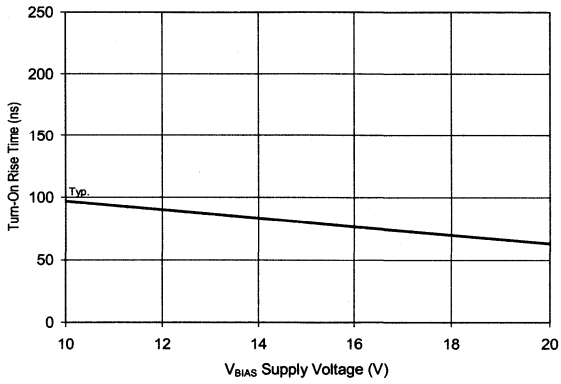


Figure 10B. Turn-On Rise Time vs. Voltage

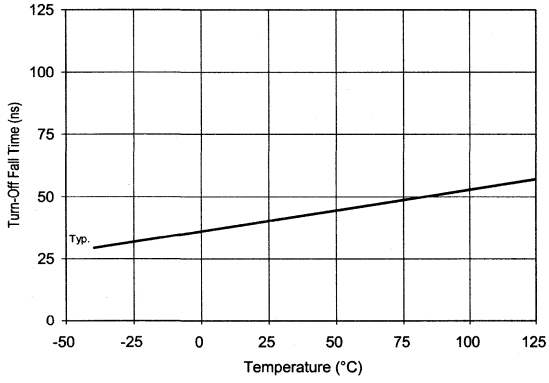


Figure 11A. Turn-Off Fall Time vs. Temperature

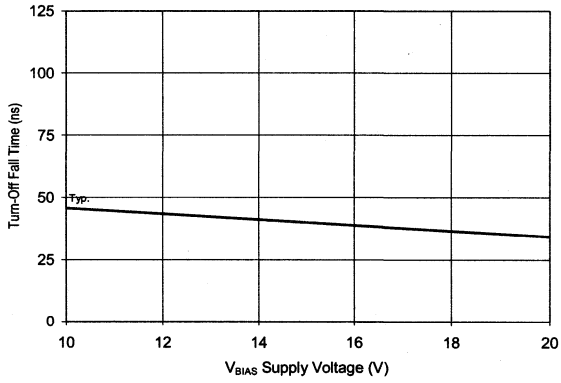


Figure 11B. Turn-Off Fall Time vs. Voltage

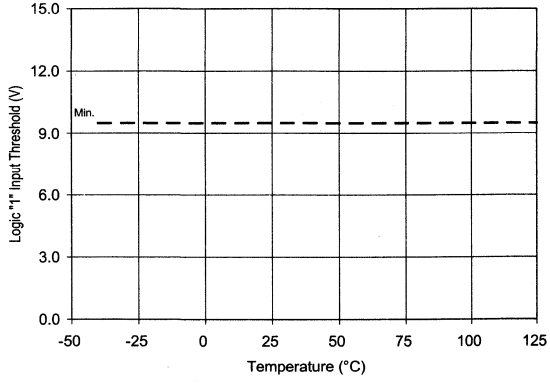


Figure 12A. Logic "1" Input Threshold vs. Temperature

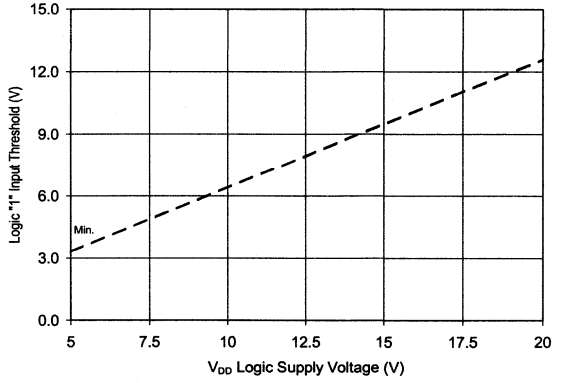


Figure 12B. Logic "1" Input Threshold vs. Voltage

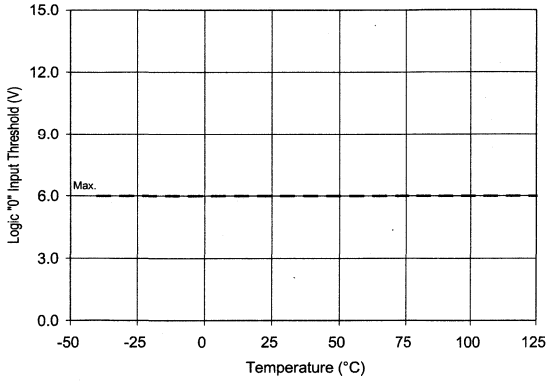


Figure 13A. Logic "0" Input Threshold vs. Temperature

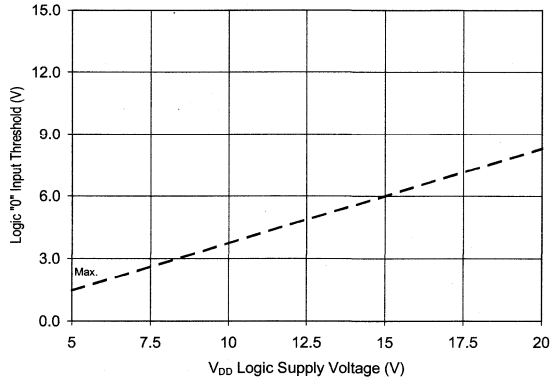


Figure 13B. Logic "0" Input Threshold vs. Voltage

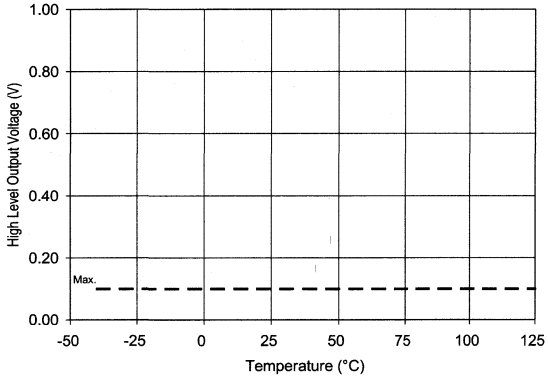


Figure 14A. High Level Output vs. Temperature

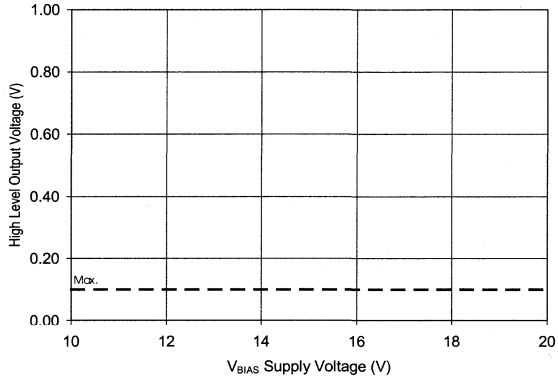


Figure 14B. High Level Output vs. Voltage

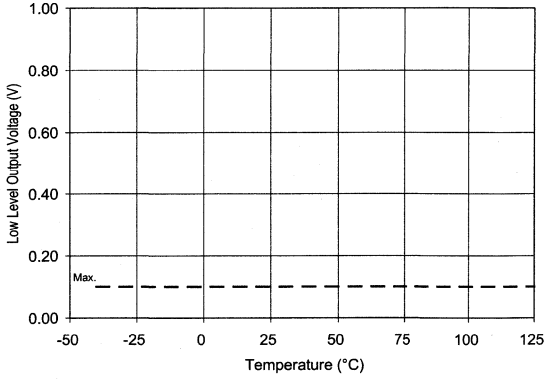


Figure 15A. Low Level Output vs. Temperature

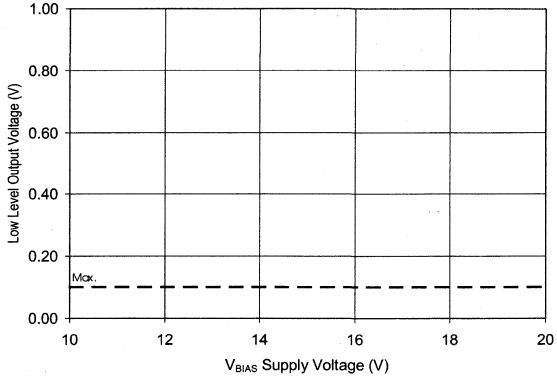


Figure 15B. Low Level Output vs. Voltage

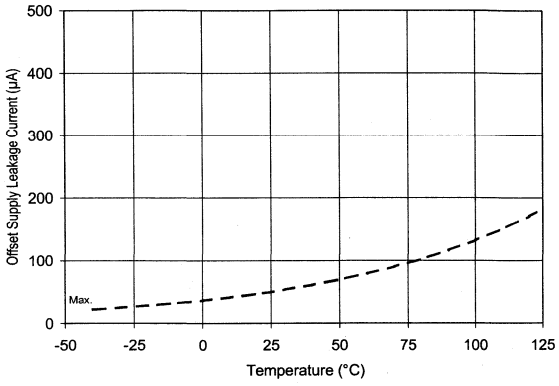


Figure 16A. Offset Supply Current vs. Temperature

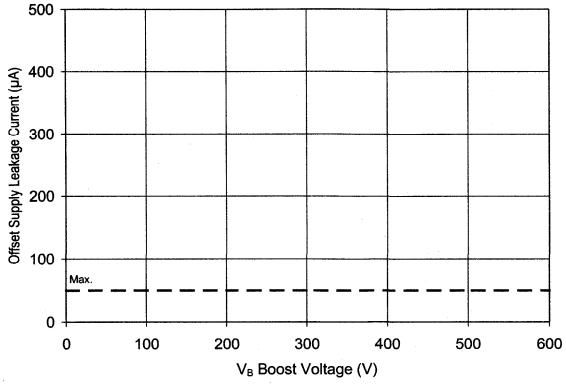


Figure 16B. Offset Supply Current vs. Voltage

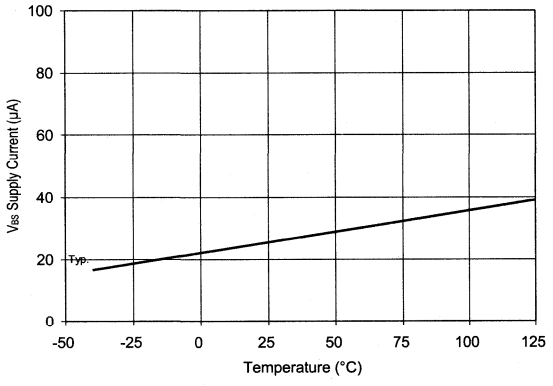


Figure 17A. V_{BS} Supply Current vs. Temperature

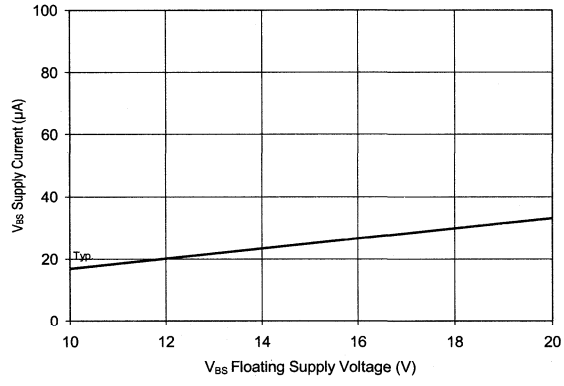


Figure 17B. V_{BS} Supply Current vs. Voltage

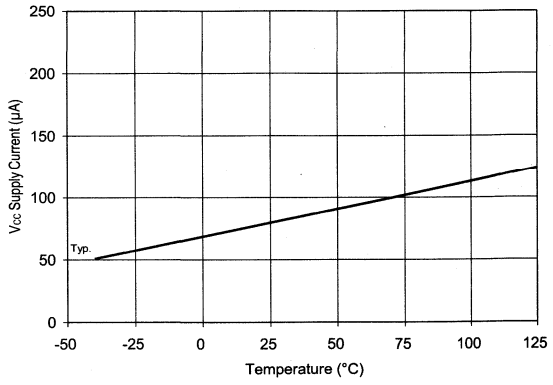


Figure 18A. V_{CC} Supply Current vs. Temperature

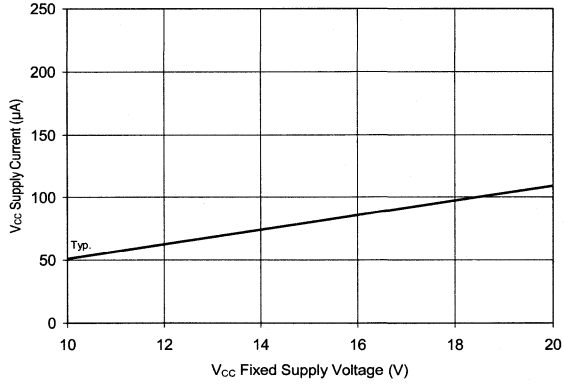


Figure 18B. V_{CC} Supply Current vs. Voltage

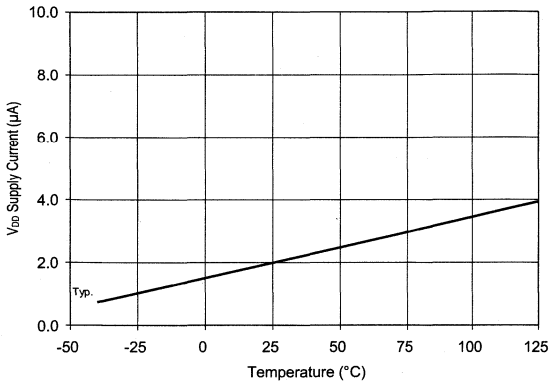


Figure 19A. V_{DD} Supply Current vs. Temperature

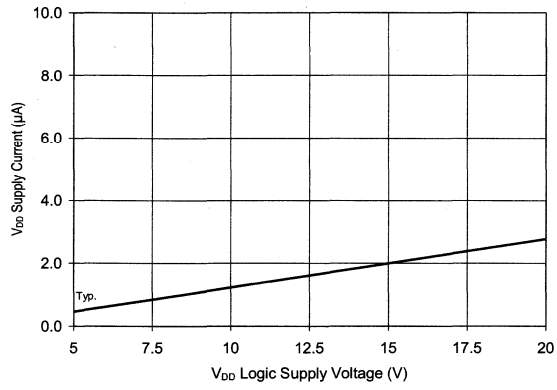


Figure 19B. V_{DD} Supply Current vs. Voltage

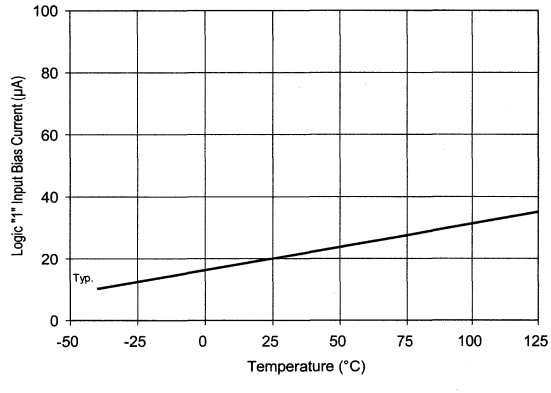


Figure 20A. Logic "1" Input Current vs. Temperature

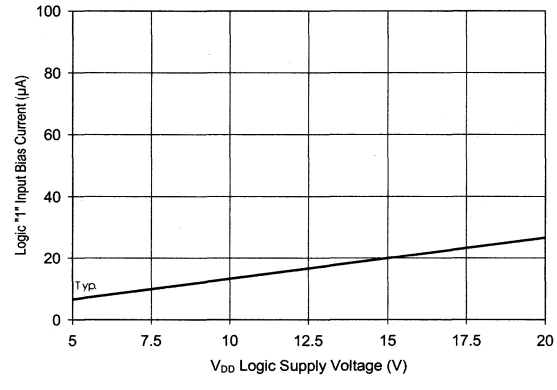


Figure 20B. Logic "1" Input Current vs. Voltage

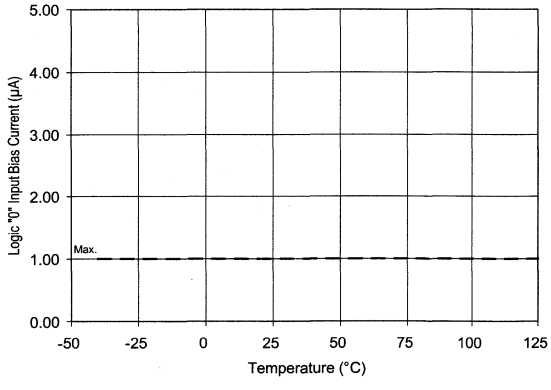


Figure 21A. Logic "0" Input Current vs. Temperature

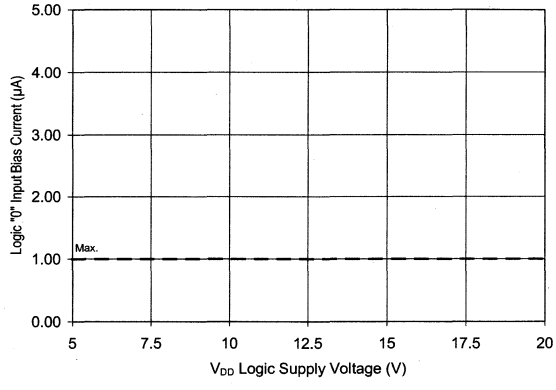


Figure 21B. Logic "0" Input Current vs. Voltage

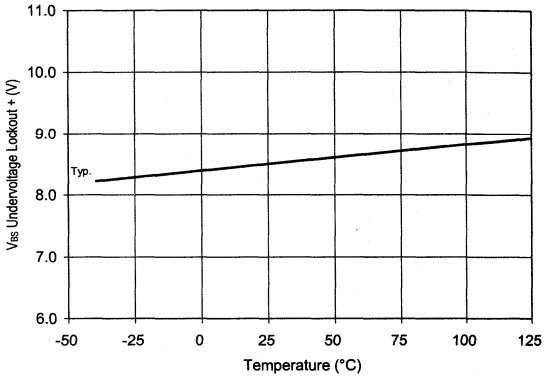


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

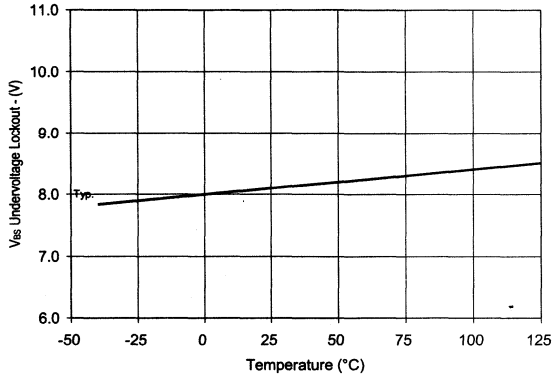


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

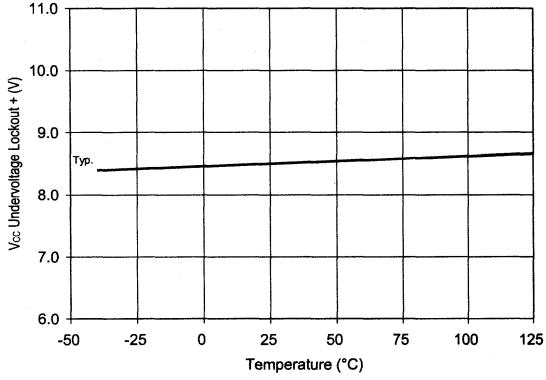


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

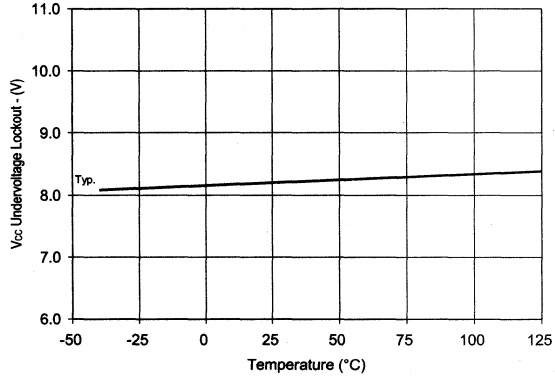


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

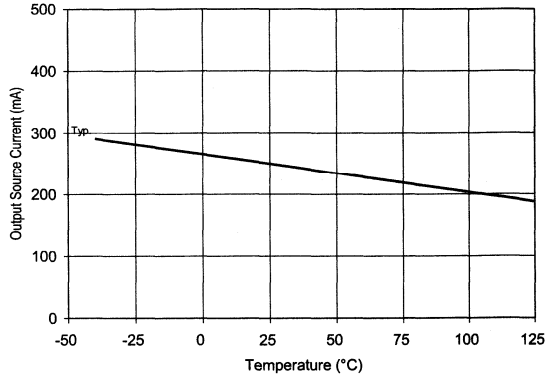


Figure 26A. Output Source Current vs. Temperature

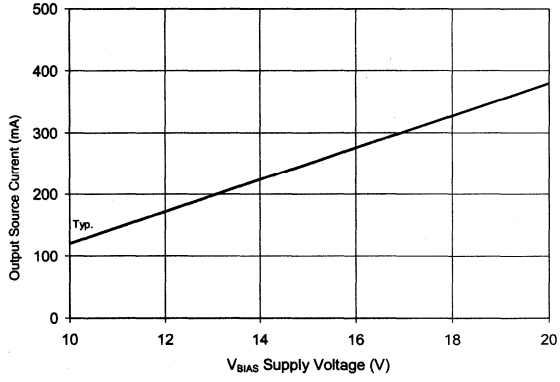


Figure 26B. Output Source Current vs. Voltage

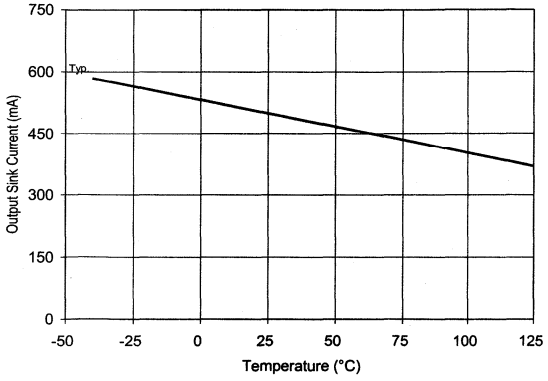


Figure 27A. Output Sink Current vs. Temperature

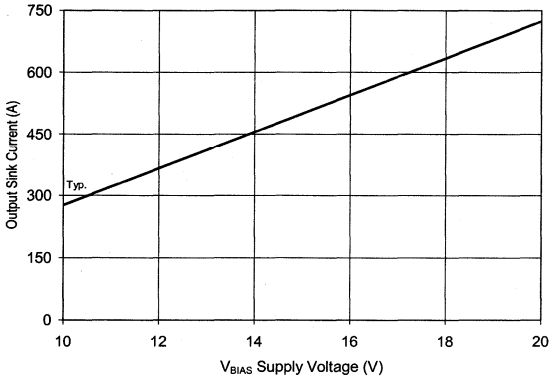


Figure 27B. Output Sink Current vs. Voltage

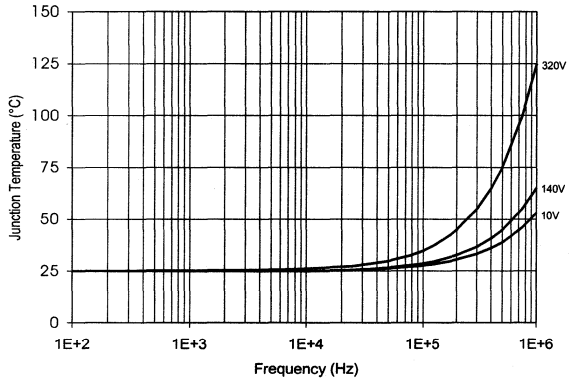


Figure 28. IR2112 T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

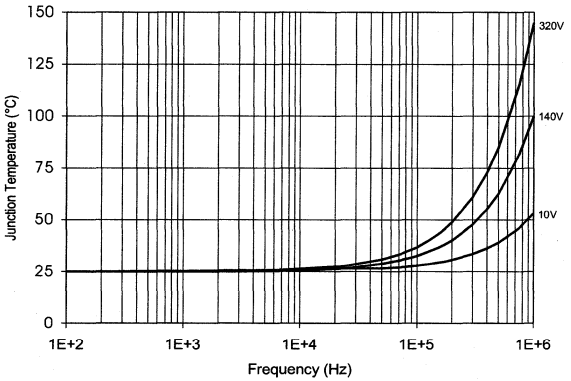


Figure 29. IR2112 T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

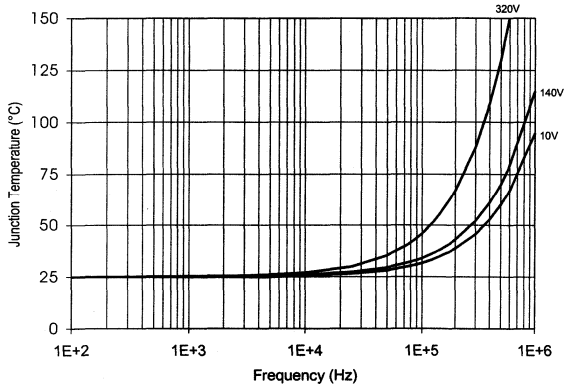


Figure 30. IR2112 T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

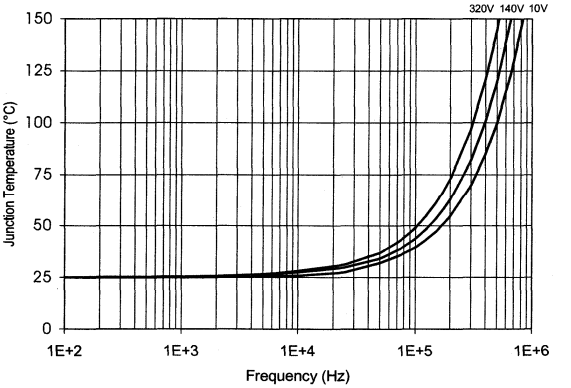


Figure 31. IR2112 T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

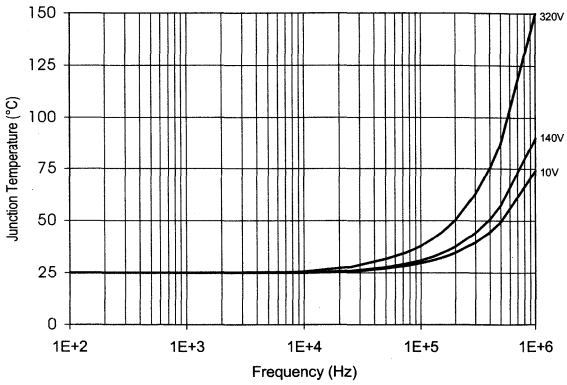


Figure 32. IR2112S T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

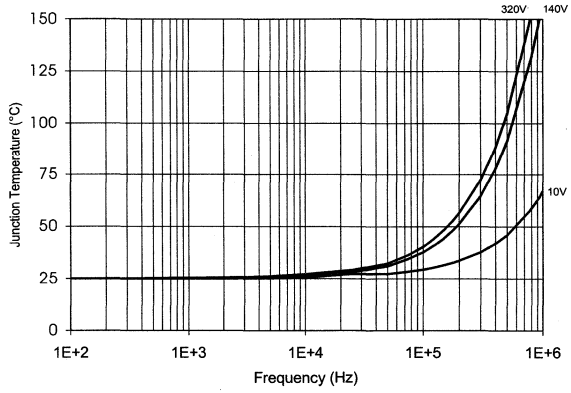


Figure 33. IR2112S T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

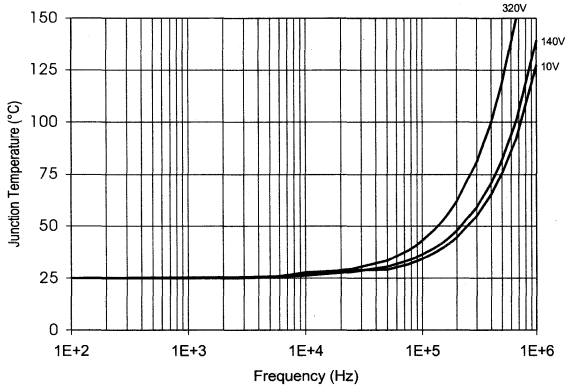


Figure 34. IR2112S T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

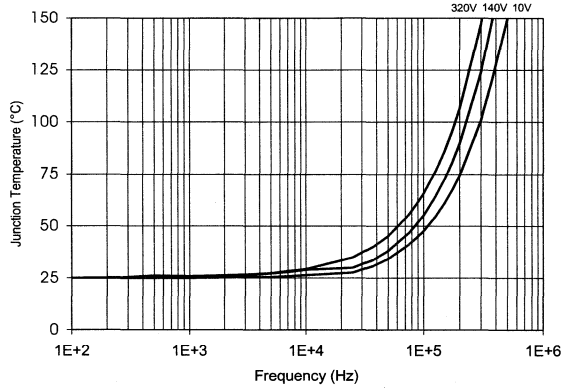


Figure 35. IR2112S T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

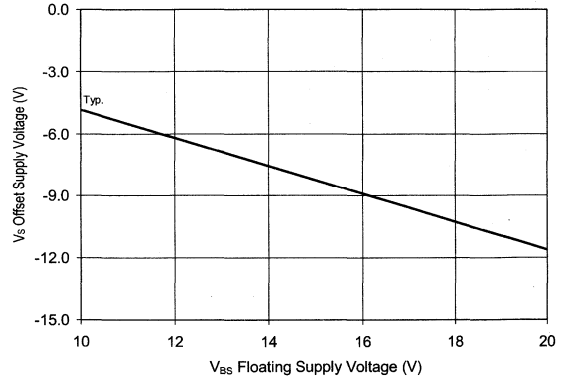


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

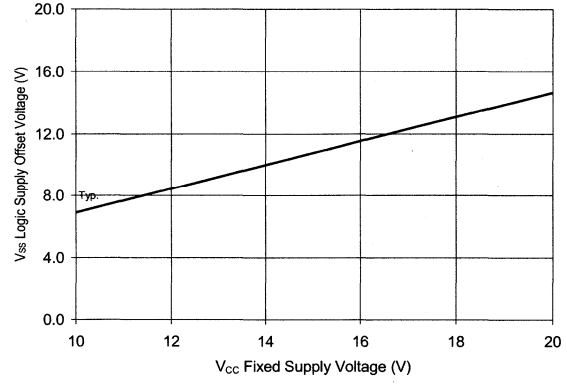
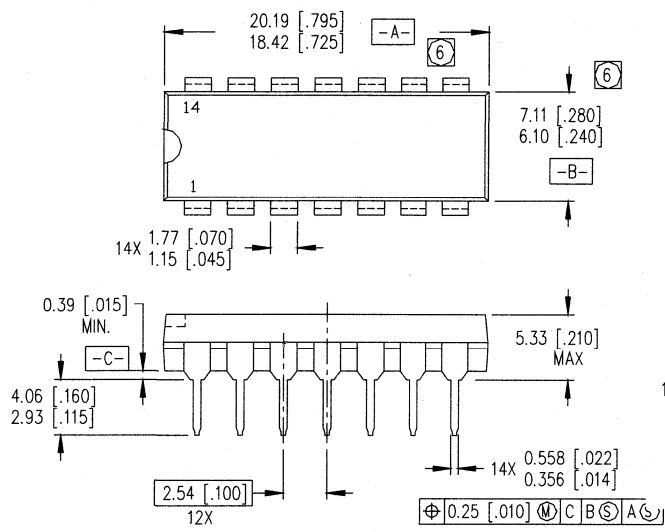
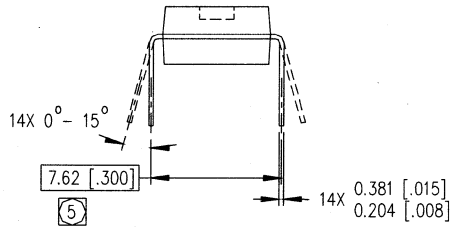


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

Case Outlines

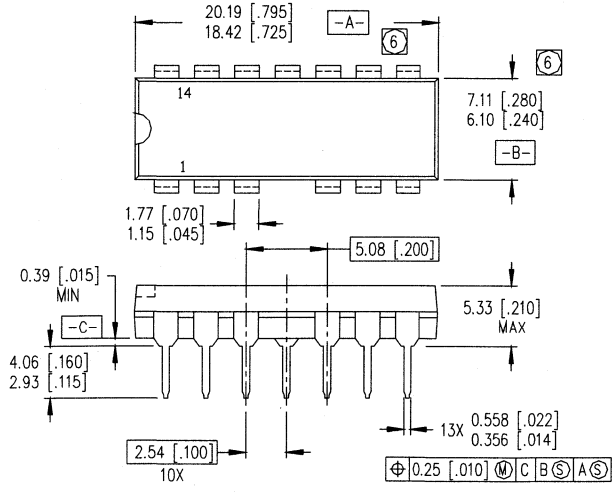


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

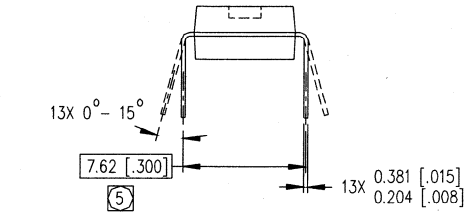


14 Lead PDIP

01-3002 03

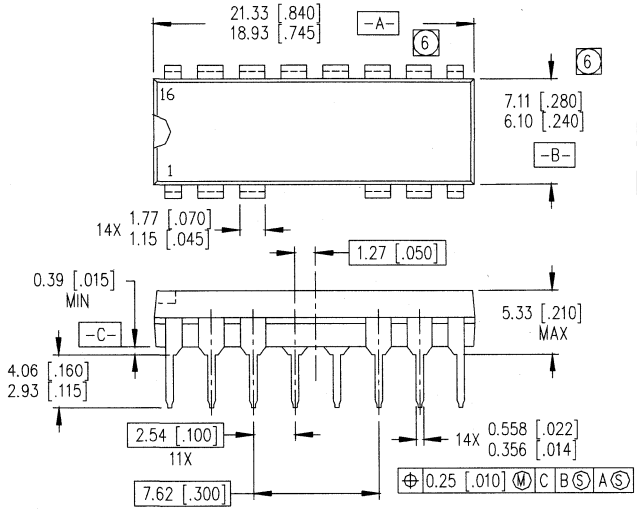


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



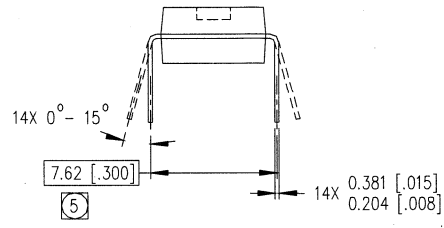
14 Lead PDIP w/o Lead 4

01-3008 02



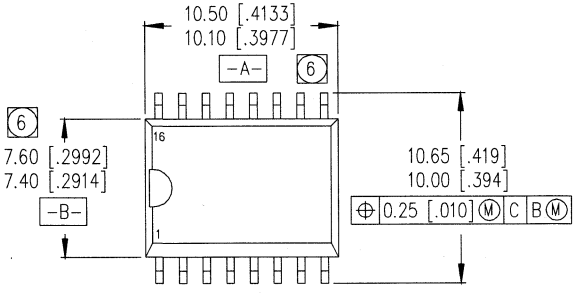
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



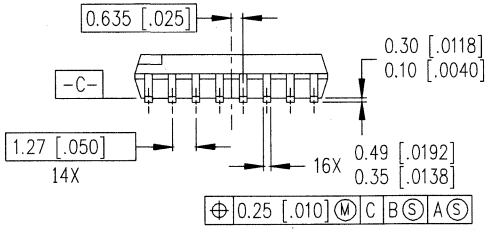
16 Lead PDIP w/o Leads 4 & 5

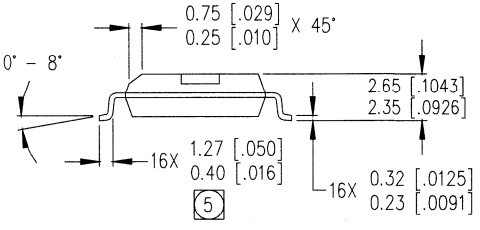
01-3010 02



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].





16 Lead SOIC (wide body)

01-3014 03

4/12/2000

International
IOR Rectifier

ADVANCE INFORMATION Data Sheet No. PD60177-B

IR4426/IR4427/IR4428

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 to 20V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs (IR4426)
- Outputs in phase with inputs (IR4427)
- OutputA out of phase with inputA and OutputB in phase with inputB (IR4428)

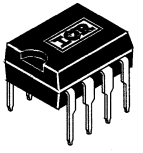
Descriptions

The IR4426/IR4427/IR4428 is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

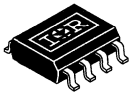
Product Summary

$I_{O+/-}$	1.5A / 1.5A
V_{OUT}	6V - 20V
$t_{on/off}$ (typ.)	85 & 65 ns

Packages

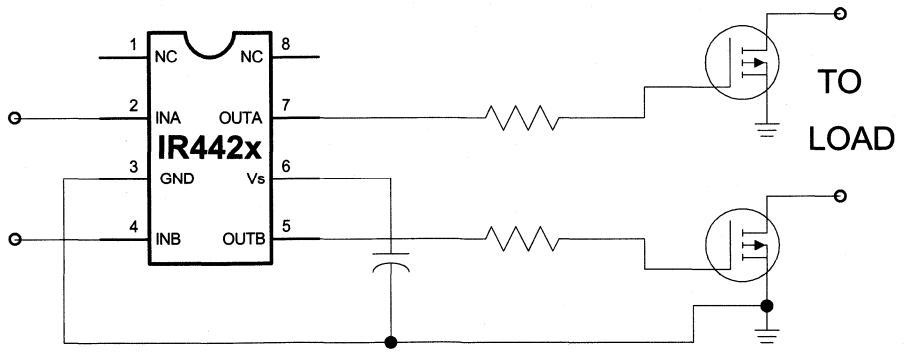


8 Lead PDIP



8 Lead SOIC

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	Fixed supply voltage		-0.3	25	V
V_O	Output voltage		-0.3	V_S + 0.3	
V_{IN}	Logic input voltage		-0.3	V_S + 0.3	
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	6	20	V
V_O	Output voltage	0	V_S	
V_{IN}	Logic input voltage	0	V_S	
T_A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4426) Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4427) Logic "0" input voltage (OUTA=LO), Logic "1" input voltage (OUTB=HI) (IR4428)	2.7	—	—	V	

DC Electrical Characteristics cont.

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

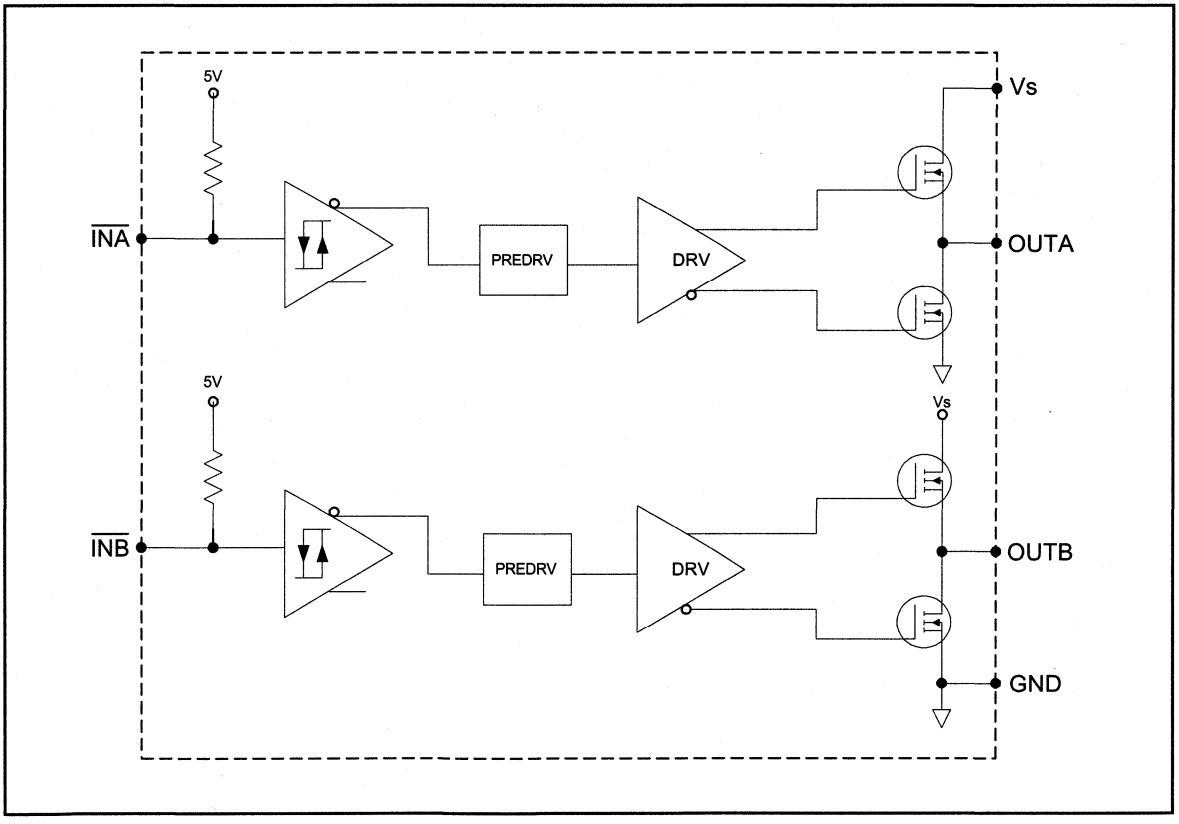
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4426) Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4427) Logic "I" input voltage (OUTA=HI), Logic "0" input voltage (OUTB=LO) (IR4428)	—	—	0.8	V	
V_{OH}	High level output voltage, V_{BIAS}-V_O	—	—	1.2		
V_{OL}	Low level output voltage, V_O	—	—	0.1		
I_{IN+}	Logic "1" input bias current (OUT=HI)	—	5	15	µA	V_{IN} = 0V (IR4426) V_{IN} = V_S (IR4427) V_{INA} = 0V (IR4428) V_{INB} = V_S (IR4428)
I_{IN-}	Logic "0" input bias current (OUT=LO)	—	-10	-30		V_{IN} = V_S (IR4426) V_{IN} = 0V (IR4427) V_{INA} = V_S (IR4428) V_{INB} = 0V (IR4428)
I_{QS}	Quiescent Vs supply current	—	100	200		V_{IN} = 0V or V_S
I_{O+}	Output high short circuit pulsed current	1.5	2.3	—	A	V_O = 0V, V_{IN} = 0 (IR4426) V_O = 0V, V_{IN} = V_S (IR4427) V_O = 0V, V_{INA} = 0 (IR4428) V_O = 0V, V_{INB} = V_S (IR4428) PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.5	3.3	—		V_O = 15V, V_{IN} = V_S (IR4426) V_O = 15V, V_{IN} = 0 (IR4427) V_O = 15V, V_{INA} = V_S (IR4428) V_O = 15V, V_{INB} = 0 (IR4428) PW ≤ 10 µs

AC Electrical Characteristics

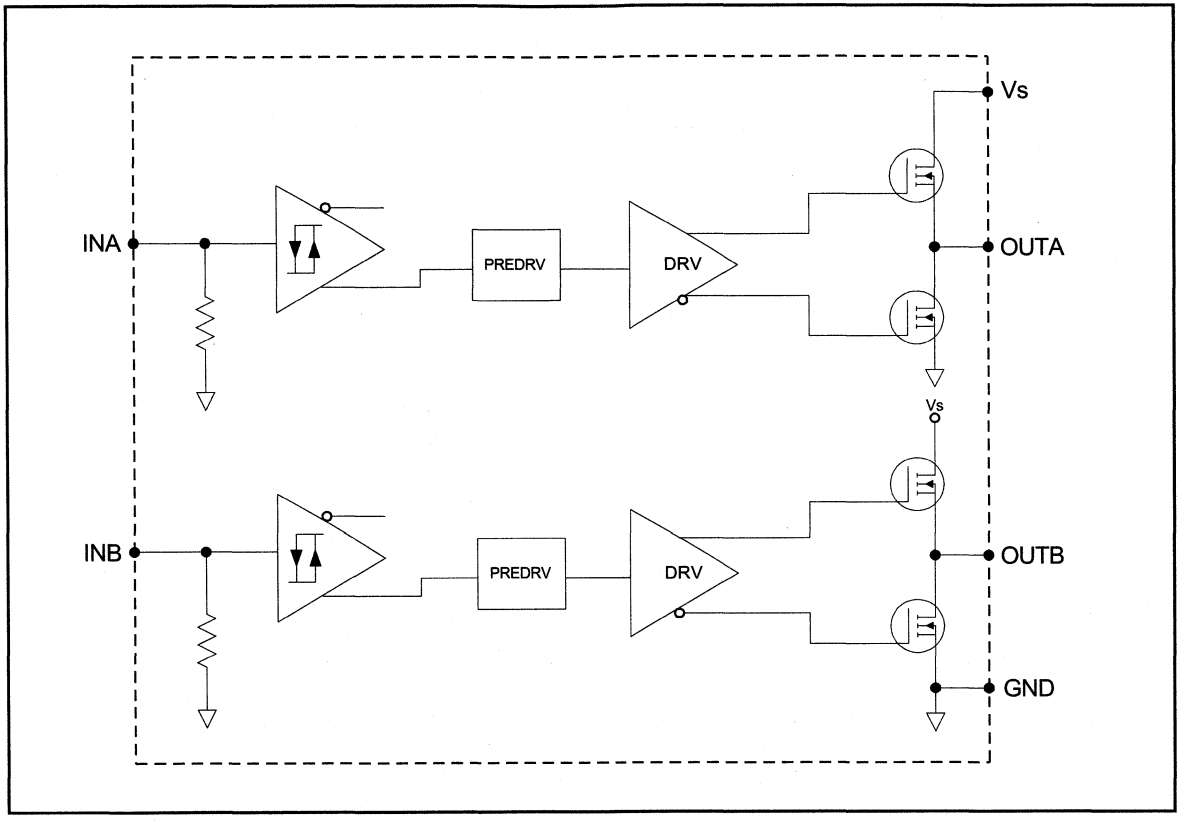
V_{BIAS} (V_S) = 15V, CL = 1000pF, T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
t_{d1}	Turn-on propagation delay	—	85	160	ns	figure 4
t_{d2}	Turn-off propagation delay	—	65	150		
t_r	Turn-on rise time	—	15	35		
t_f	Turn-off fall time	—	10	25		

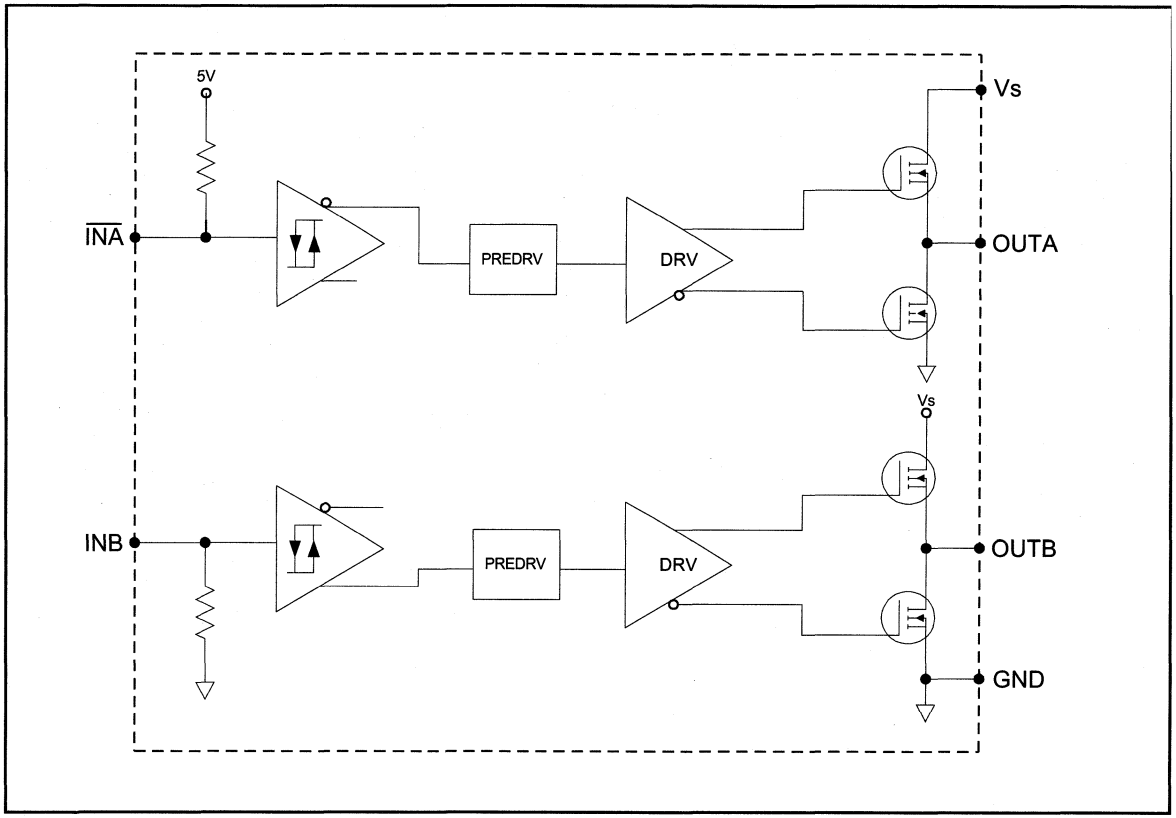
Functional Block Diagram IR4426



Functional Block Diagram IR4427



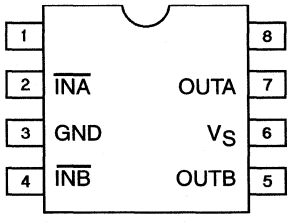
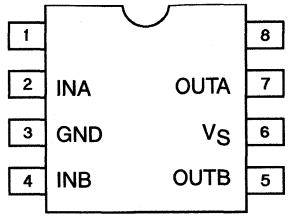
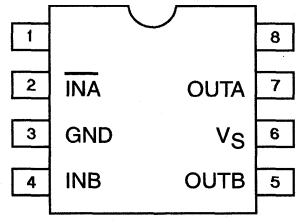
Functional Block Diagram IR4428



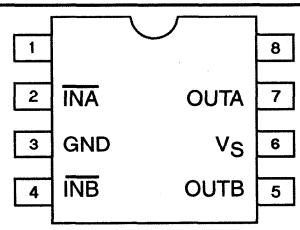
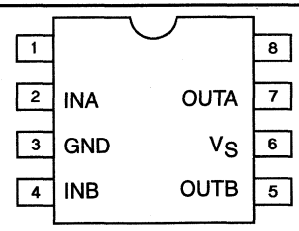
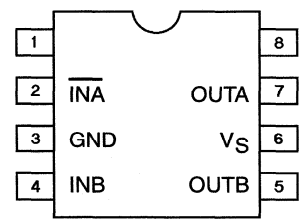
Lead Definitions

Symbol	Description
V_S	Supply voltage
GND	Ground
INA	Logic input for gate driver output (OUTA), out of phase (IR4426, IR4428), in phase (IR4427)
INB	Logic input for gate driver output (OUTB), out of phase (IR4426), in phase (IR4427, IR4428)
OUTA	Gate drive output A
OUTB	Gate drive output B

Lead Assignments

		
8 Lead PDIP	8 Lead PDIP	8 Lead PDIP
IR4426	**IR4427**	**IR4428**
Part Number		

Lead Assignments

		
8 Lead SOIC	8 Lead SOIC	8 Lead SOIC
IR4426S	**IR4427S**	**IR4428S**
Part Number		

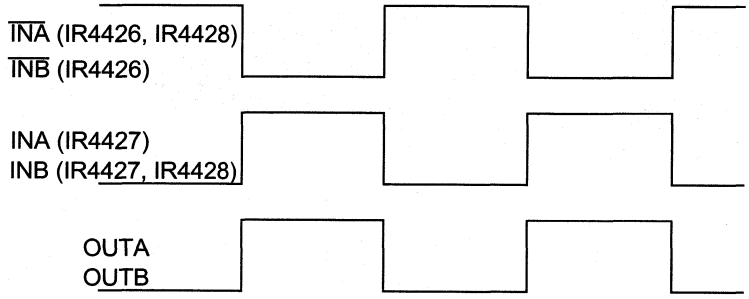


Figure 3. Timing Diagram

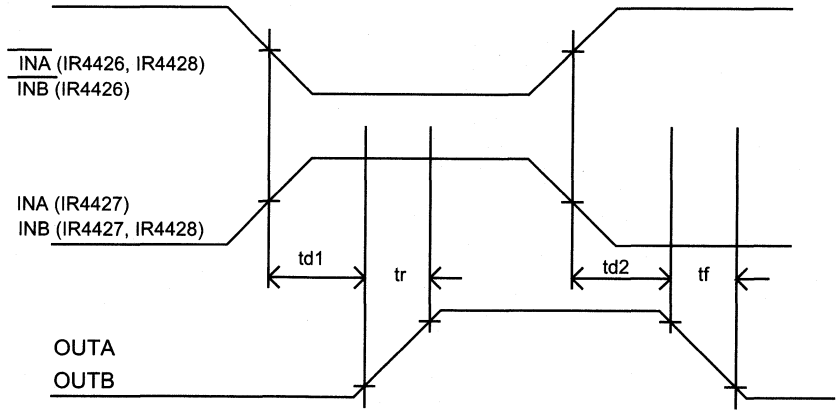


Figure 4. Switching Time Waveforms

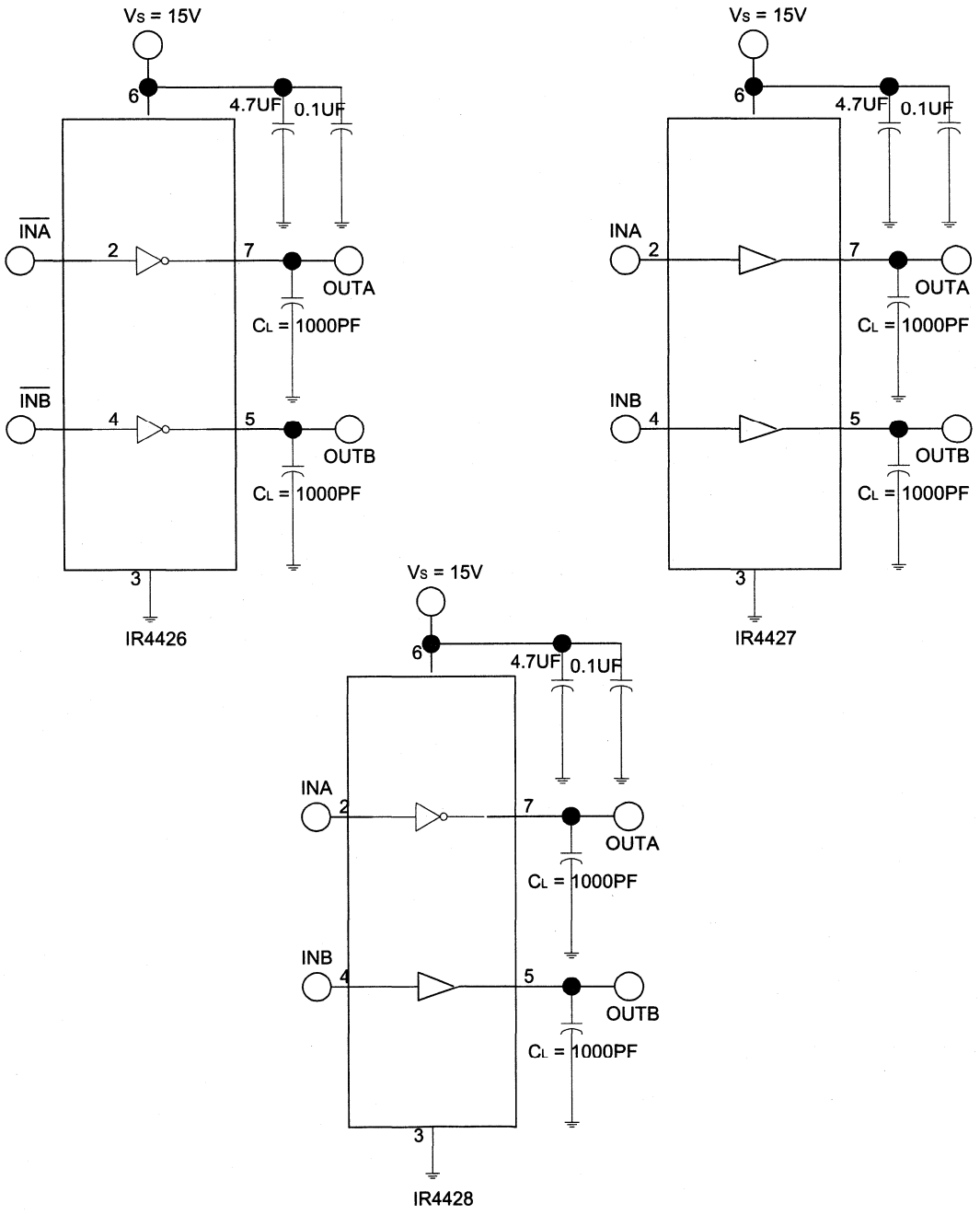
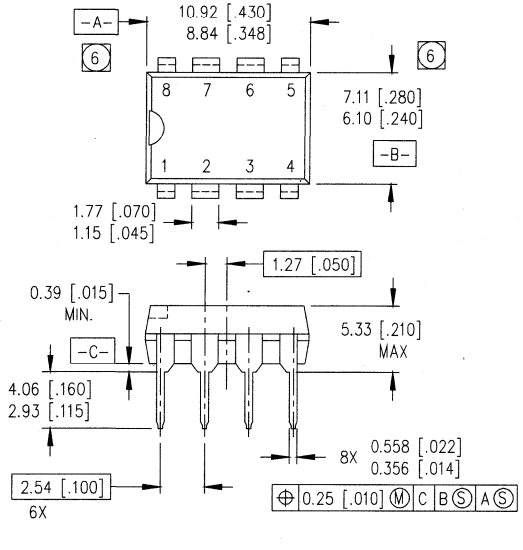


Figure 5. Switching Time Test Circuits

Caseoutline

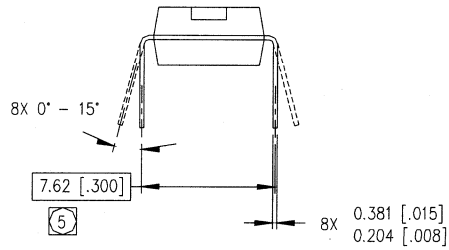


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.

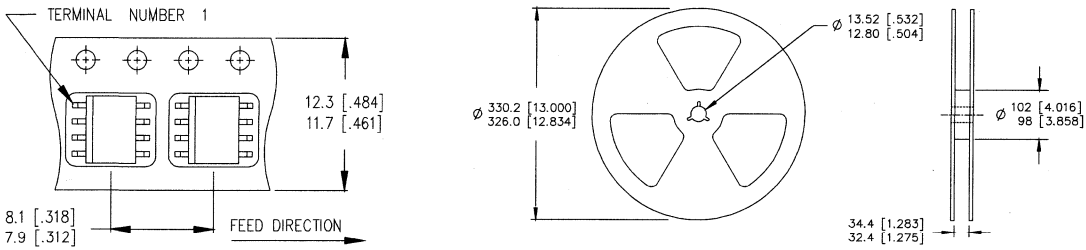
5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP 01-3003 01

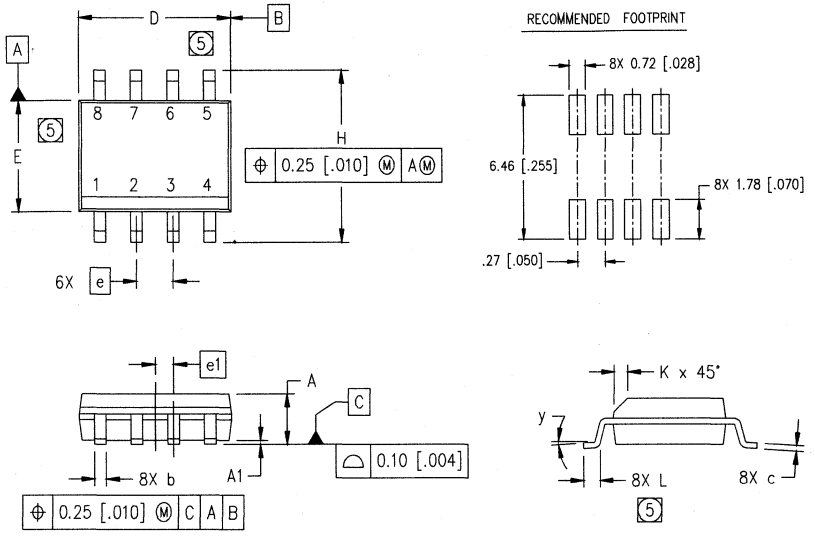
Tape & Reel



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. OUTLINE CONFORMS TO EIA–481 & EIA–541.

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

SPECIAL FUNCTION IC DATA SHEETS

SPECIAL FUNCTION IC

IR3220

FULLY PROTECTED H-BRIDGE FOR D.C. MOTOR

Features

- Over temperature shutdown
- Over current shutdown
- Inrush current limited by Soft-Start sequence
- E.S.D protection
- Status feedback
- Sleep mode for direct battery connection
- Braking/non-braking operation

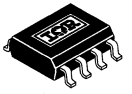
Description

The IR 3220 is a Fully Protected Dual High Side Switch I.C . With two additional Low Side switches (e.g. IRF7413), the IR 3220 drives and controls the whole H bridge topology. It provides shoot-through protection for each leg, H bridge logic control, soft-start sequence and over-current /over-temp. protections. The signals IN1 and IN2 select the operation modes and the PWM Soft-Start sequence cycles the corresponding active low side switch in order to limit the motor inrush current. By using the recommended part number and the proper cooling, the inner High Side IPS protects the whole H bridge function. The Soft-Start sequence is programmed by an RC time constant and reset itself automatically.

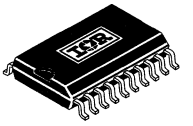
Product Summary

$R_{ds(on)}$	12mΩ typ.
$V_{cc.op.}$	5.5 to 35V
I cont. (Ta = 85°C)	7.0A
$I_{shutdown}$	30A
Oper. Freq.	20 kHz

Packages

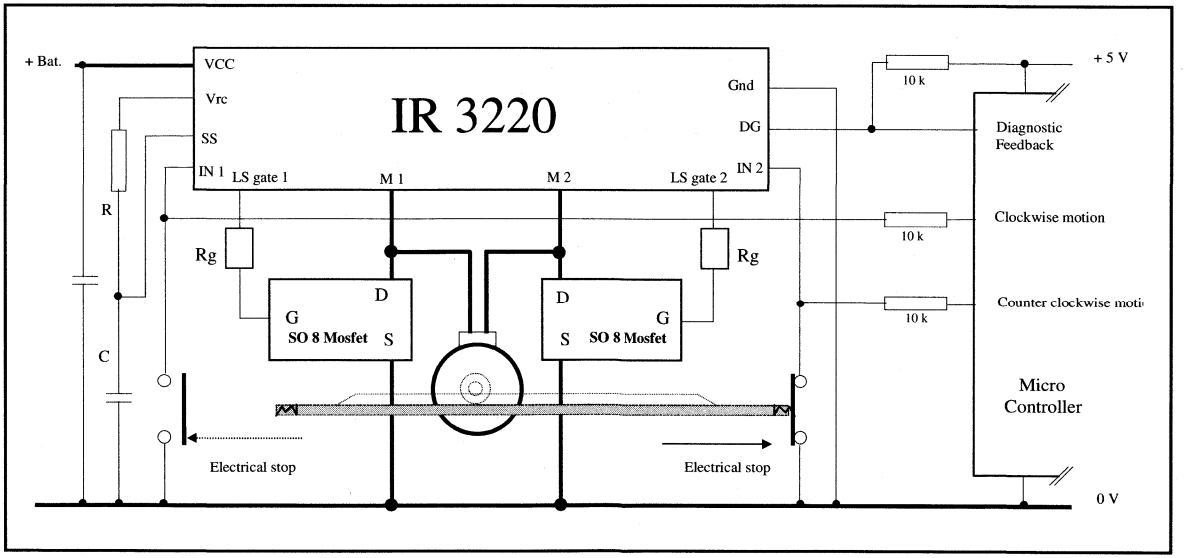


8 Lead SOIC
(e.g. IRF7413)



20 Lead SOIC (wide body)
(IR3220)

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicates sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to Gnd lead. ($T_{Ambient}$ = 25°C unless otherwise specified). Symbols with (2) refer to M2 output

Symbol	Parameter	Min.	Max.	Units
V_{m1} (2)	Maximum M1 (M2) voltage (active clamp)	Vcc-37	Vcc+0.3	V
V_{in1} (2)	Maximum IN 1 (IN 2) voltage	-0.3	5.5	
I in1 (2)	Maximum IN1 (IN 2) current	-1	10	mA
Vg1 (2)	Maximum Gate 1 (Gate 2) voltage	-0.3	7.5	V
Vss	Maximum SS voltage	-0.3	5.5	
Vrc	Maximum Vrc voltage	-0.3	5.5	
Irc	Maximum output current of the Vrc pin	—	1	mA
Vdg	Maximum diagnostic output voltage	-0.3	5.5	V
Idg	Maximum diagnostic output current	-1	10	mA
Isd cont.	Diode max. permanent current (Rth=60°C/W) (1)	—	3.0	A
	(Rth=45°C/W) (1)	—	4.0	
Isd pulsed	Diode max. pulsed current (1)	—	15	
ESD 1	Electrostatic discharge (human body model C=100pF, R=1500Ω)	—	tbd	V
ESD 2	Electrostatic discharge (machine model C=200pF, R=0Ω, L=10μH)	—	tbd	
PD	Maximum power dissipation (Rth = 60°C/W)	—	1.5	W
TJ max.	Max. storage & operating junction temperature	-40	+150	°C
T_L	Lead temperature (soldering 10 seconds)	—	300	
Vcc max.	Maximum Vcc voltage	—	37	V
Ig1 (2) max.	Maximum gate current (Ton < 5μS)	—	100	mA
Ig1 (2) avg.	Maximum average gate current	—	10	mA

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
R_{th} 1	Thermal junction to amb. resistance (stnd footprint 1 MOS on)	60	—	°C/W
R_{th} 2	Thermal junction to ambient resistance (1" sq. footprint 1 MOS on)	45	—	

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
Vcc	Continuous Vcc voltage (2)	8	18	V
V_{in1} (2)	High level IN 1 (IN 2) input voltage	4	5.5	
V_{in1} (2)	Low level IN 1 (IN 2) input voltage	-0.3	0.9	
Iout Ta=85°C	Continuous output current (Rth/amb < 5 °C/W, Tj = 125°C)	—	7.0	A
Iout Ta=105°C	Continuous output current (Rth/amb < 5 °C/W, Tj = 125°C)	—	4.5	
R in	Recommended resistor in series with IN pin	10	20	kΩ
R dg	Recommended pull-up resistor on DG pin	1	20	
R	Soft-Start resistor	5.0	100	
C	Soft-Start capacitor	0.1	3.3	µF
R gate	Recommended gate resistor for Low Side Switch	0	50	Ω

Static Electrical Characteristics

(T_j = 25°C, V_{CC} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Rds1 on	ON state resistance Tj = 25°C	—	12	—	mΩ	Vin1,2 = 5V;1m1,2 = 5A
Rds2 on	ON state resistance Tj = 150°C	—	20	—		
Vcc oper.	Functional voltage range	5.5	—	35	V	
Vclamp1 (2)	Vcc to M1 (M2) clamp voltage	37	40	48		Id =10mA see Figs.1,2
Vf1 (2)	Body diode 1 (2) forward voltage	—	0.9	—		Id = 5A, Vin1,2 = 0V
IM1 (2) leakage	M1 (M2) output leakage current	—	10	50	µA	Vm1, 2 = 0V; Tj = 25°C
Icc off	Supply current when off (sleep mode)	—	10	50		
Icc on	Supply current when on	—	8	—	mA	Vin1 = 5V
Vdgl	Low level diagnostic output voltage	—	0.3	—	V	Idg = 1.6mA
Idg leakage	Diagnostic output leakage current	—	—	10	µA	Vdg = 5.5V
Vih1 (2) th.	IN1 (IN2) high threshold voltage	—	2.6	—	V	
Vil1 (2) th.	IN1 (IN2) low threshold voltage	—	2.0	—		
Iin1 (2)	ON state IN1 (IN2) positive current	—	25	—	µA	Vin1, 2 = 5V
Vccuv	Vcc UVLO positive going threshold	—	5	—	V	
Vccuv-	Vcc UVLO negative going threshold	—	4	—		
Vss+	SS high level threshold	—	4	—		
Vss-	SS low level threshold	—	1	—		
Iss leakage	SS pin leakage current	—	0.1	10	µA	

Switching Electrical Characteristics

V_{CC} = 14V, Resistive Load = 0.4Ω, T_j = 25°C, (unless otherwise specified).

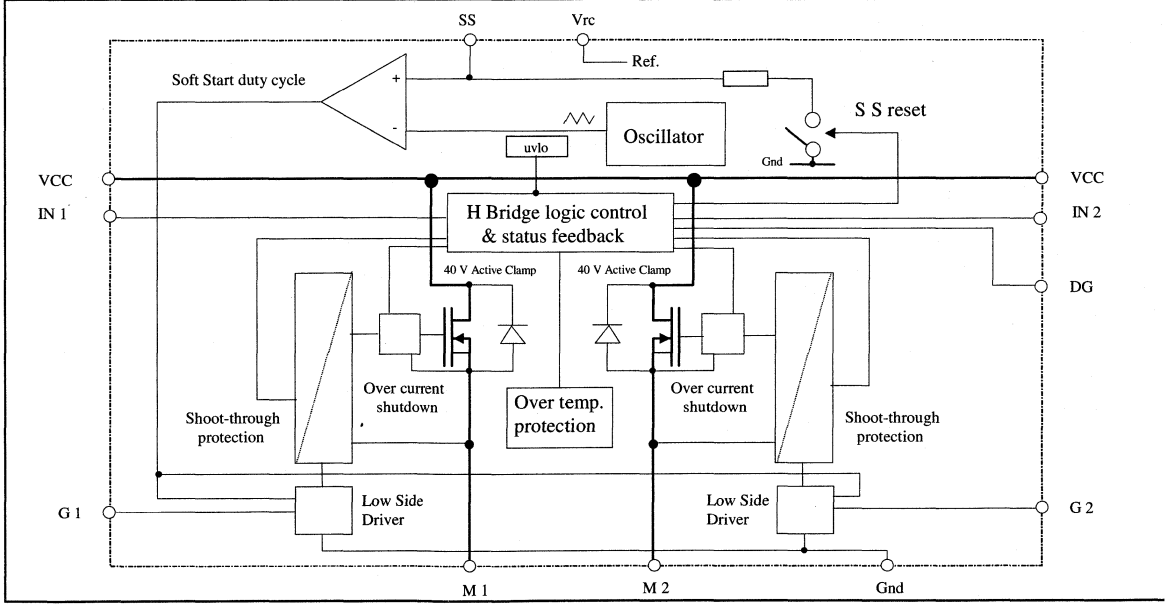
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Td_{on}	Turn-on delay time	—	5	—	µs	see figure 3
T_{r1}	Rise time to Vout = Vcc -5V	—	4	—		
Tr2	Rise time from the end of Tr1 to V_{out} = 90% of V_{CC}	—	65	—		
dV/dt (on)	Turn ON dV/dt	—	3	—	V/µs	
Tdoff	Turn-off delay time	—	65	—	µs	see figure 4
Tf	Fall time to Vout = 10% of Vcc	—	8	—		
dV/dt (off)	Turn OFF dV/dt	—	5	—	V/µs	
IN1 (2) max. freq.	Max. frequency on IN1 (IN2)	—	500	—	Hz	
Soft-Start freq.	Soft-Start oscillator frequency	15	20	30	kHz	
Ig1 (2) min.	Min. Gate 1 (Gate 2) current	50	—	—	mA	low side driver
Trd	Min. IN1 (2) OFF time to reset SS	2.0	—	—	ms	C=3.0µF, IN1 = IN2
Vg1	Gate 1 (gate 2) voltage	—	7	—	V	

Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Tsd	Over-temperature threshold	—	165	—	°C	See figure 2
Isd	Over-current threshold	25	30	35	A	See figure 2
Treset	Minimum time to reset protections	—	100	—	µS	IN1 = IN2 = 0V

Note: The low side switches present sufficient cooling capability in order to have the whole H Bridge function protected by the IR3220 inner temperature sensor.

Functional Block Diagram



Truth Table

IN1	IN2	MODES	DG	HS1	LSS1	HS2	LSS2	SS reset
L	L	Stand-by with braking - sleep mode**	H	OFF	ON	OFF	ON	ON
L	H	Foward rotation (normal operation)	H	OFF	ON*	ON	OFF	OFF
L	H	Foward rotation (protection triiggered)	L	OFF	ON*	OFF	OFF	OFF
H	L	Reverse rotation (normal operation)	H	ON	OFF	OFF	ON*	OFF
H	L	Reverse rotation (protection triggered)	L	OFF	OFF	OFF	ON*	OFF
H	H	Stand-by without braking	H	OFF	OFF	OFF	OFF	ON

* During Soft-start sequence, the low side part is switching. ** Protections are reset in this mode

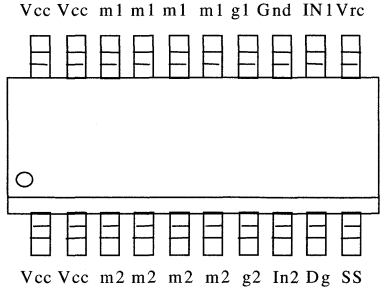
Lead Definitions

Vcc	Positive power supply	IN1	Logic input 1 (Leg 1 Cdt. / mode)
M1	Motor 1 output (high side source - leg 1)	IN2	Logic input 2 (Leg 2 Cdt. / mode)
M2	Motor 2 output (high side source - leg 2)	Dg	Diagnostic output (open drain)
G1	Gate 1 drive output (low side gate - leg 1)	Vrc	Voltage ref. output (soft-start RC)
G2	Gate 2 drive output (low side gate - leg 2)	SS	RC soft-start input (the voltage on this input drives the switching duty cycle)
Gnd	Power supply return		

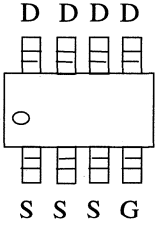
Recommended Low Side MOSFET

e.g. IRF7413 OR a 10mΩ /40V - SOIC 8 packaged Power Mosfet

Lead Assignments



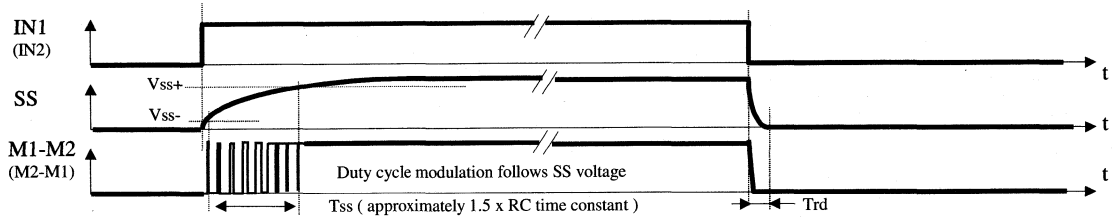
20 Lead - SOIC (wide body)



8 Lead - SOIC

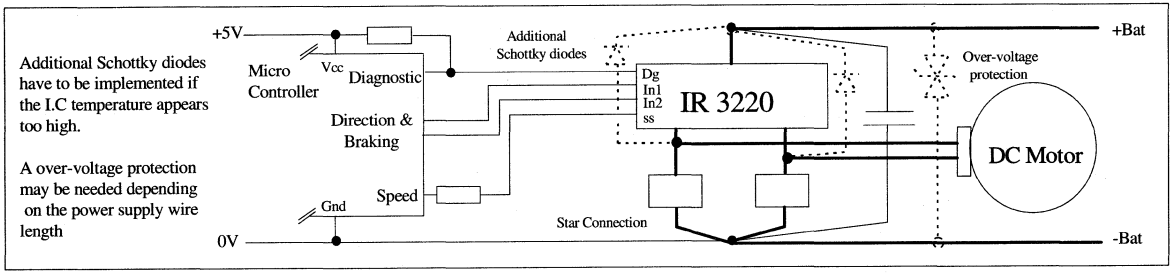
IR3220	e.g. IRF7413
Part Number	

Sof-start sequence



Permanent Switching Operation

(without external RC time constant)



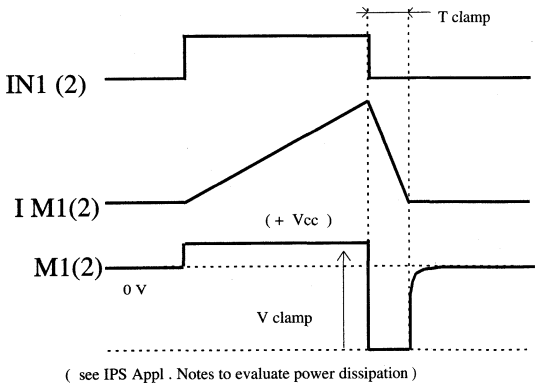


Figure 1 - Active clamp waveforms

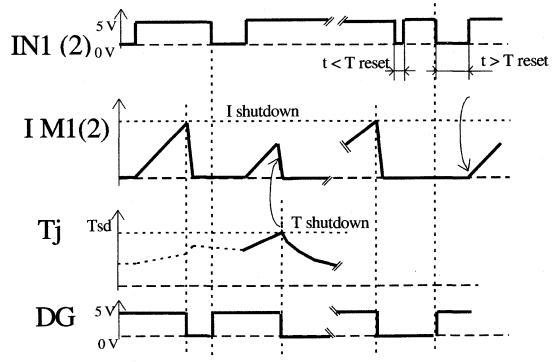


Figure 2 - Protection Timing diagram

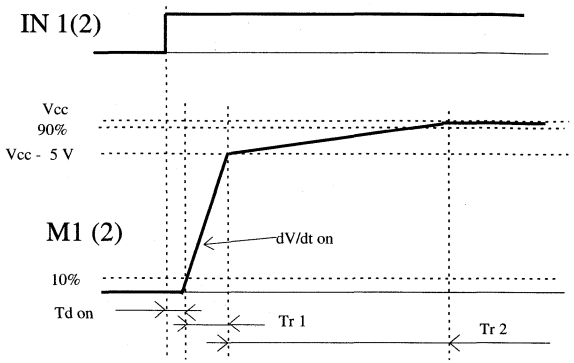


Figure 3 - Switching Time Definitions (turn-on)

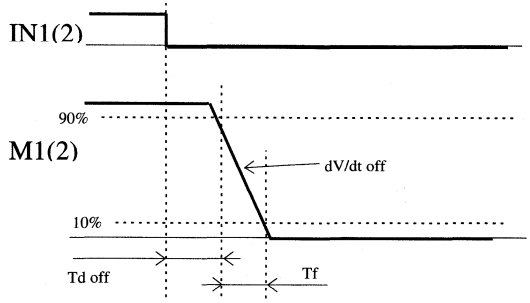


Figure 7 - Switching Time Definitions (turn-off)

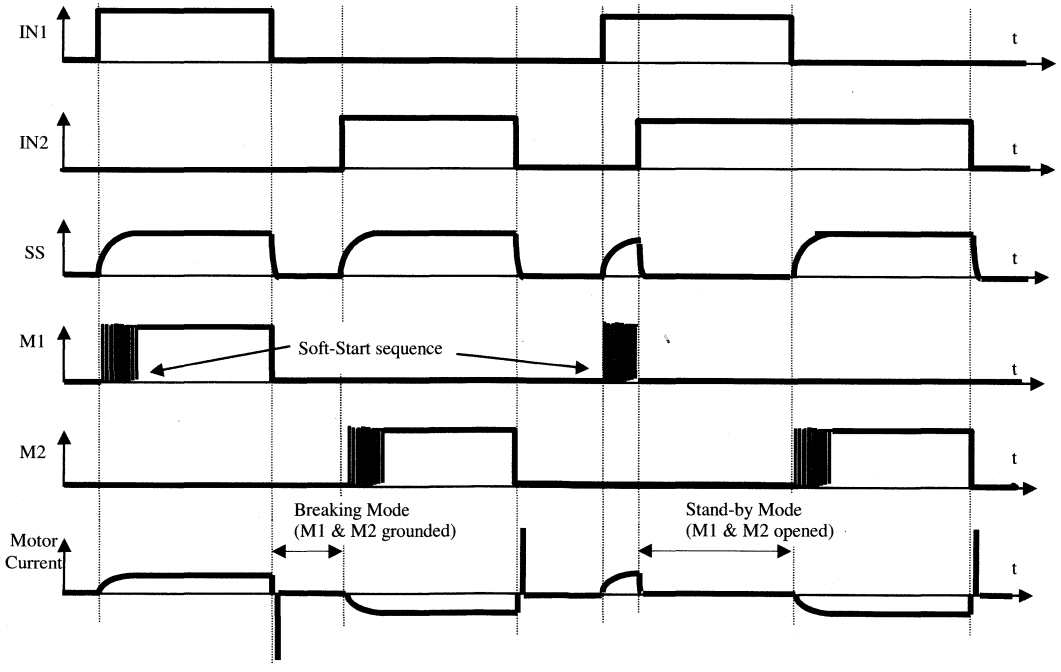


Figure 5 - IN1 (2) & M1 (2) Timing Diagrams

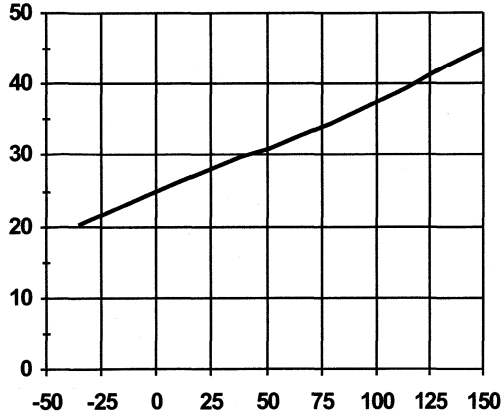


Figure 6 - IN1 (2) current (μA) vs Tj (°C)

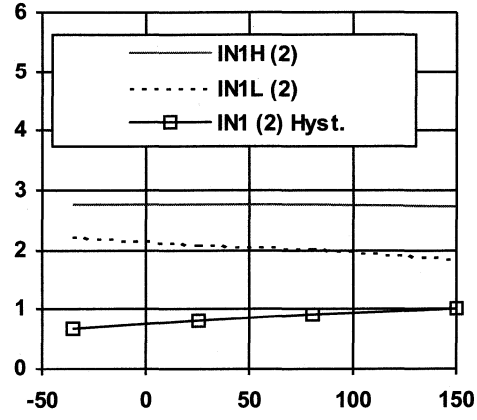


Figure 7 - IN1 (2) thresholds (V) vs Tj (°C)

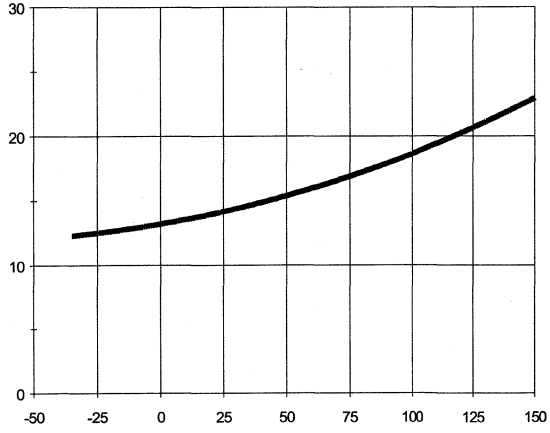


Figure 8 - Rdson (mΩ) vs Tj (°C)

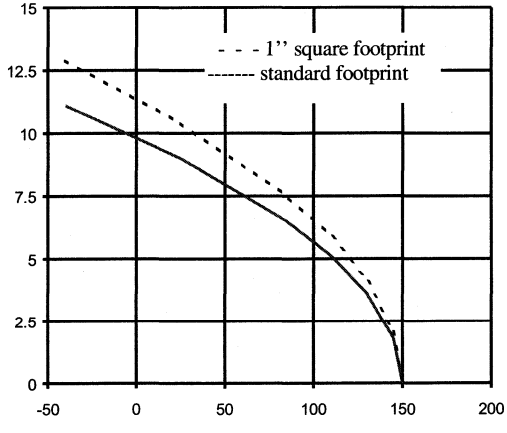


Figure 9 - Max. Cont. current (A) vs Amb. Temp. (°C)

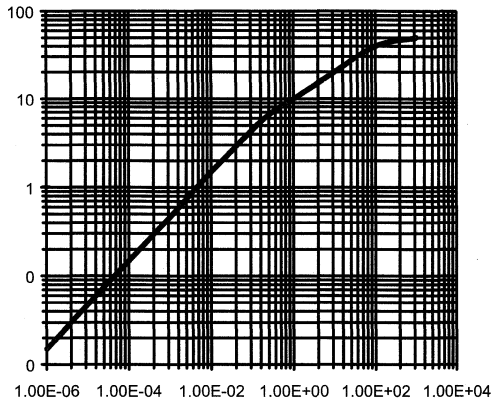


Figure 10 - Transient Thermal Imped. (°C/W) vs Time (s)

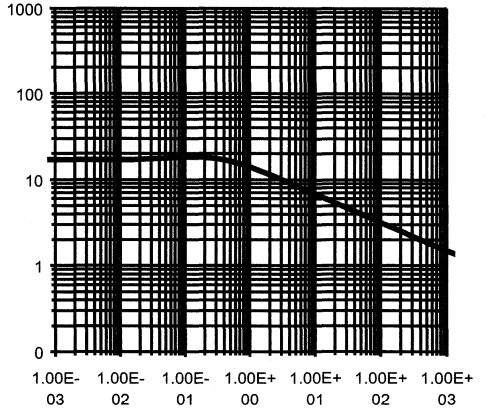
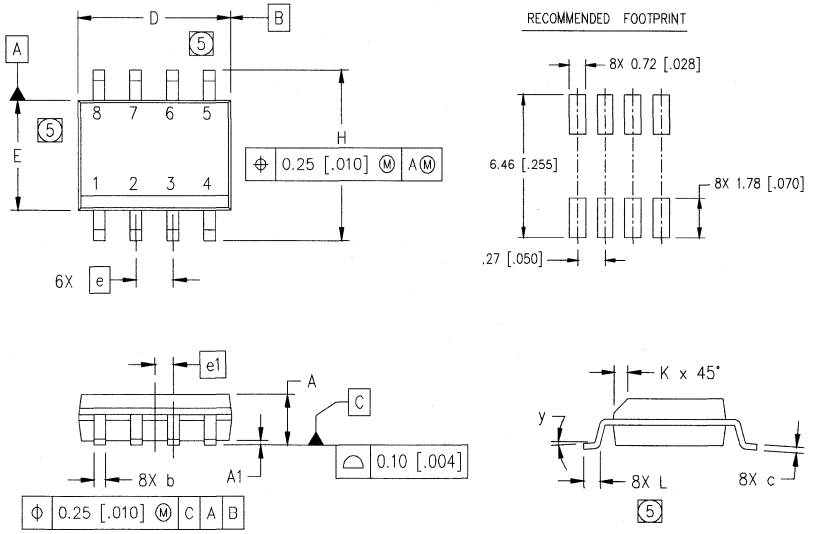


Figure 11 - Iclamp (A) vs Power Supply Wire Inductance (mH - single pulse)

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

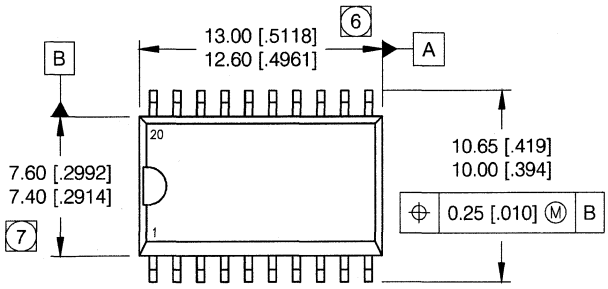
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

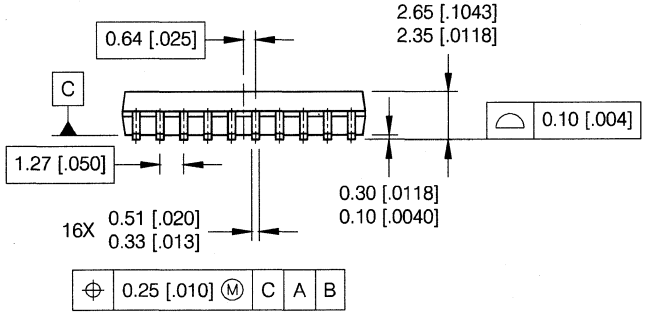
(MS-012AA) 01-0021 09

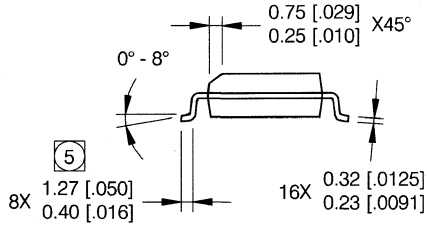
Case Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AC.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
7. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].





20 Lead SOIC (wide body) (MS-013AC) 01-3080 00

IR3310

PROGRAMMABLE CURRENT SENSING HIGH SIDE SWITCH

Features

- Load current feedback
- Programmable over current shutdown
- Active clamp
- E.S.D protection
- Input referenced to Vcc
- Reverse battery protection (reverse current operation)

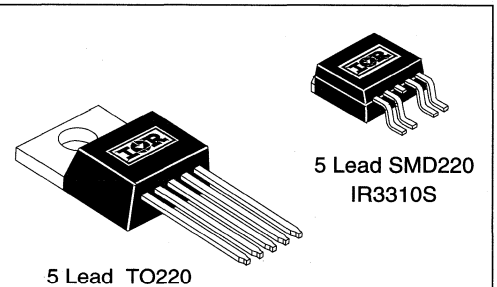
Description

The IR 3310 is a Fully Protected 4 terminal high side switch. The input signal is referenced to Vcc. When the input voltage Vcc - Vin is higher than the specified Vih threshold, the output power MOSFET is turned-on. When Vcc - Vin is lower than the specified Vil threshold, the output MOSFET is turned-off. A sense current proportional to the current in the power Mosfet is sourced to the ST pin. Over-current shutdown occurs when Vst - Vin > 4 V. Choosing Rst allows to adjust Isd. Either over-current and over-temperature latches off the switch. The device is reset by pulling the input pin high. Other integrated protections (ESD, reverse battery, active clamp) make the IR 3310 very rugged and suitable for the automotive environment.

Product Summary

$R_{ds(on)}$	5mΩ typ.
$V_{cc.op.}$	5.5 to 35V
Current ratio	10 000
$I_{shutdown}$	10 to 100A
Active clamp	40V

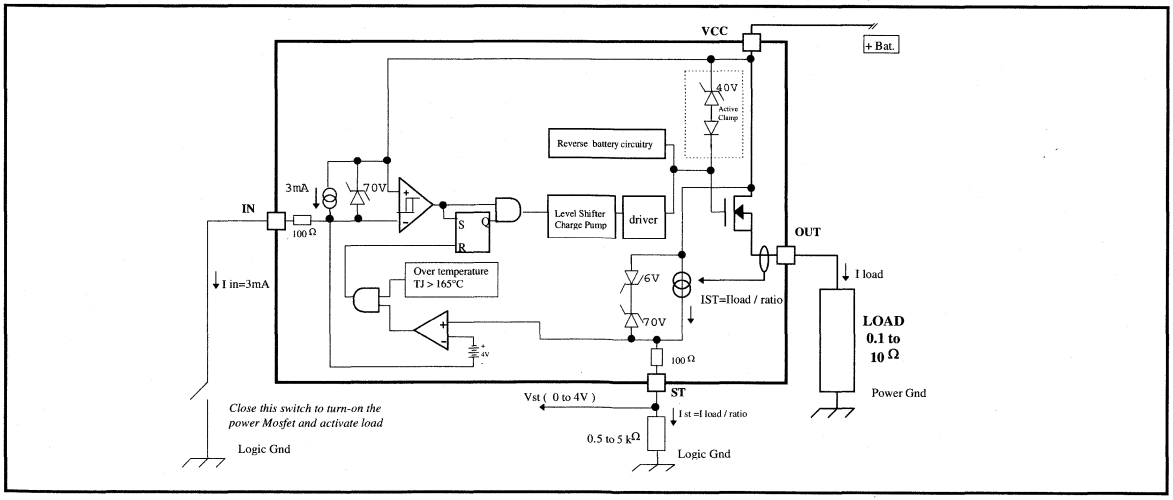
Packages



5 Lead SMD220
IR3310S

5 Lead TO220
IR3310

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicates sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to Vcc lead. ($T_{Ambient}$ = 25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
Vcc - Vin max	Maximum input voltage	-16	50	V
Vcc-Vst max	Maximum status voltage	-16	50	
Vcc - Vout max.	Maximum output voltage	-0.3	37	
Ids cont.	Diode max. permanent current (Rth = 60 °C/W) (1)	—	2.8	A
Ids1 cont	Diode max. permanent current (Rth = 5 °C/W) (1)	—	35	
Ids pulsed	Diode max. pulsed current (1)	—	100	
ESD 1	Electrostatic discharge (human body model)	—	tbd	kV
ESD 2	Electrostatic discharge (machine model)	—	tbd	
Pd	Power dissipation (Rth = 62 °C/W)	—	2	W
TJ max.	Max. storage and junction temperature	-40	150	°C
Min R st	Minimum resistor on the ST pin	0.5	—	kΩ

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
R_{th} free air	Thermal resistance - free air	60	—	°C/W
R_{th} std footprint	Thermal resistance with standard footprint	80	—	°C/W
R_{th}1" footprint	Thermal resistance with 1" footprint	50	—	°C/W
R_{th} junct. to case	Thermal resistance junction to case	5	—	°C/W

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
Vcc - Vin	Continuous input voltage	6	18	V
Vcc-Vst	Continuous status voltage	0	18	
Vcc	Supply to power ground voltage	6	18	
Iout	Continuous output current (Rth/amb < 5 °C/W, Tj = 125°C)	—	35	A
Iout 85°C amb.	Continuous output current (Rth/amb < 5 °C/W, Tj = 125°C)	—	8	
Rst	ST resistor to program Isd and scale (2 & 3)	0.5	5	kΩ

Protection Characteristics

Tj = 25°C (unless otherwise specified), Rst = 500 to 5kOhm.

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
Vst - Vin @ Isd	Over-current shutdown threshold	4	—	V	
Tsd	Over-temp. shutdown threshold	165	—	°C	see Fig. 4
Treset	Protection reset time	50	—	µS	see Fig. 4

1) Limited by junction temperature. Pulsed current is also limited by wiring
2) <500 Ohm or shorting ST to gnd may damage the part with Isd around 120A
3) >5000 Ohm or leaving ST open will shutdown the part. No current will flow in the load.

Static Electrical Characteristics

(T_j = 25°C, V_{CC} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Iq	Quiescent current	—	7	50	uA	Vcc-Vin=0, Vcc-Vout=12V
Iin	Input current	—	3	—	mA	Vcc-Vin=14V
Vih	High level input threshold voltage (4)	—	5	—	V	
Vil	Low level input threshold voltage (4)	—	4	—		
Vhys	Input hysterisis = Vih-Vil	—	1	—		
Rds1 on	ON state resistance	—	5	—	mΩ	Iout=35A, Vcc=14V
Rds2 on	ON state resistance	—	5.5	—		Iout=17A, Vcc-Vin=6V
Rds3 on	ON state resistance	—	8	—		Iout=35A, Tj = 150°C
Vclamp1	Vcc to Vout active clamp voltage	37	40	—	V	Iout = 10mA
Vclamp2	Vcc to Vout active clamp voltage	—	42	48		Iout = 35mA
Vsd	Body diode forward voltage	—	0.85	1		Id=35A, Vcc-Vin=0V

Switching Electrical Characteristics

V_{CC} = 14V, Resistive Load = 0.4Ω, T_j = 25°C, (unless otherwise specified).

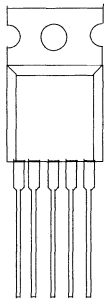
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time to Vcc-Vout= 0.9 Vcc	—	10	—	µs	see figure 2
T_{r1}	Rise time to Vcc-Vout=5V	—	16	—		
T_{r2}	Rise time from end of Tr1 to V_{out} = 10% of V_{CC}	—	300	—		
dV/dt (on)	Turn ON dV/dt	—	1.2	—	V/µs	
E_{on}	Turn ON energy	—	40	—	mJ	see figure 3
T_{off}	Turn-off delay time	—	tbd	—	µs	
T_f	Fall time to Vcc-Vout 90% of V_{CC}	—	tbd	—		
dV/dt (off)	Turn OFF dV/dt	—	tbd	—	V/µs	
E_{off}	Turn OFF energy	—	5	—	mJ	

Current Sense Characteristics

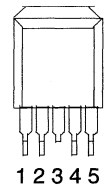
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ratio	I load / I status	—	10,000	—	—	T_j = 25°C ,Rst = 500Ω, I = 100A
Ratio	Gain variation over temperature range error ToC	-5	—	+5	%	T_j = 40 To +150°C
offset	status current when I load = 0	-0.5	0	+0.5	mA	T_j = 25°C ,Rst = 500Ω, I = 100A
offset	Offset variation over temperature range var. ToC	-0.4	0	0.4	mA	T_j = 40 To +150°C
Trst	status response time to a small I load step		10		µs	to get 90% of the I load step

4) Input threshold are measured directly between the input pin and the tab. Any parasitic resistance in common between the load current path and the input signal path can significantly affect the thresholds.

Lead Assignments



1 - In
2 - ST
3 - Vcc (tab)
4 - NC
5 - Out



5 Lead - TO220	5 Lead - SMD220
IR3310	**IR3310S**
Part Number	

The following note applies to all curves: 1) they are all typical characteristics. 2) Operation in shaded area is not recommended. 3) Tj = 25°C, Rst=500Ohm, Vbat =14V (unless otherwise specified).

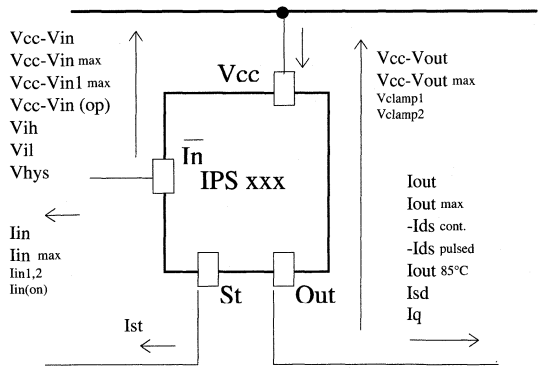


Figure 1 - Voltages and currents definition

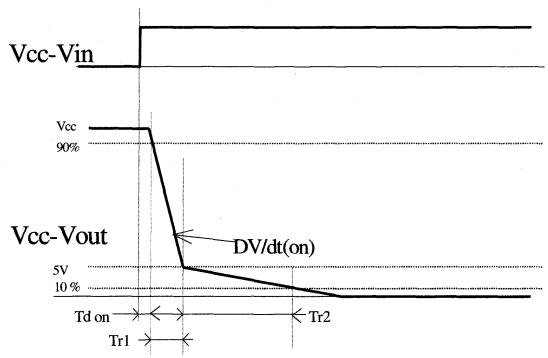


Figure 2 - Switching time definitions (turn-on)

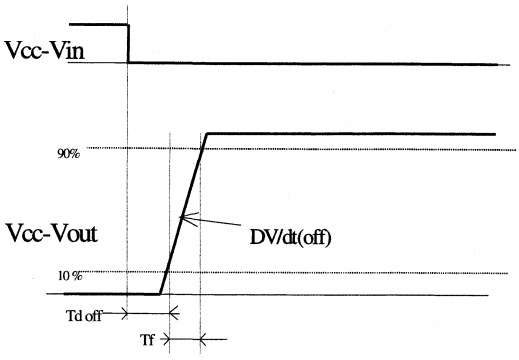


Figure 3 - Switching time definitions (turn-off)

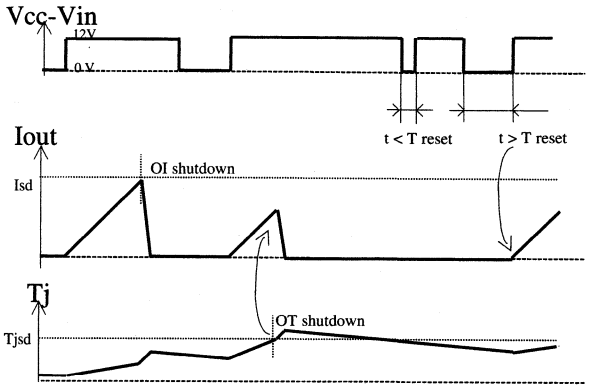
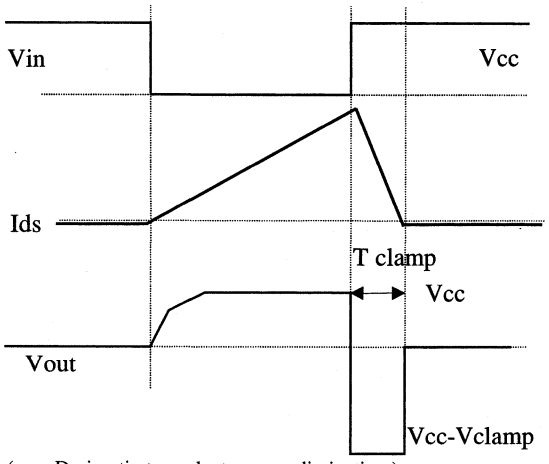


Figure 4 - Protection timing diagram



(see Design tip to evaluate power dissipation)

Figure 5 - Active clamp waveform

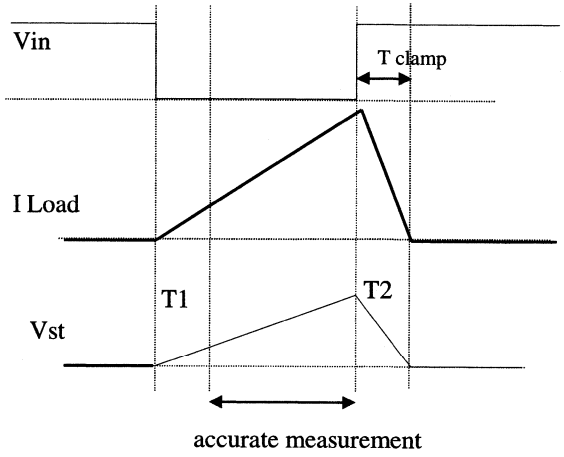


Fig 6 - Current sensing accuracy:
Measurement is accurate only when the power Mosfet is fully on (outside T1=Tdon + Tr1+Tr2) and when the part is not in the active clamp (outside T2).

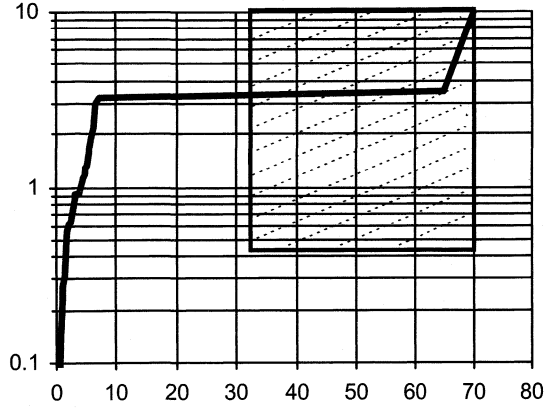


Figure 7 - Icc (mA) vs Vcc-Vin (V)

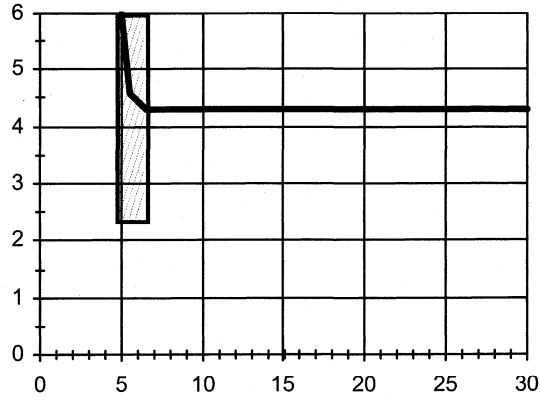


Figure 8 - Rds_{on} (mΩ) vs Vcc-Vin (V)

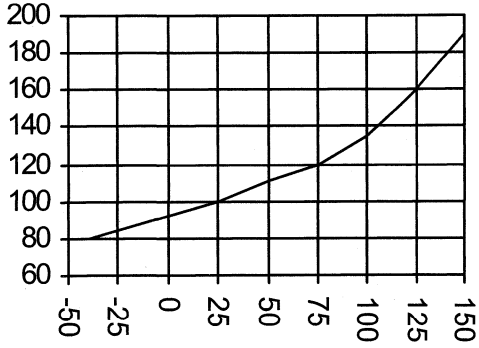


Figure 9 - Normalized Rdson (%) vs Tj (°C)

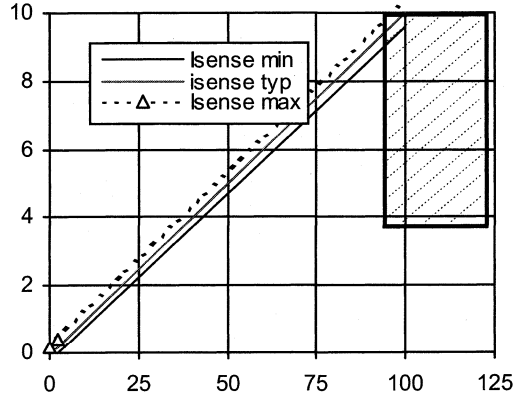


Figure 10 - I sense (mA) vs I load (A)

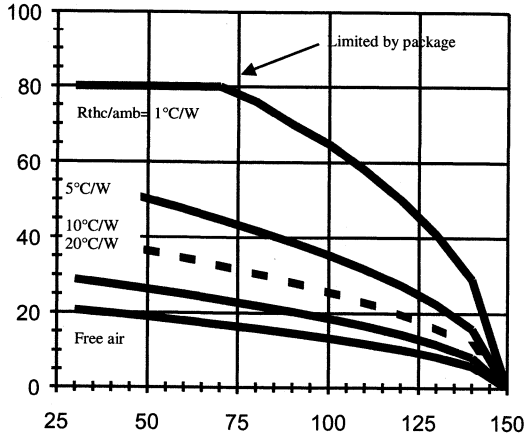


Figure 11 -Isd (A) vs Rst (Ω)

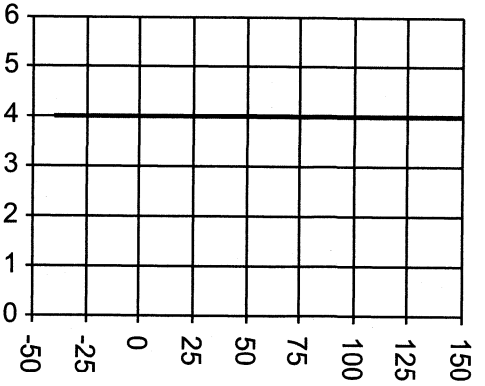


Figure 12 - Vst -Vin (V) vs Tj (°C)

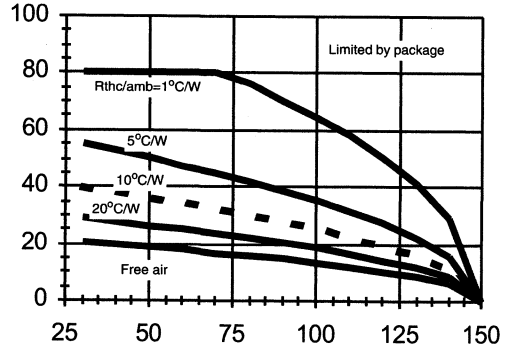


Figure 13 - Max. Cont. Iout (A) vs Temp. (°C)

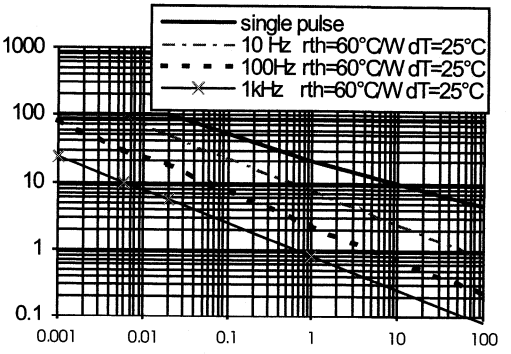


Figure 14 - Max. Iout (A) vs load inductance (uH)

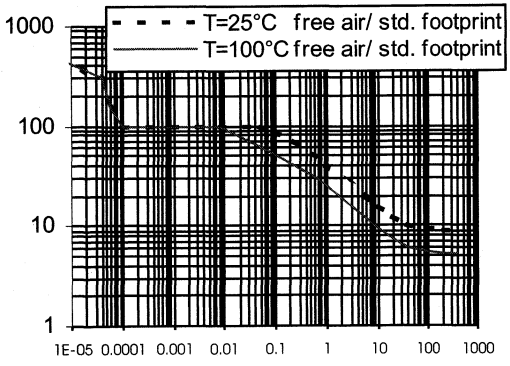


Figure 15 - I out (A) vs Protection resp. Time (s)

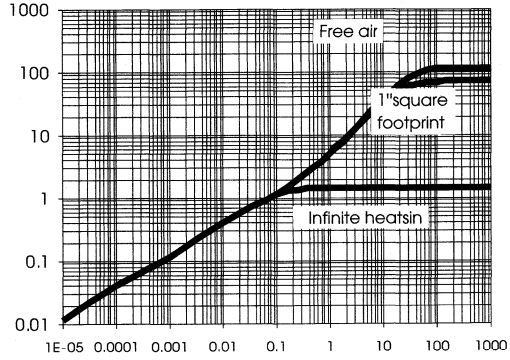


Figure 16 - Transient Rth (°C) vs Time (s)

How to use the IR 3310 device

- Check max. continuous power dissipation :

  Use figure 11 to check that max. continuous load current does not exceed the device capability in worst case ambient temperature.

- Choose Isd so that it exceeds the maximum transient current with a sufficient margin.
  I max. load shall not exceed 100A.

- Choose Rst to get Isd by mean of fig. 10 curve or using the following formula

  $$Isd = (Vst\text{-}Vin\ @\ Isd) * gain / Rst = 4V*10000 / Rst.$$

  This ensures optimum protection and full scale of Vst signal (0V for I load=0 and 4V for I load = Isd).

- To reduce power dissipation during reverse battery operation, the inner circuitry takes the potential available on ST pin in order to turn on the power MOSFET. This principle works only if Rst is within the recommended range (0.5 to 5 kΩ) and Rev.bat. voltage > 5V.

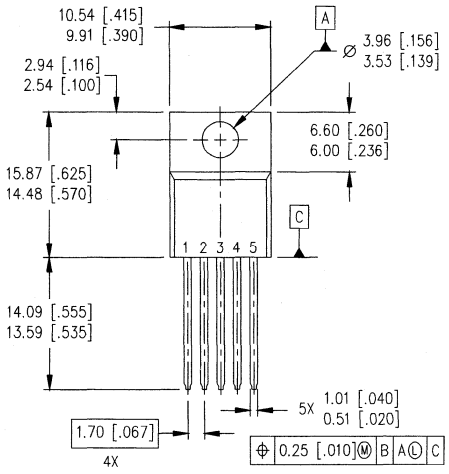
Also, the logic Gnd must not be disconnected from the Power Gnd (due to another reverse battery protection circuitry for example).

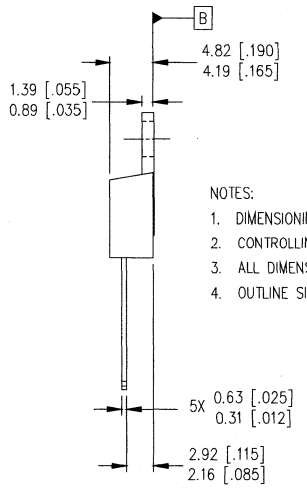
Check that junction temperature does not exceed the max. value (165°C) :

(losses multiplied by rth + max. ambient) <165°C.

Total Losses (w) = Ppower Mosfet + P (in) + P (st)

Case Outline - TO220 (5 lead)





NOTES:

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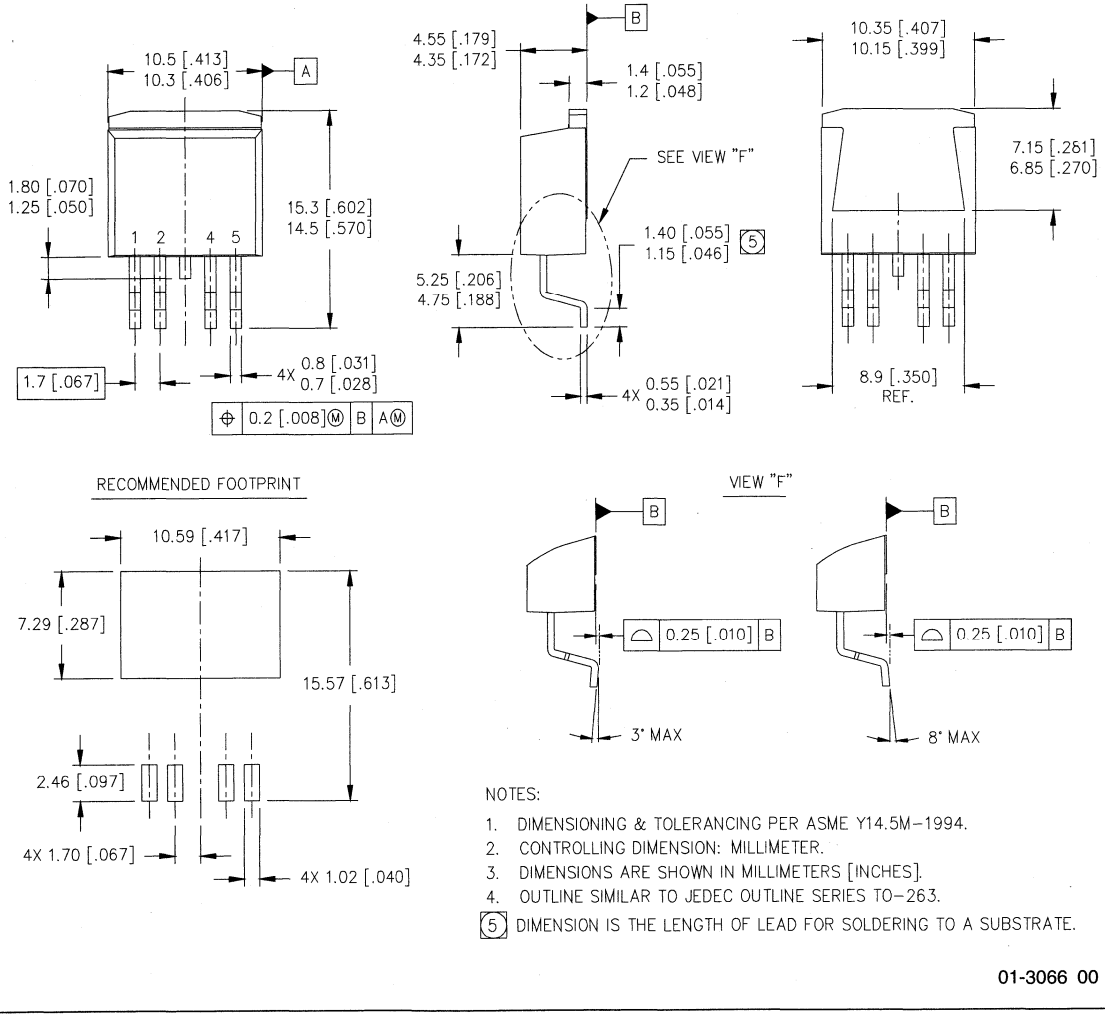
2. CONTROLLING DIMENSION: INCH.
3. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TS-001.

IRGB 01-3042 01

Case Outline - D²PAK (SMD220) - 5 Lead



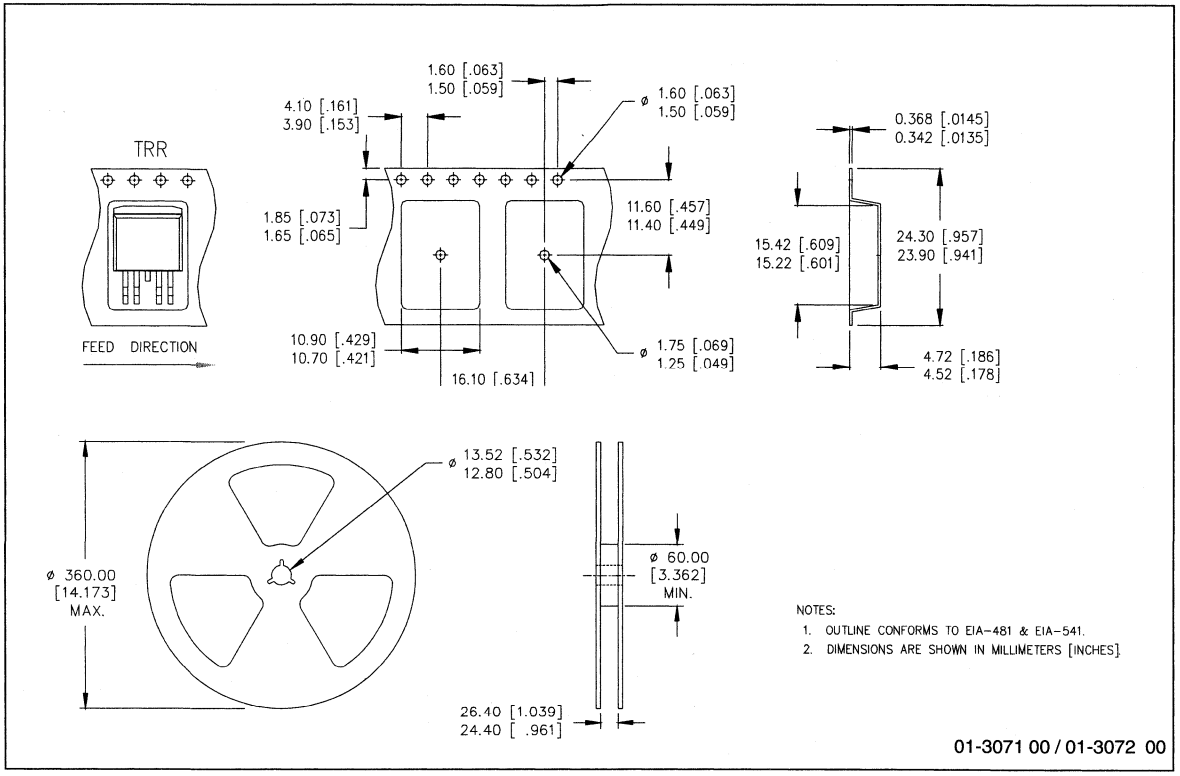
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE SIMILAR TO JEDEC OUTLINE SERIES TO–263.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-3066 00

Tape & Reel - SMD220 - 5 Lead



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IOR Rectifier

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IR2171

LINEAR CURRENT SENSING IC

Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low IQBS allows the boot strap power supply
- High Common Mode Noise Immunity
- Input overvoltage Protection for IGBT short circuit condition
- Open Drain output

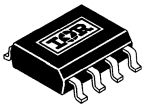
Product Summary

V_{OFFSET}	600V
I_{QBS}	1mA
V_{in}	+/-300mVmax
Gain temp. drift	50ppm/°C(typ.)
f_o	40kHz (typ.)

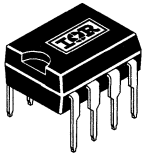
Descriptions

IR2171 is the linear current sensing IC designed for motor drive applications. It senses the motor phase current through an extenal shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM at 40kHz to eliminate need for the A/D input interface. It allows direct interface to uP via simple counter based measurement. The independently powered output enables easy interface to the opto coupler device for galvanic isolation if needed.

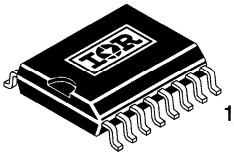
Packages



8 Lead SOIC

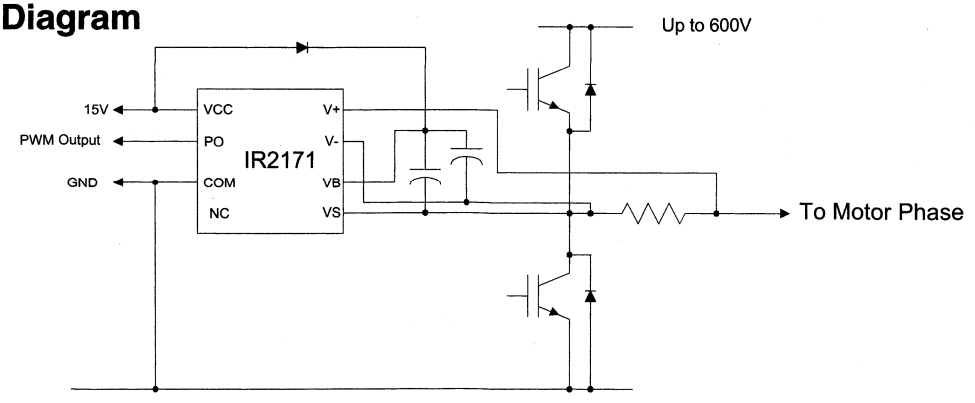


8 Lead PDIP



16 Lead SOIC
(wide body)

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		V_S -0.3	25	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{IN}	Maximum input voltage between V_{IN+} and V_{IN-}		-5	5	
V_{PO}	Digital PWM output voltage		COM -0.3	V_{CC} +0.3	
V_{IN-}	V_{IN-} input voltage (note 1)		Vs -5	V_B+0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
		16 lead SOIC	—	1.25	
$RthJ_A$	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
		16 lead SOIC	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: Capacitors are required between V_B and Vin-, and between V_B and Vs pins when bootstrap power is used. The external power supply, when used, is required between V_B and Vin-, and between V_B and Vs pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +13.0	V_S +20	V
V_S	High side floating supply offset voltage	note 2	600	
V_{PO}	Digital PWM output voltage	COM	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	9.5	20	
V_{IN}	Input voltage between V_{IN+} and V_{IN-}	-300	+300	mV
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operation for Vs of -5 to +600V. Logic state held for Vs of -5V to -V_{BS}.

DC Electrical Characteristics

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IN}	Nominal input voltage range before saturation $\|V_{IN+} - V_{IN-}\|$	-300	—	300	mV	
V_{OS}	Input offset voltage	-10	0	10		V_{IN} = 0V (note 2)
$\Delta V_{OS}/\Delta T_A$	Input offset voltage temperature drift	—	25	—	µV/°C	(note 1)
G	Gain (duty cycle % per V_{IN})	145	150	155	%/V	max gain error=5% (note 3)
$\Delta G/\Delta T_A$	Gain temperature drift	—	50	—	ppm/°C	(note 1)
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	1	2	mA	V_S = 0V
I_{QCC}	Quiescent V_{CC} supply current	—	—	1		
LIN	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
$\Delta_{LIN}/\Delta T_A$	Linearity temperature drift	—	.001	—	%/°C	(note 1)
I_{O-}	Output sink current	20	—	—	mA	V_O = 1V
		2	—	—		V_O = 0.1V

Note 1: Specification numbers are derived by design.
Note 2: ±10mV offset represents ±1.5% duty cycle fluctuation
Note 3: Gain = (full range of duty cycle in %) / (full input voltage range). Typically, gain = 90% / 600mV.

AC Electrical Characteristics

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
fo	Carrier frequency output	—	35	—	kHz	figure 1
$\Delta f/\Delta T_A$	Temperature drift of carrier frequency	—	300	—	ppm/°C	V_{IN} = 0V & 5V
Dmin	Minimum duty	—	5	—	%	V_{IN+}=-300mV,V_{IN-}=0
Dmax	Maximum duty	—	95	—	%	V_{IN+}=+300mV,V_{IN-}=0
BW	fo bandwidth		15		kHz	V_{IN+}=100mV pk-pk sine wave, -3dB
PHS	Phase shift at 1kHz		-10		°	V_{IN+}=100mVpkpk sine wave

Timing Waveforms

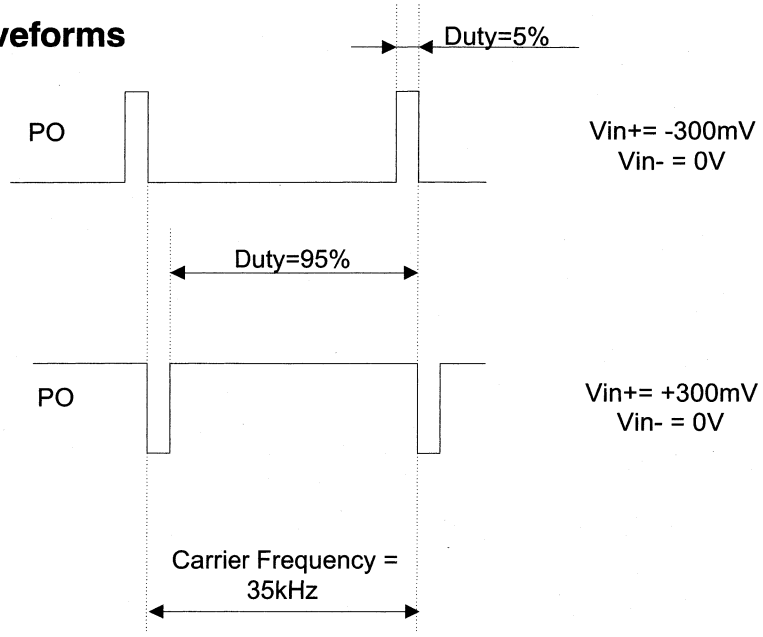


Figure 1 Output waveform

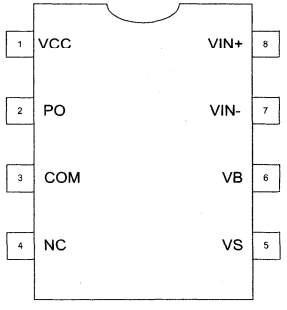
Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at a same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM periods gives consistent measurement of the current feedback over the temperature drift.

Lead Definitions

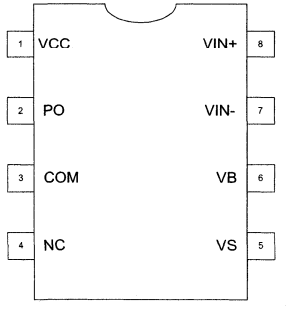
Symbol	Description
V_{CC}	Low side and logic supply voltage
COM	Low side logic ground
VIN+	Positive sense input
VIN-	Negative sense input
VB	High side supply
VS	High side return
PO	Digital PWM output
N.C.	No connection

Lead Assignment



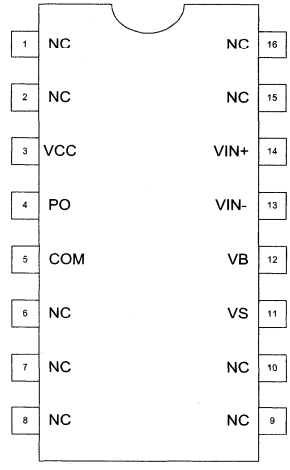
8 lead SOIC

IR2171S



8 lead PDIP

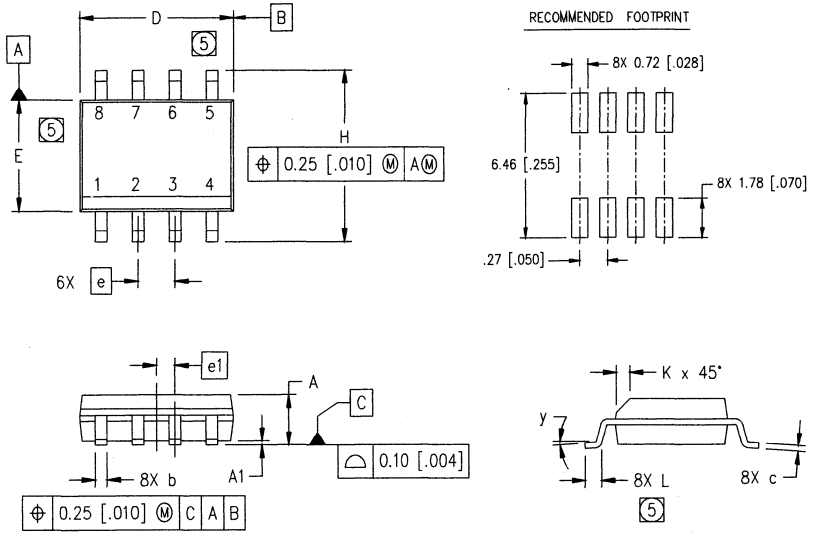
IR2171



16 lead SOIC

IR21716S

Case Outline

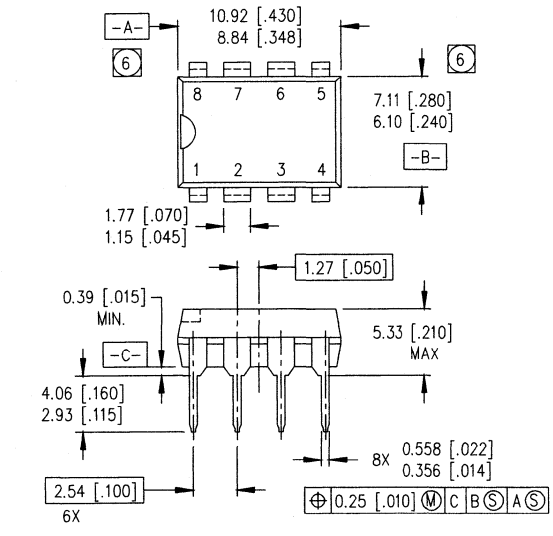


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

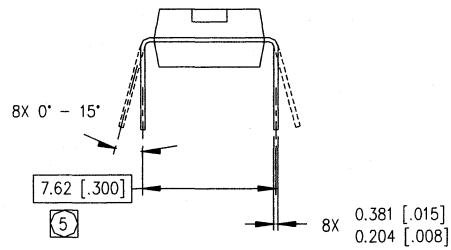
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

(MS-012AA) 01-0021 09

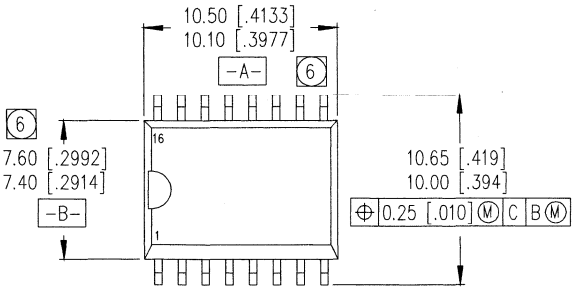


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-3003 01

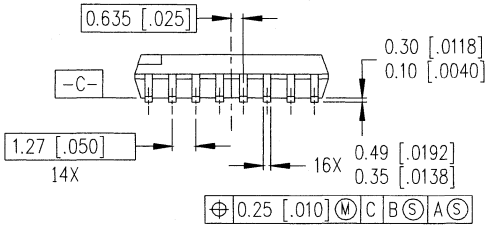


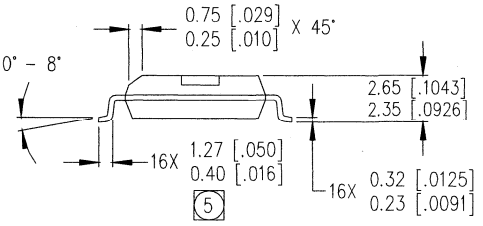
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–013AA.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].





16 Lead SOIC (wide body)

01-3014 03

IR2172

LINEAR CURRENT SENSING IC

Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low I_{QBS} allows the boot strap power supply
- Independent fast overcurrent trip signal
- High common mode noise immunity
- Input overvoltage protection for IGBT short circuit condition
- Open Drain outputs

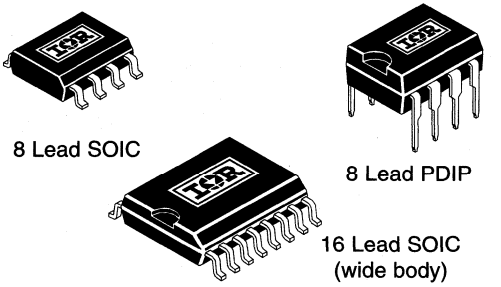
Description

IR2172 is the monolithic current sensing IC designed for motor drive applications. It senses the motor phase current through an extenal shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM to eliminate need for the A/D input interface. The dedicated overcurrent trip (OC) signal facilitates IGBT short circuit protection. The OC output pulse can be programmed by the external resistor and capacitor. The open-drain outputs make easy for any interface from 3.3V to 15V.

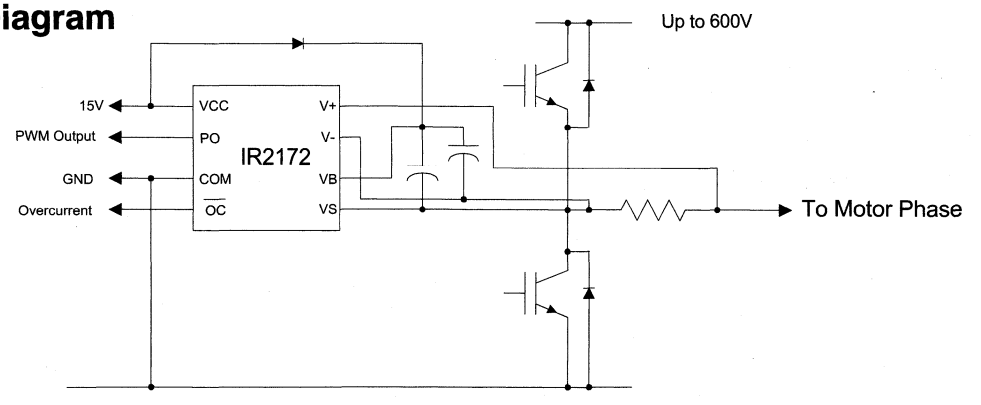
Product Summary

V_{OFFSET}	600Vmax
I_{QBS}	1mA
Vin	+/-300mVmax
Gain temp.drift	50ppm/°C (typ.)
f_o	40kHz (typ.)
Overcurrent trip signal delay	1.5usec (typ)
Overcurrent trip level	+/-300mV (typ.)

Packages



Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		-0.3	25	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{IN}	Maximum input voltage between V_{IN+} and V_{IN-}		-5	5	
V_{PO}	Digital PWM output voltage		COM -0.3	VCC +0.3	
V_{OC}	Overcurrent output voltage		COM -0.3	VCC +0.3	
V_{IN-}	V_{IN-} input voltage (note 1)		V_S -5	V_{B+} 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
		16 lead SOIC	—	1.25	
$RthJA$	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
		16 lead SOIC	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: Capacitors are required between V_B and Vin-, and between V_B and Vs pins when bootstrap power is used. The external power supply, when used, is required between Vs and Vin-, and between V_B and Vs pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +13.0	V_S +20	V
V_S	High side floating supply offset voltage	note 2	600	
V_{PO}	Digital PWM output voltage	COM	VCC	
V_{OC}	Overcurrent output voltage	COM	VCC	
V_{CC}	Low side and logic fixed supply voltage	9.5	20	
V_{IN}	Input voltage between V_{IN+} and V_{IN-}	-300	+300	mV
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operation for Vs of -5 to +600V. Logic state held for Vs of -5V to -V_{BS}.

DC Electrical Characteristics

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IN}	Nominal input voltage range before saturation $\|V_{IN+} - V_{IN-}\|$	-300	—	300	mV	
V_{OC+}	Overcurrent trip positive input voltage	288	300	312		
V_{OC-}	Overcurrent trip negative input voltage	-312	-300	-288		
V_{OS}	Input offset voltage	-10	0	10		V_{IN} = 0V (note 2)
$\Delta V_{OS}/\Delta T_A$	Input offset voltage temperature drift	—	25	—	µV/°C	(note 1)
G	Gain (duty cycle % per V_{IN})	145	150	155	%/V	max gain error=5% (note 3)
$\Delta G/\Delta T_A$	Gain temperature drift	—	50	—	ppm/°C	(note 1)
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	1	2	mA	V_S = 0V
I_{QCC}	Quiescent V_{CC} supply current	—	—	1		
LIN	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
$\Delta V_{LIN}/\Delta T_A$	Linearity temperature drift	—	.001	—	%/°C	(note 1)
I_{OPO}	Digital PWM output sink current	20	—	—	mA	V_O = 1V
		2	—	—		V_O = 0.1V
I_{OCC}	OC output sink current	10	—	—		V_O = 1V
		1	—	—		V_O = 0.1V

Note 1: Specification numbers are derived by design.
Note 2: ±10mV offset represents ±1.5% duty cycle fluctuation
Note 3: Gain = (full range of duty cycle in %) / (full input voltage range). Typically, gain = 90% / 600mV.

AC Electrical Characteristics

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
fo	Carrier frequency output	—	40	—	kHz	figure 1
$\Delta f/\Delta T_A$	Temperature drift of carrier frequency	—	1000	2000	ppm/°C	V_{IN} = 0 & 5V
Dmin	Minimum duty	—	5	—	%	V_{IN+}=-300mV,V_{IN-}=0V
Dmax	Maximum duty	—	95	—	%	V_{IN+}=+300mV,V_{IN-}=0V
BW	fo bandwidth		15		kHz	V_{IN+} = 100mVpk -pk sine wave, gain=-3dB
PHS	Phase shift at 1kHz		-10		°	V_{IN+} =100mVpk-pk sine wave

AC Electrical Characteristics cont.

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Proagation delay characteristics						
tdoc	Propagation delay time of OC	1	1.5	—	µsec	
twoc	Low true pulse width of OC	—	1	—		

Timing Waveforms

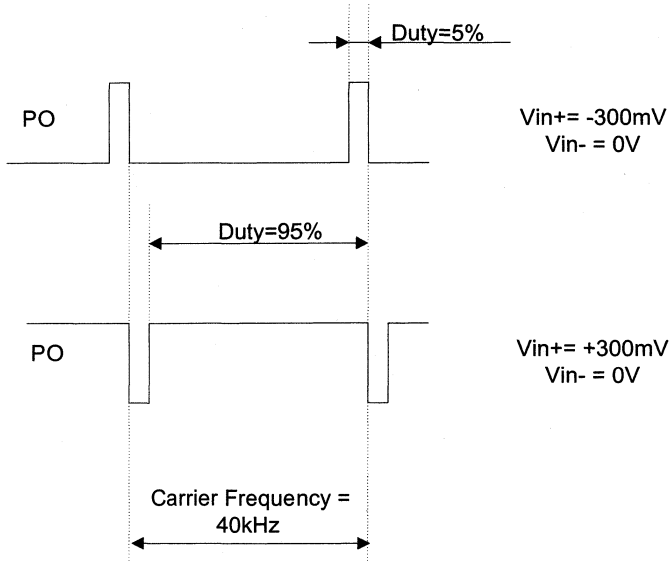


Figure 1 Output waveform

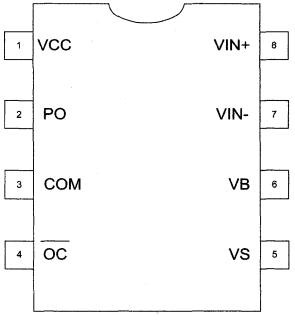
Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at the same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM period gives consistent measurement of the current feedback over the temperature drift.

Lead Definitions

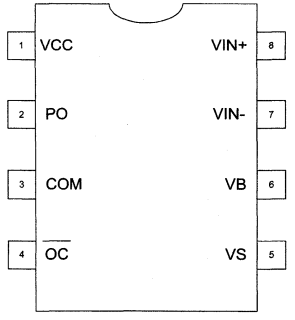
Symbol	Description
V_{CC}	Low side and logic supply voltage
COM	Low side logic ground
V_{IN+}	Positive sense input
V_{IN-}	Negative sense input
V_B	High side supply
V_S	High side return
PO	Digital PWM output
$\overline{OC}$	Overcurrent output (negative logic)
N.C.	No connection

Lead Assignment



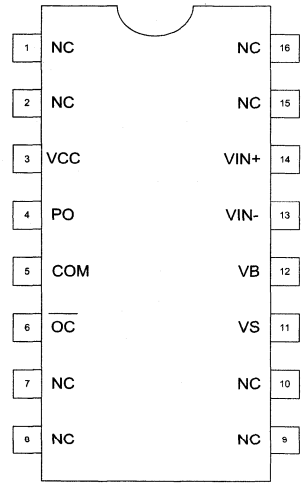
8 lead SOIC

IR2172S



8 lead PDIP

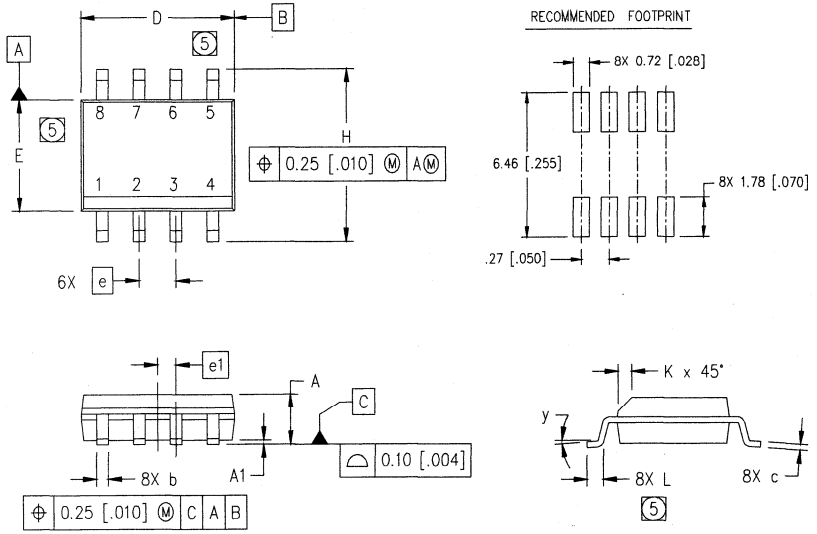
IR2172



16 lead SOIC

IR21726S

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

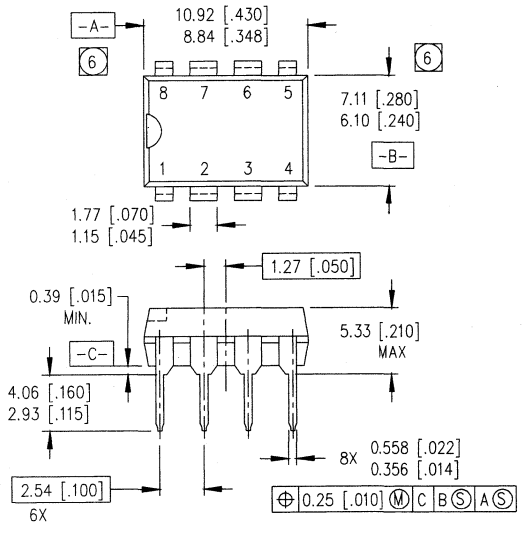
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

6 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 0

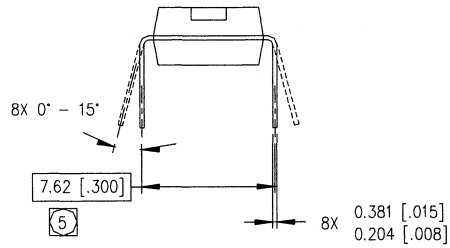


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.

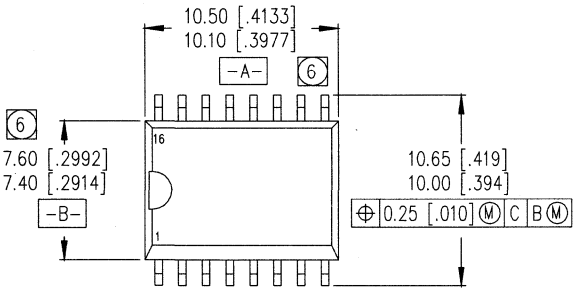
5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

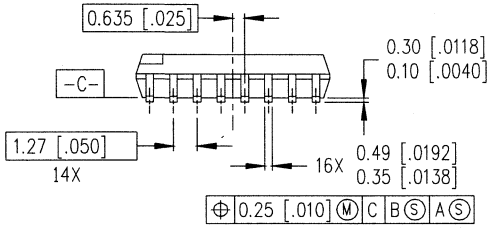
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-3003 01



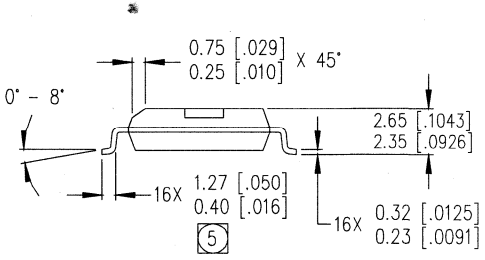


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



16 Lead SOIC (wide body)

01-3014 03

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IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
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APPLICATION NOTES

APPLICATION NOTES

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DESIGN TIP

DT 99-4

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Intelligent Power Switches (IPS): Basic Features & Protection

By X. de Frutos and A. Mathur

TOPICS COVERED

Choice of IPS for Different Loads
Current & Temperature protections
Active Clamp Mode
Protection Circuitry with Vcc referenced Input High Side IPS

Intelligent Power Switches (IPS) are IR's High Side and Low Side Protected Power MOSFETs. IPS devices are designed to safely handle ordinary overload conditions as well as several extraordinary conditions. In this Design Tip, we will look at some of the most important, though basic, protection features that IPSs offer. Initially, however, we will overview the main considerations for various loads, and how to choose an IPS based on these considerations.

1. CHOICE OF IPS FOR DIFFERENT LOADS

1-1 Filament bulbs

As shown in Fig. 1a, the inrush current from a filament bulb can exceed 10 times the rated current. Therefore IPSs with current limitation features are preferred. To decide on the current limitation value, Ilim, one needs to make a trade-off between the power dissipated (in the linear mode) and the protection level. As an initial approximation, a value of about 6 times the nominal current is commonly used for Ilim. However, it is important to ensure that the junction temperature does not exceed the protection temperature limit (Fig 1c). Perform tests to verify that the difference between the highest junction temperature and the protection limit (shown in Fig 1c as θ margin) is a safe value. If needed, a detailed temperature profile can be evaluated by simulation (using a bulb model).

1-2 Inductive loads

Inductive loads are efficiently protected by an IPS with either over-current (OI) shutdown or current limitation features. There are several points to bear in mind when designing around an inductive load. First, for electromechanical devices (electrovalves, relays, etc), the inrush peak current due to the inner air gap must not trigger the OI shutdown. Second, one should ensure that the current and temperature never exceed the protection limit for the worst condition. Third, the Active Clamp effect

(described in Section 3) also has to be accounted for. However, for a first order approximation, use the curve 'Max. Current-out vs Load Inductance' shown in the datasheets. (Fig. 10 in the IPS 511 datasheet is an example of such a graph).

1-3 Resistive Loads

Resistive loads are efficiently protected by an IPS with either an **over-current shutdown** or a **current limitation**. As a first order design approximation, refer to the datasheets for the table 'Recommended Operating Conditions' and for the graph 'Current-limit vs. Junction Temperature,' (e.g. Fig. 13 in the IPS511 datasheet). After this, one should evaluate the current and temperature for the worst operating conditions, to ensure that they are within the protection limits. Change the design accordingly.

2. OVER-CURRENT & OVER-TEMPERATURE PROTECTION

In many applications, extra protection circuits are required to satisfy the safety and reliability of the end system. The two most common (and lethal) problems are over-current and over-temperature. IR's IPS devices have been designed to protect against, among other things, these two basic maladies.

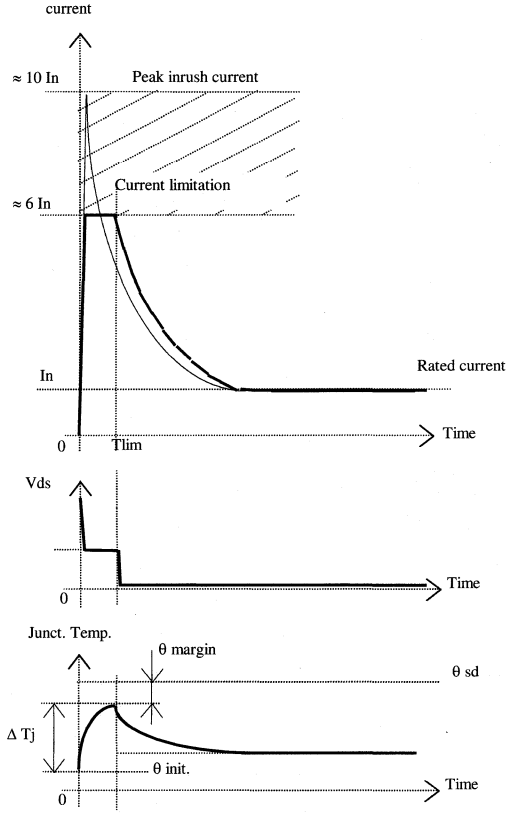
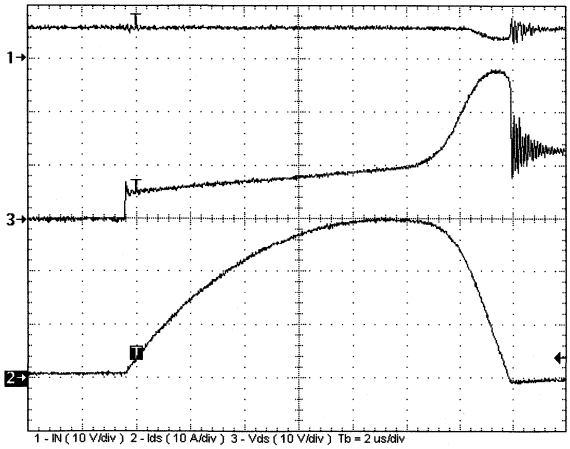


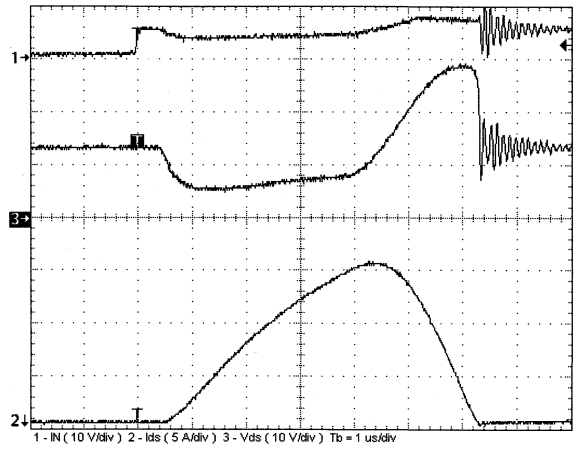
Figure 1: Filament Bulb Inrush Current.
(a) Current Profile (b) Vds Profile (c) Temperature Profile

2-1 Over-Current Shutdown (OI)

The basic premise of over-current shutdown is self-explanatory: when the current exceeds the Current Shut Down limit (Isd), the switch is turned-off (shut down). There are two possible modes for over-current. One is caused when the load short-circuits under constant input. Fig. 2a shows the waveforms associated with the shutdown for this case. The other mode of over-current is when the switch turns on with a short-circuit of load. See Fig. 2b for the shutdown for this type of over-current. The time taken to shut down can be evaluated from the 'Ids vs. Time' curve. For instance in Fig. 2a, Curve 2, the shutdown time (the time between the initial rise of current and subsequent return to normal) is about 14 micro-seconds, while in Fig. 2b, it is about 11 micro-seconds. (The current shutdown time is actually a function of the peak current, the inner delay, and the dI/dt slope.) Note that the Active Clamp is activated at the end of each short-circuit as evidenced by the rise in Vcc. To reset the IC, hold the input voltage low for the minimum reset time (Treset), as specified in the Protection Characteristics Table in the datasheet.



(a) Load short-circuit waveforms (Low Side IPS)
Esd = 3.3 mJ Vcc = 14 V

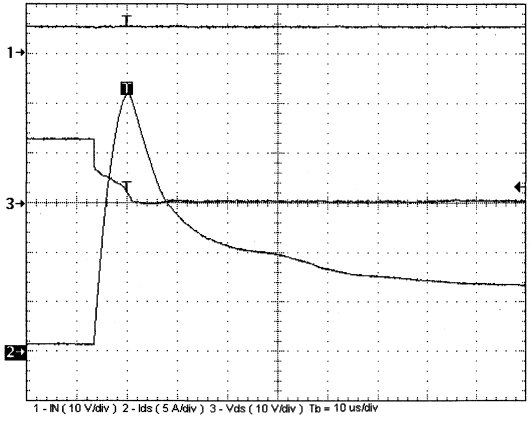


(b) Turn-on with a drain short-circuit (Low Side IPS)
Esd = 0.45 mJ Vcc = 14 V

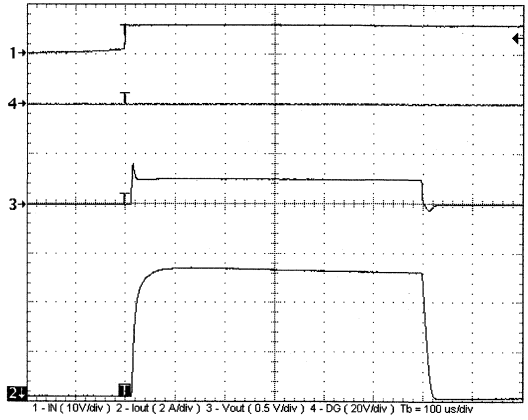
Figure 2: Over-current Shutdown

2-2 Current Limitation (Ilim)

In the current limitation protection type, the IC continuously checks the drain current. When the drain current reaches the Ilim value, an inner current loop drives the power MOSFET in a linear mode. However, this protection type reacts differently under the two possible modes of over-current. In the first case, where the load short-circuits during an on phase (Fig. 3a), there is a sharp current peak before the current limiting protection sets in. However, in the second case (when the switch turns on with the drain short-circuited), the limitation is a lot smoother. As can be seen in Fig 2b, there is no sharp spike in the current. Yet, the response time in both cases keeps the instantaneous current within the power MOSFET Safe Area. Current limitation is sustained until the over-temperature protection sets in (Section 2-3).



(a) Load short-circuit waveforms



(b) Turn-on with a drain short-circuit

Figure 3: Current Limitation Protection

2-3 Over-Temperature Protection

Over-temperature protection is the last line of defense against slow current increases, e.g. during ar over-load. As the name implies, when the junction temperature exceeds the shutdown temperature limit, Tsd (typically 165°C), the switch is turned off. Actually, this type of protection causes the switch to latch off. To reset the IPS, hold the input voltage low for a minimum reset time, Treset (given in the 'Protection Characteristics' table of the datasheet). When the device has an automatic restart (with hysteresis), it latches on after the junction temperature falls down to its restart value (typically 158°C)

Precautions when Designing for Over-temperature protection:

- OT shutdown is a protection. Do not use it as a functional threshold (whether as a thermal oscillator or otherwise). If used as a threshold, the junction temperature would permanently stay at about160°C, and significantly (and adversely) affect the IPS's lifetime.

- The Active Clamp (Section 3) overrides the temperature protection. There is no way to interrupt the current in active clamp or reverse bias mode (body diode).

- In certain circumstances (e.g. switching into a hard short-circuit at high frequencies), a thermal runaway could occur. See the Design Tip on High Frequency Operation (DT99-5, Section 3).

2-4 Important Considerations when Designing for Over-Current and Over-Temperature Protectior

The 'Ids vs. Protection Response Time' curve (I-vs-T curve) provides an overview of the protectior features of the IPSs. (Figure 14 in the IPS021 datasheet is an example). The representative I-vs-T curve in Fig. 4 shows the region where over-current protection dominates, as well as the region where over-temperature protection takes over.

When designing the current path around the load, there are two key points to bear in mind. First, the path's current capability should always be *higher* than the curve shown, such that the current path does not burn out before the over-current protection kicks in. Second, the load's current capability should always be *lower* than the curve shown, such that one avoids false triggering of over-current protection.

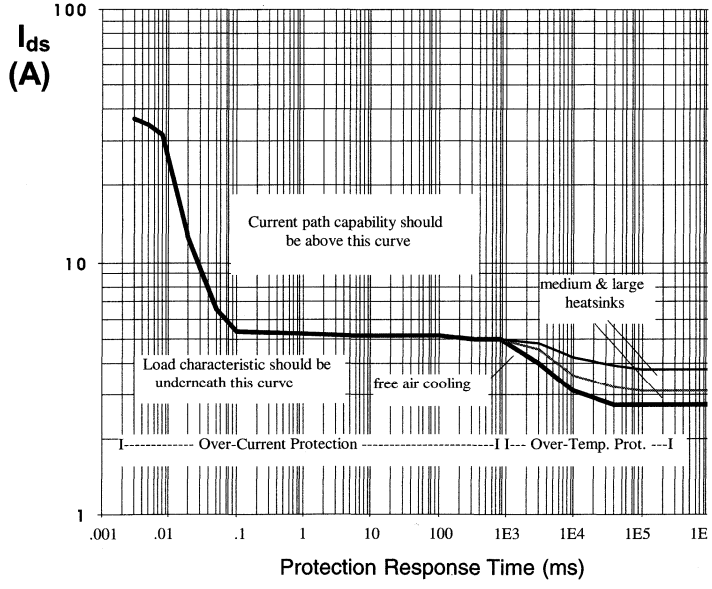


Figure 4: Protection Characteristic of IPS

3. ACTIVE CLAMP MODE

3-1 Purpose of Active Clamping

Turning off an inductive load requires additional consideration in the energy dissipation capabilities. Essentially the stored energy (½.L.I²) will have to be dissipated by the power MOSFET. This dissipation is not dependent on the Rds(on), but rather on the energy rating of the die and the scheme of the inductive turn-off clamp. The re-circulation time for the load to be de-energized with the load current going to zero is a function of Vclamp. A higher value of Vclamp will be able to de-energize faster. Compared to conventional methods of dissipating this energy quickly (such as free-wheel diodes, Zener clamps, and MOSFET avalanches), active clamping provides the most efficient means to dissipate the energy stored in the inductor. Consequently, the active clamping feature is integrated into all IPS devices.

3-2 Active Clamping Methodology

The active clamp feature is shown in Figure 5. During the off-state, the power MOSFET is turned back on when Vds > Vzener +Vf,diode + Vthreshold,MOSFET. Also, there are two large resistances, the resistor and the MOSFET, within this current path to help dissipate energy. (Note that during the active clamp the FET is in a linear, or high-resistance, mode.) The load demagnetizes quickly during active clamp because the stored energy in the load is dissipated across a large potential [Vcc - Vclamp]. The larger the difference, the faster the demagnetization.

The energy dissipated by the IPS during the Active Clamp sequence is Vclamp x ∫Ids(t)dt. The energy stored by the inductance is [Vclamp - Vcc] x ∫Ids(t) dt. Thus, it is important to notice that during the active clamp sequence, the device dissipates more power than the load. (The current through the load and the IPS is the same but the voltage across the IPS is higher than the one across the load).
The total energy dissipated by the IPS can be calculated using the formula:
E_{IPS} = (½.L.I²). (Vclamp / (Vclamp - Vcc))

The maximum inductive load allowed for each IPS can be estimated from the graph 'Iclamp vs Inductive Load', given in the datasheets (e.g. Figure 15 in the IPS021L datasheet).

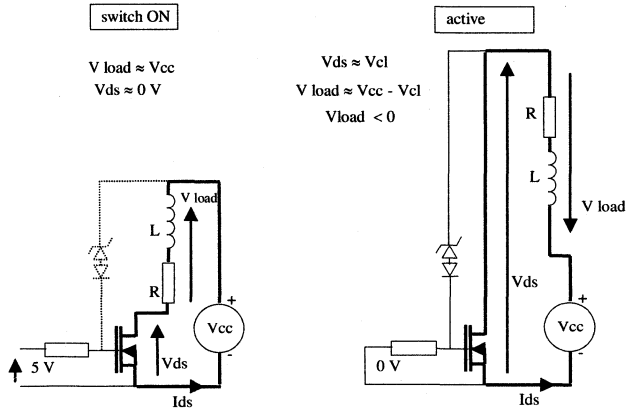
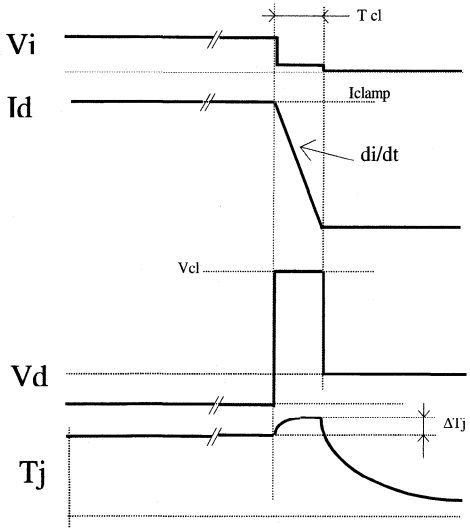


Figure 5: Active Clamp Circuitry

3-3 Thermal Issues During the Active Clamp Mode

Junction temperature of the MOSFET rises during active clamp because the FET operates in the linear mode. When needed, ΔTj can be evaluated as follows:



di/dt of the Demag. current : di/dt = [Vcc - Vcl] / L

Clamping Time : Tcl = Iclamp / | di/dt |
Clamping average current : Icl avg = Iclamp / 2

Power dissip. during clamping : Pcl = Vcl . Icl avg

Junction Temperature rise : DTj = Pcl . Rth (for Tcl)

Notes:
Load inductance in (H)
Voltages in (V) and Current in (A)
Rth (for Tcl) is the corresponding transient thermal impedance for Tcl
(See 'Transient Thermal Imped. Vs Time' curve in the datasheet)

3-4 Active Clamping for High and Low side IPSs

The above discussion (and Figure 5) used a low-side switch architecture as the example. High side IPS devices work similarly. As the high-side switch is internally referenced to the Vcc pin, its drain goes below grounded during clamping. Figure 6a and 6b show Active Clamp waveforms for both low and high side switches.

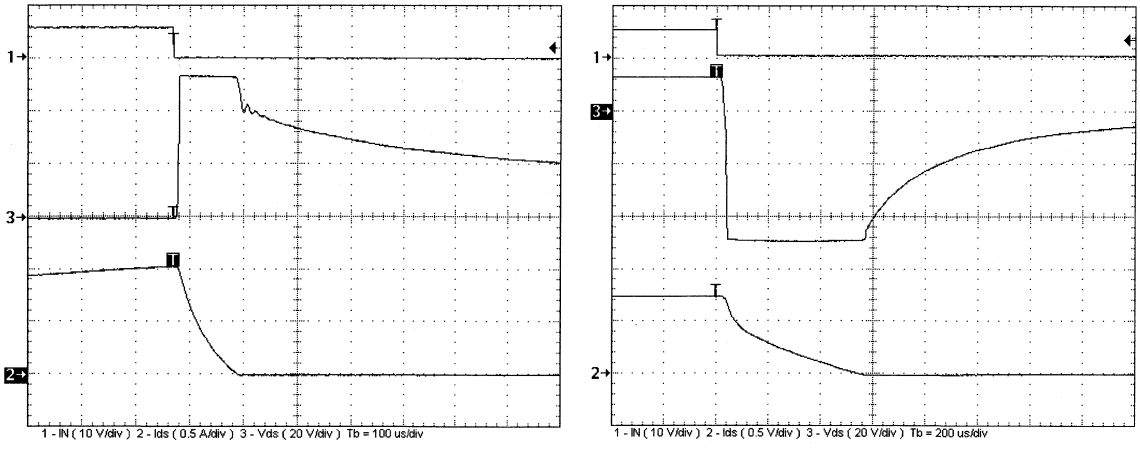


Figure 6: Clamping Waveforms. (a) Low Side Switch (b) High Side Switch

For low side switches, the return path of the clamp includes the input pin. Sink current can be limited by adding a resistor in series with IN pin. IPS products are able to turn the load back on if the input is cycled while clamping.

4. PROTECTION CIRCUITRY WITH Vcc REFERENCED INPUT HIGH SIDE IPS

A Vcc referenced Input high side IPS is different from a regular high side IPS in that its input pin is referenced to the Vcc pin. Vcc referenced Input high side IPSs are usually used in the automotive environment, and therefore require the additional protective circuitry shown in Figure 7, whose components consist of:

(a) A shottky diode (low current rated), to avoid a negative voltage at the microprocessor output under a reverse battery condition.
(b) A zener diode, to protect the input against voltage peaks, and
(c) A resistor, Rin, to limit the diode current. The maximum value of this resistor can be calculated as:

$$Rin < \frac{Vcc\ min - Vih - Vf - Vce}{Iin\ on}$$

where
Vcc min = minimum operating Vcc voltage (V)
Vih = high level input threshold voltage (V)
Iin on = typical current for the input pin (A)
(Vcc-Vin = Vih)
Vf = diode forward voltage drop (V)
Vce = open collector voltage (V)
Rin = input resistor (W)

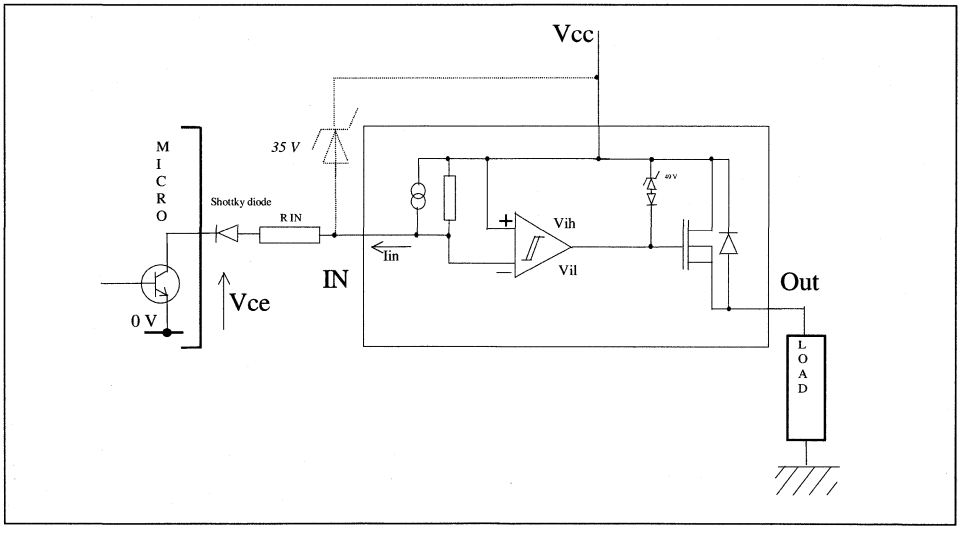


Figure 6: Clamping Waveforms. (a) Low Side Switch (b) High Side Switch

In a Vcc referenced Input high side IPS, a high current flows through the Vcc pin. Any parasitic resistance in series with this pin will significantly modify input threshold because the voltage drop across the parasitic resistor acts as a voltage feedback to the input. One must, therefore, make an effort in board layout, to minimize such parasitic resistance.

5. CONCLUSION

This Design Tip is meant to explain only the basic features and protections offered by IPS devices. For further information on the Switching and Diagnostic capabilities of these devices, refer to Design Tip 99-5. Design Tip 99-6 offers an in-depth understanding of IPS operations in an automotive environment.

International
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DESIGN TIP

DT 99-5

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

Intelligent Power Switch (IPS) Switching & Diagnostic Capabilities

By X. de Frutos and A. Mathur

TOPICS COVERED

Diagnostic Capabilities
Switching Characteristics
High Frequency Operation

Intelligent Power Switches (IPSs) are fully protected switches. This Design Tip explains both the diagnostic features offered by these products, as well as their switching behavior.

1. DIAGNOSTIC CAPABILITIES

In this section, we will look at how IPSs diagnostic features indicate over-temperature, over-current, and over-load conditions.

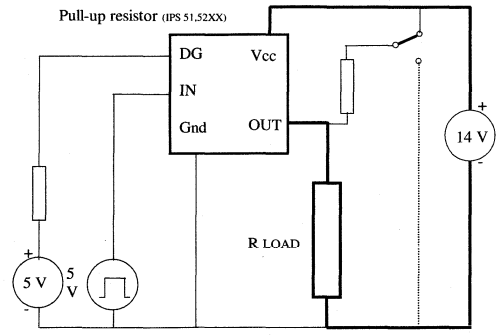
1-1 High Side IPS Diagnostic Capabilities

Most high side IPSs offer a dedicated diagnostic output pin (DG), which diagnoses the following conditions:

- An over-current condition (OI) occurs when the IPS is either in current limiting or in current shutdown mode. This condition causes the DG signal to react as shown in Table 1.
- An over-temperature condition (OT) is diagnosed by the IPS51, IPS52, and IPS54XX series as shown in Table 1. As indicated in Table 1, devices with an inbuilt hysteretic-temperature-protection feature cycles the DG output under an OT condition.
- An open-load condition (OL) is detected by all High Side IPS devices. There are two methods of detecting an OL condition. First, as in the IPS54XX series, the DG output is based on the current level of the load. For these devices, however, the DG output cannot distinguish

between OI, OT and OL conditions. Second, as in the IPS51XX and IPS52XX series, open-load is detected by sensing the load voltage. To do so, the IPS51XX and IPS52XX series need an additional Vcc pull-up resistor on the output. If the switch is OFF when DG flags a fault, OL has occurred. If the switch is ON, it is either an OI or an OT condition.

Note, however, that a fault when the IPS is OFF indicates either an OL or else a short to Vcc. To differentiate between these last two, switch the pull-up resistor to ground. An open-load will cause the DG pin to stop indicating a fault, while a short to Vcc would continue to show a fault.



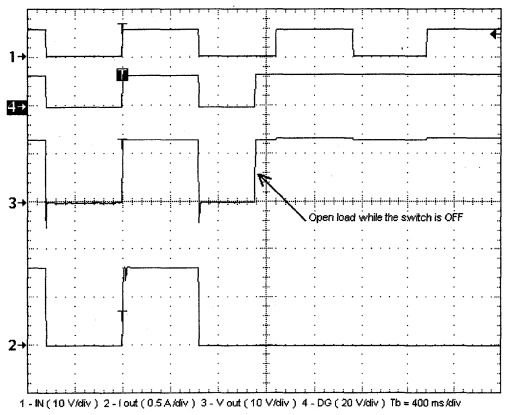
I open load = current threshold considered for open load detection (A)
Vsih = open load detection voltage (typ. 3 V)
R pull-up = (Vcc - Vsih) / I open load

Figure 1: Diagnostic Circuit

Condition	IN	OUT51,52XX	OUT54XX	DG 51,52XX	DG54XX
Normal	H	H	H	H	H
Normal	L	L	L	L	H
Open load	H	H	X	H	L
Open load	L	H	X	H	H
Short-circuit	H	I Limit.	L (latched)	L	L
Short-circuit	L	L	L	L	H
Over-temperature	H	L (cycling)	L (cycling)	L	L (cycling)
Over-temperature	L	L	L	L	H

Table 1: Truth Table for Diagnosis of Problem

Figures 2a & 2b show the open load timing diagrams for IPS51XX, IPS52XX and IPS 54XX parts.



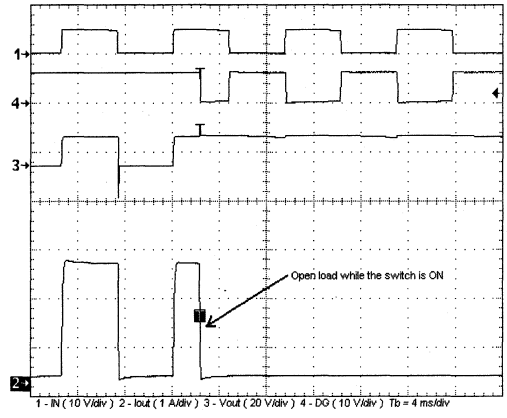


Fig. 2: Open Load Timing Diagrams (a) IPS 51,52XX (b) IPS 54XX

Note that, for the IPS 54XX, turning on with large inductive loads will delay the DG signal because of the time needed for the current to reach the open load threshold.

1-2 Low Side IPS Diagnostic Capabilities

A status signal can be added to low side switches by adding the circuitry shown in Figure 3, which generates a logic signal corresponding to over-temp and over-current shutdowns. The RC delay should be adjusted in order to mask fault indication during a positive going edge at IN. Over-current and over-temperature are detected only during an ON state.

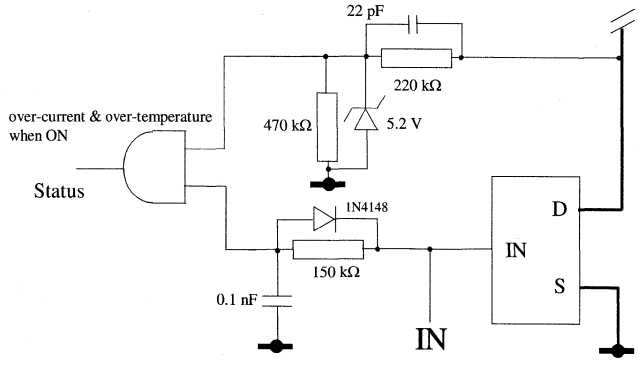


Figure 3: Low Side IPS Status Schematic.
(Component values should be adjusted to switching time.)

2. SWITCHING CHARACTERISTICS

Each of the 3 different types of IPS devices has a different reference, which, in turn, affects their switching characteristics. Low-side IPSs and regular (or grounded) high-side IPSs are usually driven with 5 V logic signals.

Low-Side IPS:
The triggers on the low side IPS inputs are referenced to the source. To guarantee a proper switching waveform, a maximum of a 1 ms rise time is required for the input signal. As shown in Figures 4a and 4b, one can control the switching characteristics, i.e. the dI/dt curve, by adding a resistor in series with the input. This resistor should not exceed 10 kΩ.

Regular High-Side IPS:
Regular high-side IPSs have a hysteretic input, and therefore an input resistor in series has no effect on switching. Figure 4c & 4d show typical switching waveforms.

Vcc referenced Input High-Side IPS:
Vcc referenced Input high-side IPSs have a hysteretic input referenced to the Vcc pin. Again, an input resistor in series has no effect on switching.

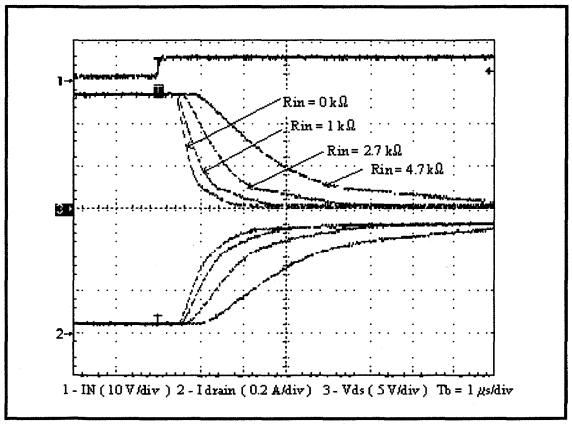


Figure 4a - IN resistor effect on turn-on

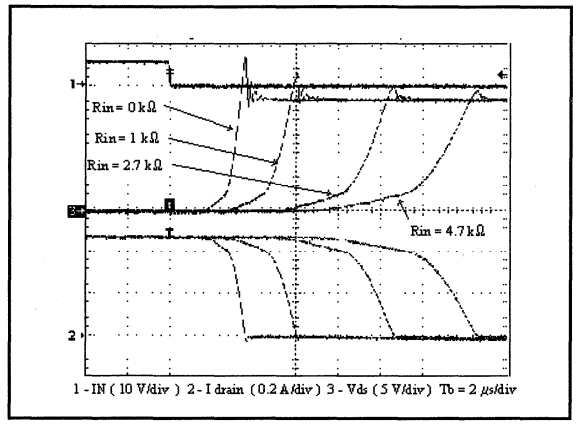


Figure 4b - IN resistor effect on Turn-off

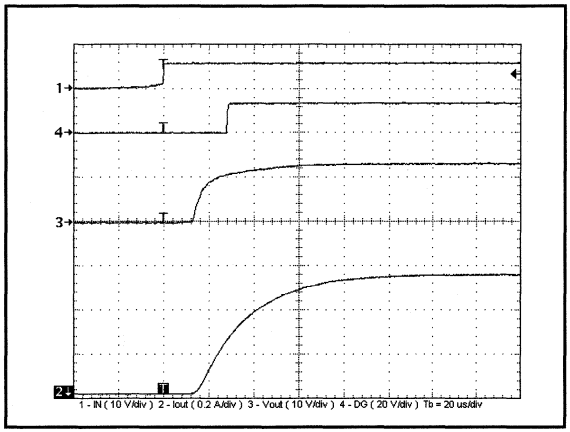


Figure 4c - High side switch turn-on waveforms

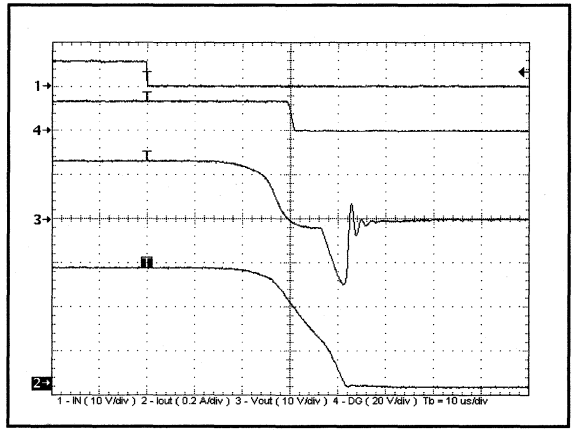


Figure 4d - High side switch turn-off waveforms

Figure 4: Turn-on and Turn-off Waveforms

IPSs protect against electrostatic discharge on the functional pins (IN and DG), by using a zener diode between ground and the pin concerned. This zener can also be used as a voltage clamp so long as its current doesn't exceed 5 mA.

3. HIGH FREQUENCY OPERATION

The switching frequency of an IPS device is limited by a possible thermal run-away condition. During a short-circuit at high frequencies, for instance, the PWM generator will reset the device at each cycle, and will thereby cause over-heating. To avoid over-heating, the maximum allowable frequency for a free running PWM generator can be estimated using the formula:

$$Fmax.\ (Hz) < [150 - Tamb.] / [Rth' \cdot Esc]$$

where :

Tamb = maximum ambiant temperature (°C) ;
Rth' = total junction / air thermal resistance (including heatsink effect) (°C/W)
Esc = short-circuit energy (J).

Low Side IPSs are able to operate at higher frequencies if the PWM generator features an overall protection loop (as shown in Figure 5), in which the protection loop stops the pulses as soon as a missing cycle is detected on the load. With its efficient short-circuit protection, thermal runaway is avoided, and therefore a far higher operating frequency can be chosen. Also, a microprocessor can easily integrate this protection function using either the DG output or the Low Side IPS status schematic (in Fig 3), in conjunction with the protection loop in Figure 5. The component values in Figure 5 must be adapted according to the operating frequency.

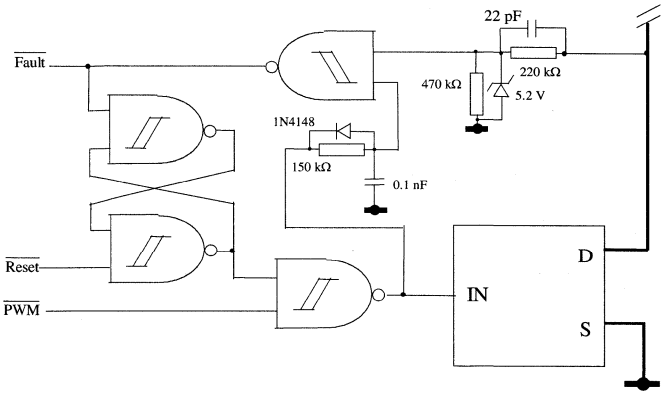
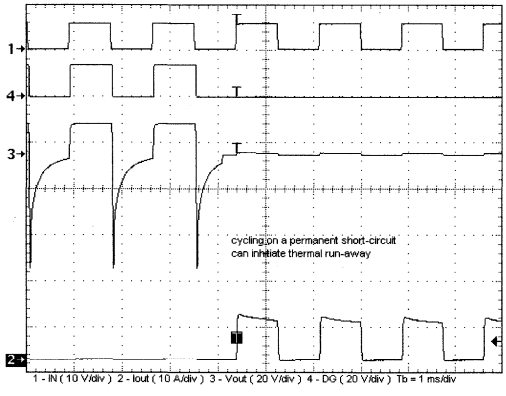
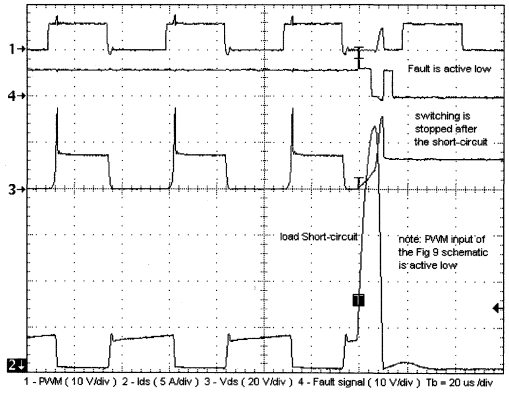


Figure 5: Status Schematic Including Protection Loop

Figures 6a and 6b show the switching waveforms and the protection loop effect.



(a) High Side



(b) Low Side with Protection Loop

Figure 6: Switching Waveforms.

4. CONCLUSION

This Design Tip explains the Switching and Diagnostic capabilities of the IPS devices. For information on the basic protective features offered by these devices, refer to Design Tip 99-4. Design Tip 99-6 offers an in-depth understanding of IPS operations in an automotive environment.

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DESIGN TIP

DT 99-6

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

Intelligent Power Switches (IPS): Operation in an Automotive Environment

By X. de Frutos and A. Mathur

TOPICS COVERED

Ground loss
Ground offset
Voltage peaks
Reverse battery conditions
Battery disconnection
Load dump capability

Intelligent Power Switches (IPSs) are particularly appreciated in the automotive environment, where they have to deal with some of the worst electrical conditions - including ground loss or offset, voltage peaks, reverse or disconnected battery, and load dump. IPSs protect against all these conditions, while driving loads ranging from power relays and electrovalves to motors and lamps. Low side, high side and groundless high side switches use different internal structures to do so, and their behaviour varies for various electrical stresses. (Automotive electrical stresses refer to the ISO 7637 definitions).

1. GROUND LOSS

1-1 Low Side IPSs

When the ground is disconnected on a low side switch, the load is no longer activated. Figure 1 shows the parasitic structure that is activated in this case. A resistor in series, Rin, limits the current that would flow into the microcontroller. The resistor has to be a low enough value (about 1kΩ) such that the voltage drop across it is negligible, thus assuring proper operation under normal conditions.

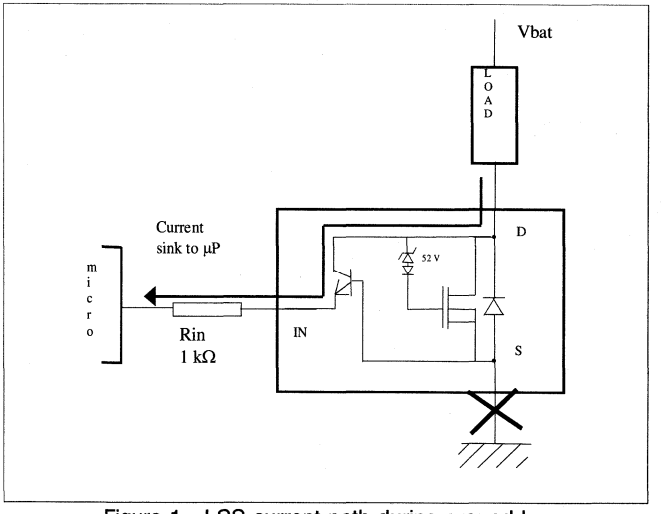

Figure 1 - LSS current path during ground loss

1-2 High Side IPSs

High side switch logic control is referenced to Vcc. When the ground is disconnected, the IN pin is pulled-up to Vcc. The Power MOSFET turns-off and the load is no longer activated. Resistors in series (about 15kΩ each) limit current re-injection through DG and IN to about 1 mA. Figure 2 shows the current path during ground loss.

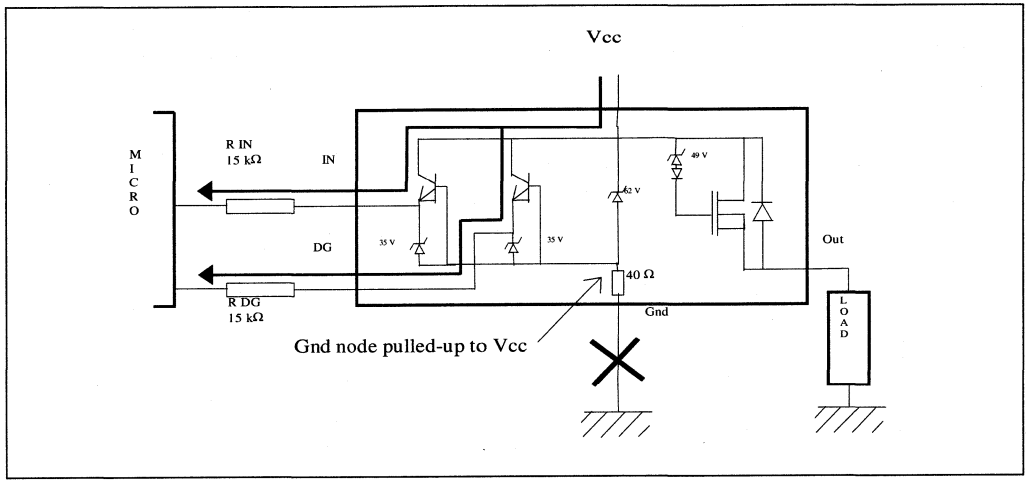

Figure 2 - HSS current path during ground loss

1-3 Vcc referenced Input High Side IPSs

A Vcc referenced Input high side switch is not connected to a ground in normal use. Therefore, a loss of ground connection is irrelevant.

2. GROUND OFFSET

The floating gate drive of the high side switches allows positive and negative voltages between load ground and logic ground. The ground offset is defined as the common mode of the output voltage referenced to the logic ground (see Figure 3). The IPS remains under active control as long as the load ground is (a) less than Vcc, and (b) greater than (Vcc-Vcl).

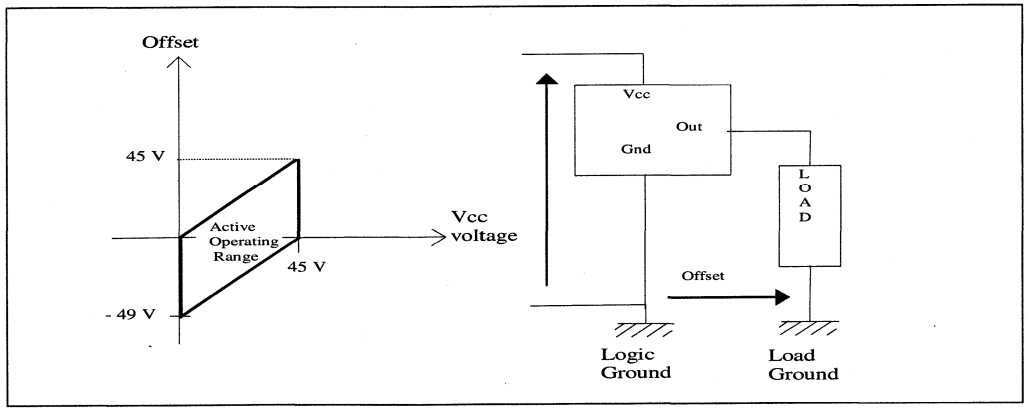

Figure 3 - HSS ground offset definition

3. VOLTAGE PEAKS

The profile of a voltage pulse on Vcc or Vbat is typically defined by the rise time, duration and source resistance. For example, in a typical case of the IR European version, positive pulses have the following characteristics: Vp = 100 V, tr = 1 ms, Td = 50 ms, Ri = 10Ω; while negative pulses have a shorter duration: Vp = 100 V, tr = 1 ms, Td = 2 ms, Ri = 10Ω.

Both types of pulses represent inductive effects: the positive pulse is generated when the current through an inductance in series with the device is turned-off; the negative one is generated when the current through an inductive load in parallel with the device is switched-off.

3-1 Low Side IPS

Positive Pulse
For low side switches, when the Vcc voltage exceeds Vclamp, the difference between Vpulse and Vclamp activates the load, and therefore prevents current re-injection into the microprocessor.

Negative Pulse
Negative pulses also activate the load by turning on the body-diode. A reverse bias protection scheme helps to avoid current re-injection to the microprocessor (Fig 4b).

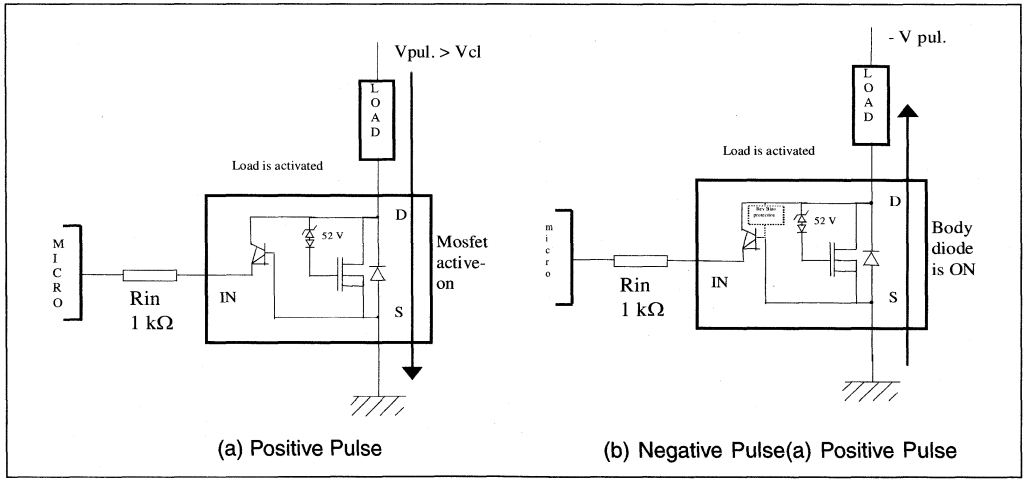

Figure 4 - LSS current paths during pulses

3-2 High Side IPS

Under either a positive or negative pulse on Vcc, one may need to add the zener diodes (shown in Fig 5) to supplement the limited power dissipation capability of the internal structure of a high side IPS device.

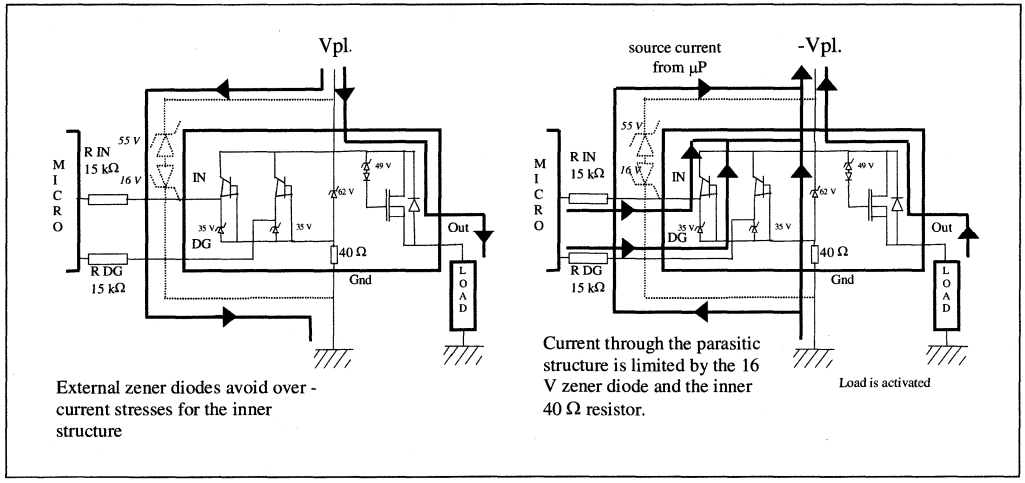

Figure 5 - High Side IPS current paths during pulses

3-3 Vcc referenced Input High Side IPS

For Vcc refeenced Input high side switches, such as the IPS 5551T, an additional zener diode must be added between Vcc and IN, as shown in Figure 6, to limit the current to and from the microprocessor In either a positive or negative pulse, the load is activated.

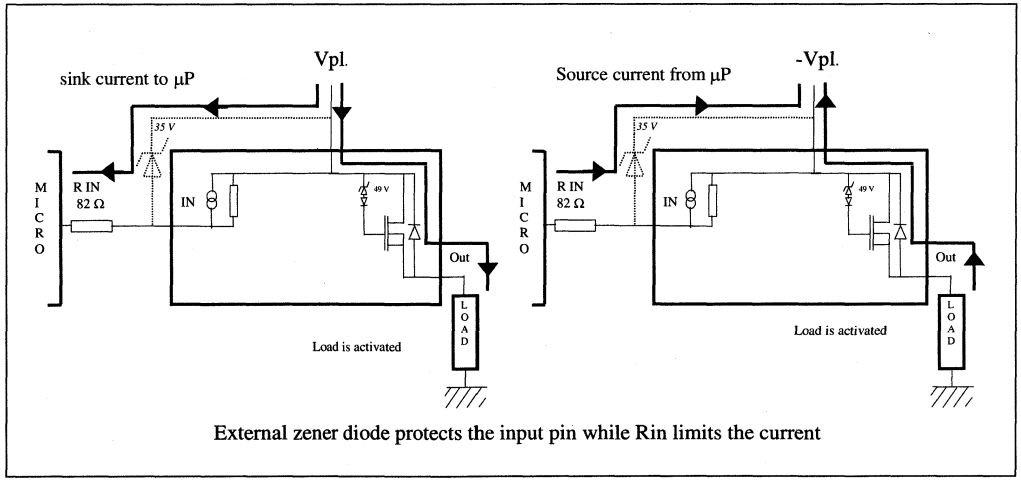

Figure 6 - External zener diode protects the input pin while Rin limits the current

4. REVERSE BATTERY CONDITION

4-1 Low Side IPSs

When a reverse battery condition occurs, current flows through the forward biased body diode (as shown in Figure 7), and activates the load. In this case the junction temperature should be evaluated, since this condition can, in several seconds, heat the junction to a high temperature due to diode dissipation.

An inbuilt reverse bias protection prevents this current from being re-injected into the microcontroller.

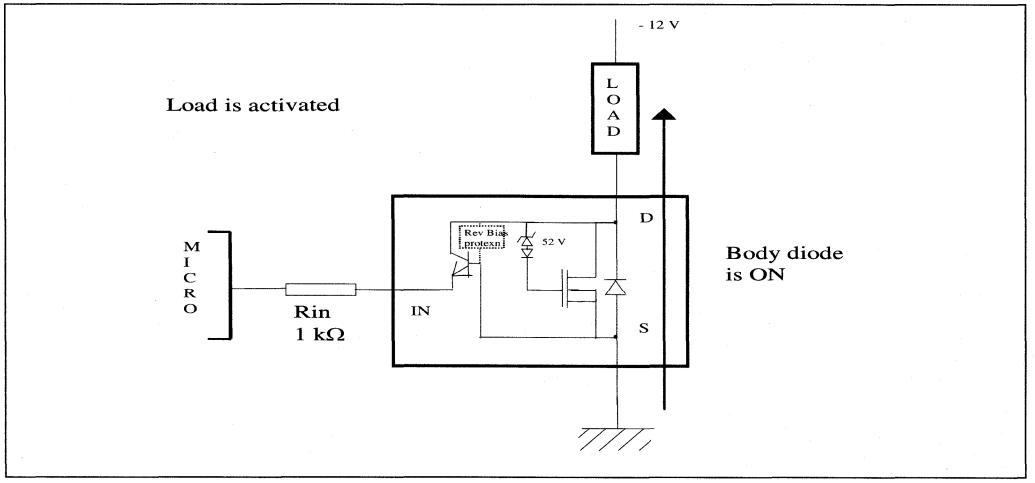

Figure 7 - LSS current path during reverse battery

4-2 High Side IPSs

A schottky diode in series with the ground return is used to prevent negative bias (Figure 8). The load is activated through the body diode, and therefore, the junction temperature rise (due to diode dissipation) has to be evaluated. If the load cannot be activated, a power schottky diode should be inserted in the positive Vcc line. (An IPS with a low Rds(on) can be used instead of the schottky to reduce the voltage drop.)

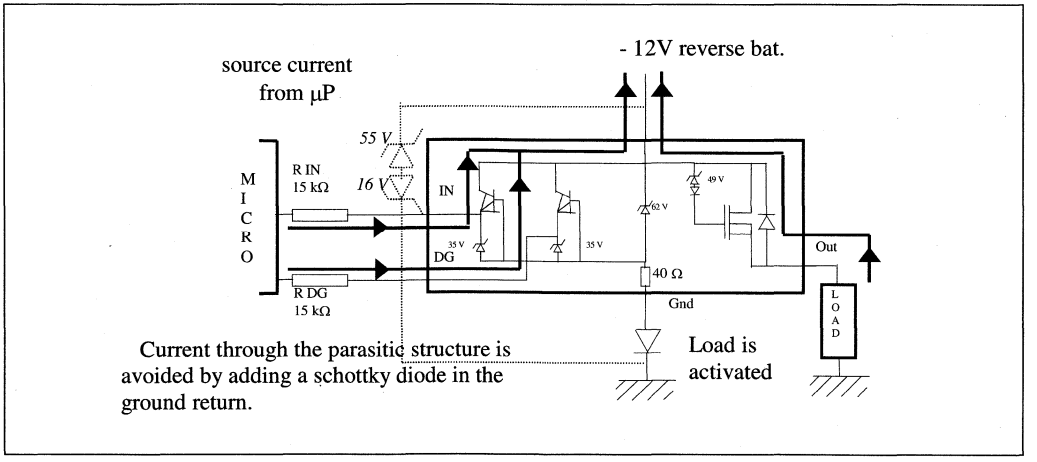

Figure 8 - HSS current path for -14V reverse battery

4-3 Vcc referenced Input High Side IPSs

A schottky diode in series with the input is used to prevent negative bias (Figure 9). (A low current shottky diode is suitable). Again, the load is activated through the body diode.

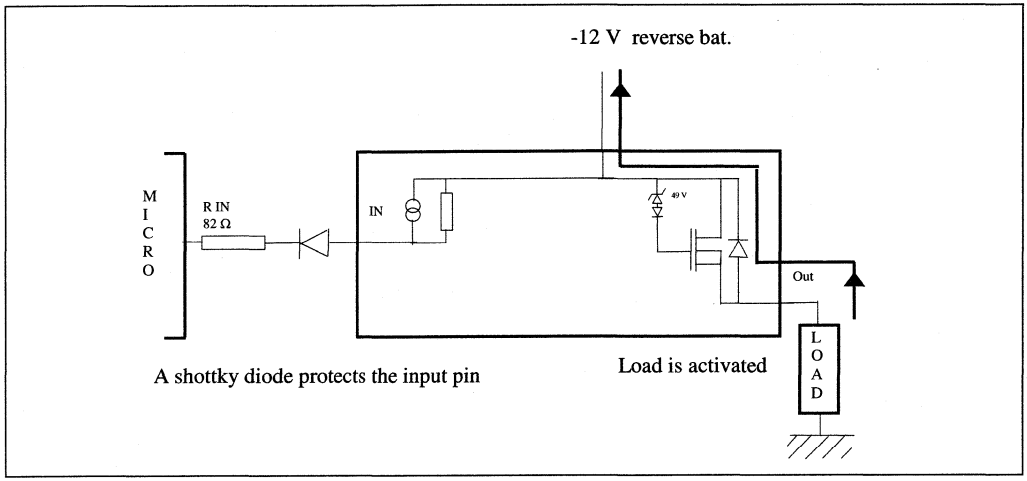

Figure 9 - Groundless HSS current path for -14V reverse battery

5. BATTERY DISCONNECTION

If the supply is disconnected while an inductive load is energised, the current must find an alternate path. However, since the low side and Vcc referenced Input high side switches cannot offer any demagnetisation path, a disconnected battery condition leads to a situation similar to the 'reverse battery condition'.

For a high side IPS, however, the load current will attempt to flow through the internal diode and the 40Ω resistor. To protect this resistor (which can only withstand 0.4 A), it is necessary to add an alternate current path that uses a zener (DZ1) and a diode (D2) in series as shown in Figure 10.

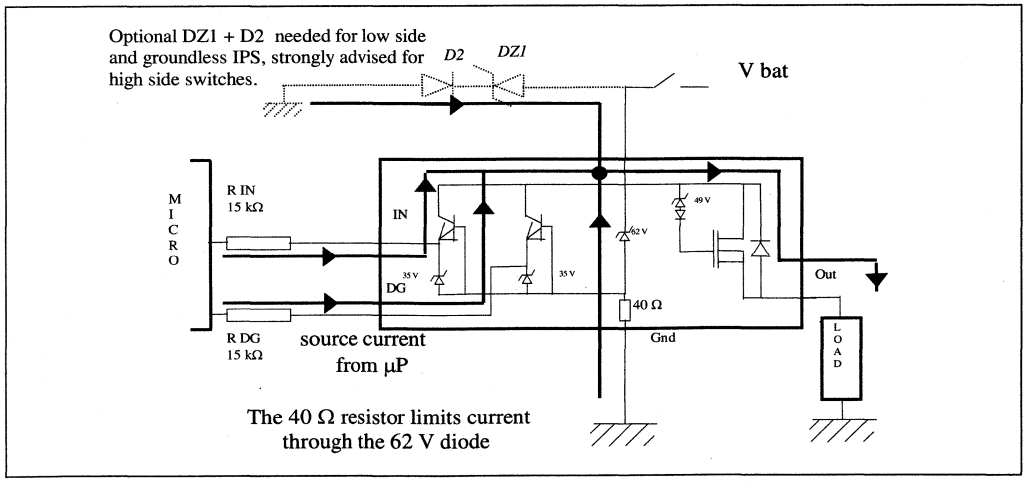

Figure 10 - HSS current path with battery disconnection

6. LOAD DUMP CAPABILITY

A load dump occurs when the battery is disconnected while the alternator is at full flux. Its profile on Vcc is defined by its maximum peak voltage, its rise time, its duration and its source resistance. For example, for our European versions, typical load dump values are: Vp = 37 V, Tr = 10 mS, Ton = 200 ms and Ri = 2Ω.

As a general rule, IPSs should have a Vcl rating above the load dump voltage (to prevent current re-injection to the micro). The load dump overvoltage remains below Vcl so nothing happens when the switch is OFF. When ON, however, power dissipation increases (Rdson x I^2 load dump) and the rise in junction temperature, ΔTj, has to be evaluated.

If the system requires the load to operate during load dump, the drain current has to remain below Isd.

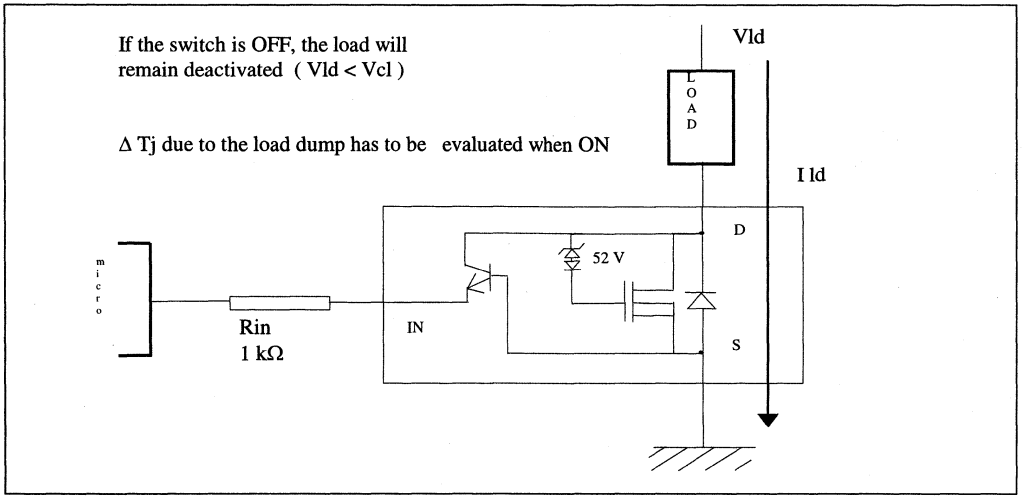

Figure 11 - LSS current path during load dump

7. CONCLUSION

This Design Tip offers an in-depth understanding of IPS operations in an automotive environment. For information on the basic protective features offered by these devices, refer to Design Tip 99-4. Design Tip 99-5 describes the Switching and Diagnostic capabilities of the IPS devices.

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DESIGN TIP

DT 99-8

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Using IR2171/IR2172 within DSP-controlled AC Drives

By Dorin O. Neacsu

TOPICS COVERED

Description of the control system including the linear current sensing ICs
Using Texas Instruments TMS320C240 DSP
Hardware description
Software description
Open-loop results

1. DESCRIPTION OF THE CONTROL SYSTEM INCLUDING THE LINEAR CURRENT SENSING ICs

Many applications require a three-phase AC drive ranging from hundreds of W to few MW. All of these cases are based on a three-phase inverter controlled by a microcontroller or DSP system. Measurement of at least two phase currents is desired in more advanced systems that are employing Field-Orientation Control of induction or synchronous machines.

There are several methods generally used for measurement of inverter currents:

- shunt resistors on the phase currents followed by linear optocouplers;
- Hall effect current sensors used on the phase currents;
- shunt resistors on the DC link current followed by an OpAmp and extensive reconstruction hardware/software.

IR2171/IR2172 are a promising alternative to these methods and they are based on sensing the phase currents through an external shunt resistor and transfer of the signal to the low side after converting it from analog to digital. The level shift function is realized using IR's high-voltage isolation technology. The output signal is a carrier pulse-width modulated wave with *fc* around 40kHz that can interface to a microcontroller system directly or through a galvanical separation. The duty ratio varies according to the shunt resistor voltage up to ±260mV.

This new approach has inherent advantages over the previous solutions in reduced cost and size as well as the possiblity of using the microcontroller system on the same ground level as the power system (especially in low power applications). Design note introduces the IR2171/IR2172 by explaining their use

as current measurement system within a micro-controlled AC drive. The *Texas Instruments TMS320F(C)240* has been chosen as an example due to its simple interface. Both system interface and software are explained and performance is analyzed based on some results that are finally detailed.

The PWM signal is applied to a counter input and the pulse widths are transformed in digital code by counting at the microcontroller clock frequency. The temperature drift of the output carrier voltage can be cancelled by measuring both intervals corresponding to the low and high level. A software routine is expected to calculate the duty ratio and to transform this data into an equivalent current value.

2. Using TMS320C(F)240 DSP

Texas Instruments TMS320C(F)240DSP is a good performing computing engine with rich peripherals designed for AC motor drive applications. The Field-Orientation control structure based on this DSP contains

- the Event Manager for the generation of the Space Vector PWM signals;
- 2 capture channels for the encoder.

The other two channels of the capture unit are herein used to the phase current measurement.

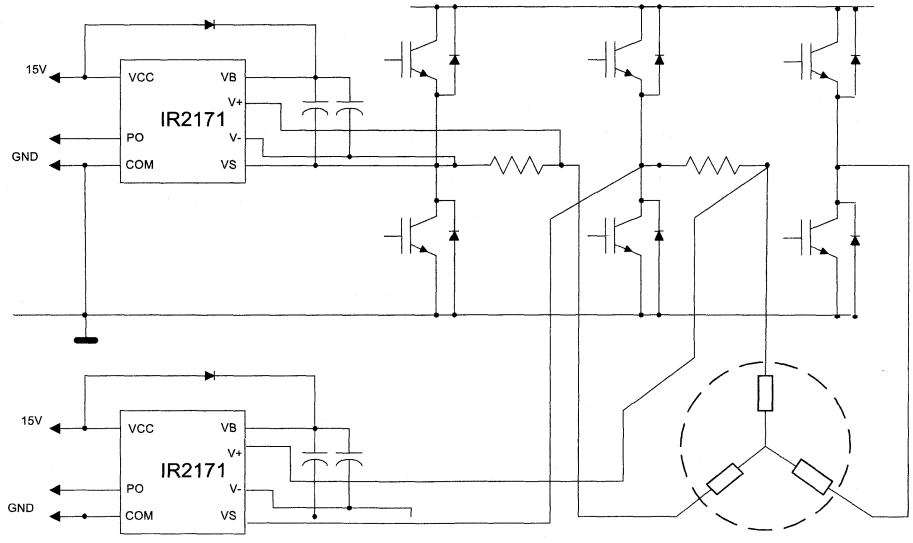

Figure 1 - IR2171 current measurement in a three-phase inverter drive

In this respect, a timer is selected to count at the CPU clock frequency of 20 or 30MHz and the counter content is saved into a stack at transitions on the capture input pins. The latency from a transition happens on an input pin and the moment the counter value is locked is 3.5-4.5 CPU clock cycles.

Since it is likely to measure both active and inactive state intervals, the timer content should be saved at both rising and falling edges. Unfortunately, the DSP system does not allow to separate the capture event from the interrupt generation event. In other words, we cannot capture both transitions

and ask the capture unit to generate an interrupt for reading data at each second transition. When employing interrupts on both edges, there is not enough time to serve those interrupts and to perform the main Field-Orientation control program. There would be 2 interrupts at each *1/fc* for each current measurement, each interrupt service routine lasting for at least 2μs. The DSP utilization factor would therefore be seriously affected.

Another possible problem is related to the minimum pulse width that is basically 2 μs, but can reach its minimum of τmin=1.87μs due to technological dispersion.

The delay between the interrupt request and its service is composed of:

- the synchronization time it takes for the interrupt to be recognized by the peripheral interface and converted into a request to the DSP. It takes:
  - **2 clock cycles** for internal interrupts
  - **4 clock cycles** for external interrupts.
- the CPU response time to recognize and acknowledge the enabled interrupt request. The minimum latency is **4 clock cycles** and longer for multicycle operations (memory access using wait states, repeat loops, pipeline operation, or serving other interrupt before the interrupts are unmasked again).
- the time needed by ISR to branch to get the specific event that produced the interrupt. possible case leads to minimum **4 clock cycles**.
- the time needed by the software routine designed to serve the interrupt to save the status registers, accumulator and sometimes other registers before doing the expected stack readings, savings of data to memory and other calculations. Minimum time expected for this interrupt routine initialization is **6 clock cycles**.

The overall time necessary to save the capture unit data to memory is very close to the value of the minimum pulse width of the input PWM signal.

Noticing these allows us to propose a solution based on having only one interrupt for each period (around 40kHz) at each falling edge of the capture input signal. During the appropriate interrupt servicing routine, the last two values of the capture stack are read and minor calculations are employed to defining the pulse widths. Such interrupt can be requested by a separate input of the DSP and acting as an external interrupt. The interrupt latency is about the same in this approach when compared to the solution of having two interrupts at each sampling interval, interrupts caused by the capture unit itself. However, the DSP utilization factor is improved allowing further development such as Field-Oriented Control or sensorless control.

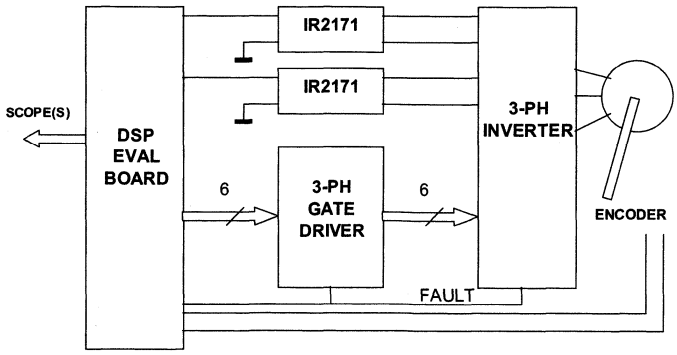

Figure 2 - Block diagram of the control system

3. Hardware description

The interface of the two IR2171 devices with the DSP is shown in Fig.2. The TMS320C24x DSP controllers evaluation module has been used for testing the current acquisition. *Table I* provides some information about the interface with IR2171, but the power supply, clock and usual circuitry is not included.

Name of the signal		DSP TMS320C240 pin	Eval.board connector
PWM outputs to be connected to the inverter gate drivers	PWM1/CMP1	94	P1-pin3
	PWM2/CMP2	95	P1-pin4
	PWM3/CMP3	96	P1-pin5
	PWM4/CMP4	97	P1-pin6
	PWM5/CMP5	98	P1-pin7
	PWM6/CMP6	99	P1-pin8
Fault signal	PDPINT	52	P1-pin26
Encoder signals	CAP1/QEP1	67	P1-pin21
	CAP2/QEP2	68	P1-pin22
2171-ph.A	CAP3/QEP3	69	P1-pin23
2171-ph.B	CAP4/QEP4	70	P1-pin24
2171-ph.A	XINT2	54	P4-pin19
2171-ph.B	XINT3	55	P4-pin20
Scope-ch.1	DACOUT0	-	P2-pin25
Scope-ch.2	DACOUT1	-	P2-pin26
Scope-ch.3	DACOUT2	-	P2-pin27
Scope-ch.4	DACOUT3	-	P2-pin28

Table I

4. Software description

This section describes the software routines that could be included in any control software for a 3-phase motor drive in order to make use of the IR2171 for current measurements.

This solution is not unique and it is presented herein as a test example. Moreover, only those parts of code that refer to the capture unit configuration and current calculations are included herein.

```
;********* initialization of variables ----------------------
.....
;******** Vector address declarations  **********************************
              .sect   ".vectors"
RSVECT        B       START   ; PM 0    Reset Vector          1 ;00
INT1          B       CRT_ISR  ; PM 2    Int level 1           4 ;02
INT2          B       PWM_ISR  ; PM 4    Int level 2           5 ;04
INT3          B       PHANTOM  ; PM 6    Int level 3           6 ;06
.....
       .text
```

```
;********* M A I N    C O D E   - starts here    ************************
START: ……..
;*********   SYSTEM CONFIGURATION          *********************************
…..
              LDP    #04h          ;
              MAR    *,1           ;
              LAR    AR0,#initar   ;
……..
;********* CONFIGURE EVENT MANAGER   ------------------
; Configure I/O pins as capture units ------------------
              LDP    #0E1h         ;
              SPLK   #0FF00H,OPCRA ;
              SPLK   #00F0H,OPCRB  ;
;********* INITIALIZE EVENT MANAGER   ------------------
              ……..
;------ Configure CAPCON and enable capture operation --------
              SPLK #1001101000001111b,CAPCON     ;
;------ External digital inputs used for interrupting at current measurement
              LDP    #0E0h                ;
              SPLK #1000000000000001b,XINT2_CNTL;
              SPLK #1000000000000001b,XINT3_CNTL;
……..
;********* Main background loop   ************************************
MAIN          LDP    #04h          ;
              NOP                  ;
              NOP
              B      MAIN          ;
;********* Routine Name: P W M _ I S R   ************************
PWM_ISR:      CLRC   INTM          ;
              SST    #0,stk1              ; save ST0 - Forced Page 0
              SST    #1,stk2              ; save ST1 - Forced Page 0
              LDP    #00h          ;
              SACL   stk3   ; save ACCL
              SACH   stk4   ; save ACCH
              LDP    #0E8h         ;
              SPLK   #0FFFFh,IFRA  ; Clear all Group A interrupt flags
;******** Phase Current calculation - Phase A = IaDelta2/[IaDelta1+IaDelta2]
              LDP    #04h          ;
              LACC   IaDelta2      ;
              ADD    IaDelta1      ;
              SACL   GPR2          ;
              ZALR   IaDelta2      ;
              RPT    #15           ; Place 16-bit pos. divisor in data memo
              SUBC   GPR2          ; Execute SUBC for 16 times
                                   ; L-ACC=quotient and H-ACC=remainder
              SACL   Ia            ; Save 'Ia' in D0 format (norm.)
;******** Phase Current calculation - Phase B = IbDelta1/[IbDelta1+IbDelta2]
              LACC   IbDelta2      ;
              ADD    IbDelta1      ;
              SACL   GPR2          ;
              ZALR   IbDelta2      ;
              RPT    #15           ; Place 16-bit pos. divisor in data memo
              SUBC   GPR2          ; Execute SUBC for 16 times
                                   ; L-ACC=quotient and H-ACC=remainder
              SACL   Ib            ; Save 'Ib' in D0 format (norm.)
……..
```

```
;******** configure DAC for scope **********************************
                LDP     #04h            ; Set data page pointer to 0000h
                LACC    Ia,12           ;
                SACH    DAC0_VAL        ; Load Ta to channel 1 of DAC
                LACC    Ib,12           ;
                SACH    DAC1_VAL        ; Load Tb to channel 2 of DAC
                LACL    IaTime1         ;
                SACL    DAC2_VAL        ; Load Tc to channel 3 of DAC
                LACL    IaTime2         ;
                SACL    DAC3_VAL        ; Load Tc to channel 3 of DAC
                OUT     DAC0_VAL,0000h      ; Write to the DAC0 register
                OUT     DAC1_VAL,0001h      ; Write to the DAC1 register
                OUT     DAC2_VAL,0002h      ; Write to the DAC2 register
                OUT     DAC3_VAL,0003h      ; Write to the DAC3 register
                OUT     DAC3_VAL,0004h      ; Start DAC conversions by writing DAC
update reg.
;********* Restore regs  ----------------------
                LDP     #00h            ;
                ZALH    stk4            ; restore ACCH
                ADDS    stk3            ; restore ACCL
                LST     #1, stk2        ; restore ST1
                LST     #0, stk1        ; restore ST0
                RET                     ;
;********* Routine Name: C R T _ I S R   ************************
CRT_ISR         SST     #0,*-           ;
                SST     #1,*-           ;
                LDP     #0E0h           ;
                BIT     SYSIVR,13       ;
                BCND    Ib_ISR,TC       ; If TC=1, run XINT3_S_ISR (Ib)
Ia_ISR          LDP     #0E8h           ; Set data page pointer to 7400h
                LAR     AR6,FIFO3       ; Read the old stack data to AR6
                LAR     AR7,FIFO3       ; Read the newer stack data to AR7
                SACL    *-              ;
                SACH    *-              ;
                CLRC    INTM            ;
                LDP     #04h            ;
                SAR     AR6,IaTime1     ; Save first reading to 'IaTime1'
                LACC    IaTime1         ;
                SUB     IaTime2         ;
                SACL    IaDelta1        ; Calculate the 'off' time.
                SAR     AR7,IaTime2     ; Save second reading to 'IaTime2'
                LACC    IaTime2         ;
                SUB     IaTime1         ; Calculate the 'on' time
                SACL    IaDelta2        ;
                B       SAVEREG         ;
Ib_ISR          LDP     #0E8h           ; Set data page pointer to 7400h
                LAR     AR4,FIFO4       ; Read the old stack data to AR6
                LAR     AR5,FIFO4       ; Read the newer stack data to AR7
                SACL    *-              ;
                SACH    *-              ;
                CLRC    INTM            ;
                LDP     #04h            ;
                SAR     AR4,IbTime1     ; Save first reading to 'IbTime1'
                LACC    IbTime1         ;
                SUB     IbTime2         ;
                SACL    IbDelta1        ; Calculate the 'off' time
                SAR     AR5,IbTime2     ; Save second reading to 'IbTime2'
                LACC    IbTime2         ;
                SUB     IbTime1         ;
                SACL    IbDelta2        ; Calculate the 'on' time
```

```
SAVEREG     SETC   INTM        ;
            MAR    *+,AR0      ;
            LACC   *+,16       ;
            ADDS   *+          ;
            LST    #1,*+       ;
            LST    #0,*        ;
            CLRC   INTM        ;
            RET                ;
```

5. Results

Several tests have been made in order to validate both hardware and software. In the beginning, open-loop tests have been carried out by applying pure sinusoidal input signals to the IR2171/2172 development board. Most of the waveforms are obtained by reconstruction through 12-bit D/A converters. The data is sent to this converter when currents are calculated by DSP from input data during the interrupt routine for inverter switching PWM generation that occurs at each 4kHz. Effects of sampling could be noticed in most waveforms. However, they are inherent in a digital system and provide information about the real data used by the control loop. The worst case shows a delay of 38μs that corresponds to 13.68° for 1kHz input signal. This delay is measured from the original sinusoidal signal to the left-end point of each S/H level and it contains not only IR2171 phase delay (about 10° phase shift) but also delay due to DSP internal S/H.

5-A Waveforms (Fif. 3)

Trace 3 (up) = input signal
Trace 4 (mid)=2171 to DSP signal (40kHz)
Trace 2 (dwn)= signal reconstructed through the D/A conv.

5-B Phase delays (Fig. 4)

Trace 3 = input signal
Trace A = DSP signal

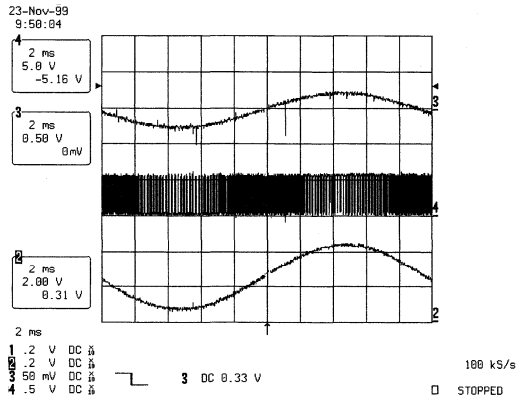

Figure 3a
Input signal: freq.=50Hz, amplitude of 240mV

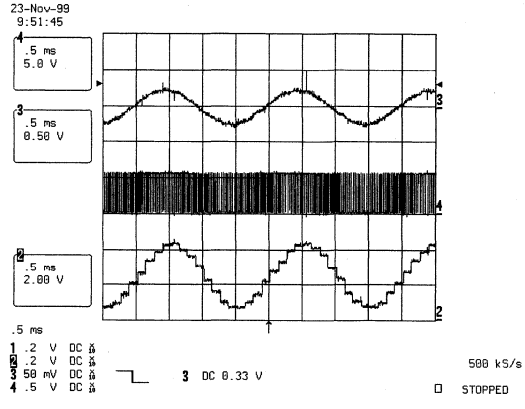

Figure 3b
Input signal: freq.=500Hz, amplitude of 240mV

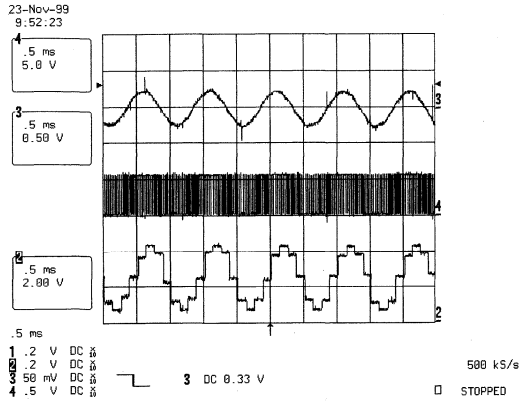

Figure 3c
Input signal: freq.= 1kHz, ampl. of 240mV

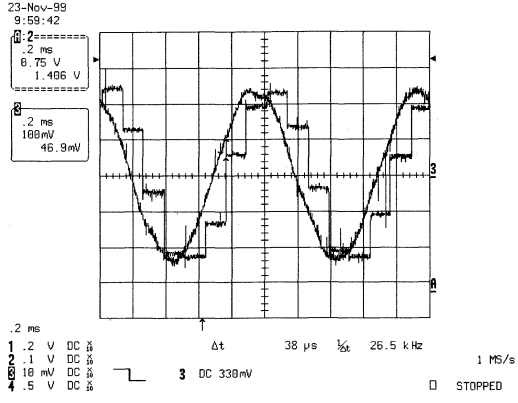

Figure 4
Phase delay measurement for 1kHz signal

5-C. Capture operation

A better understanding of the counter operation and capture units can be achieved by looking at the Fig.5. Both low and large duty ratio cases are presented. One has to keep in mind that the internal counter counts up to *0FFFFh* (16 bits) while the D/A converter allows us to see 12 bits only. As a result, the counter content would look truncated on the scope. This, however, does not affect the meaning of these waveforms. Also, the D/A signals are output during the very fast interrupt routine that occurs during current acquisition (at about 40kHz). Figure 5 presents:

Trace 3 (up) = input signal
Trace 4 (mid) = 2171 to DSP signal (40kHz)
Traces 2,1 (down) = counter at reading time

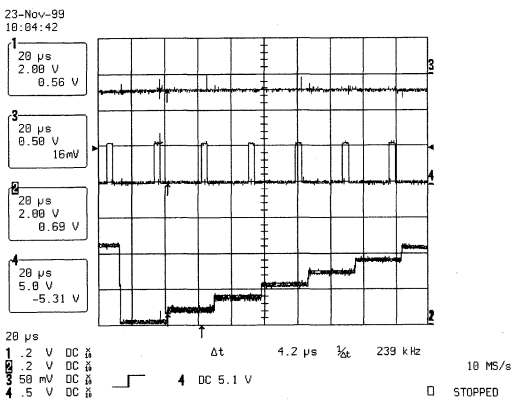

Figure 5a Low duty ratio

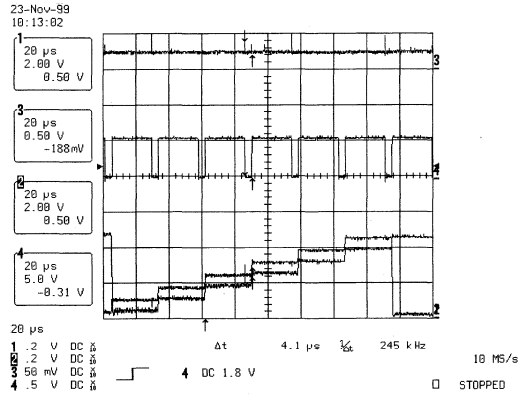

Figure 5b Large duty ratio

5-D Transfer characteristics

Trace 3 (up) = input signal

Trace A (down) = signal reconstructed through the D/A converter

The IN/OUT characteristics are presented at two different frequencies (50Hz and 1kHz) and it is possible to see the effect of sampling the current measurement at the PWM frequency.

The same characteristics are plotted as X-Y functions they are allowing us to observe their linearity.

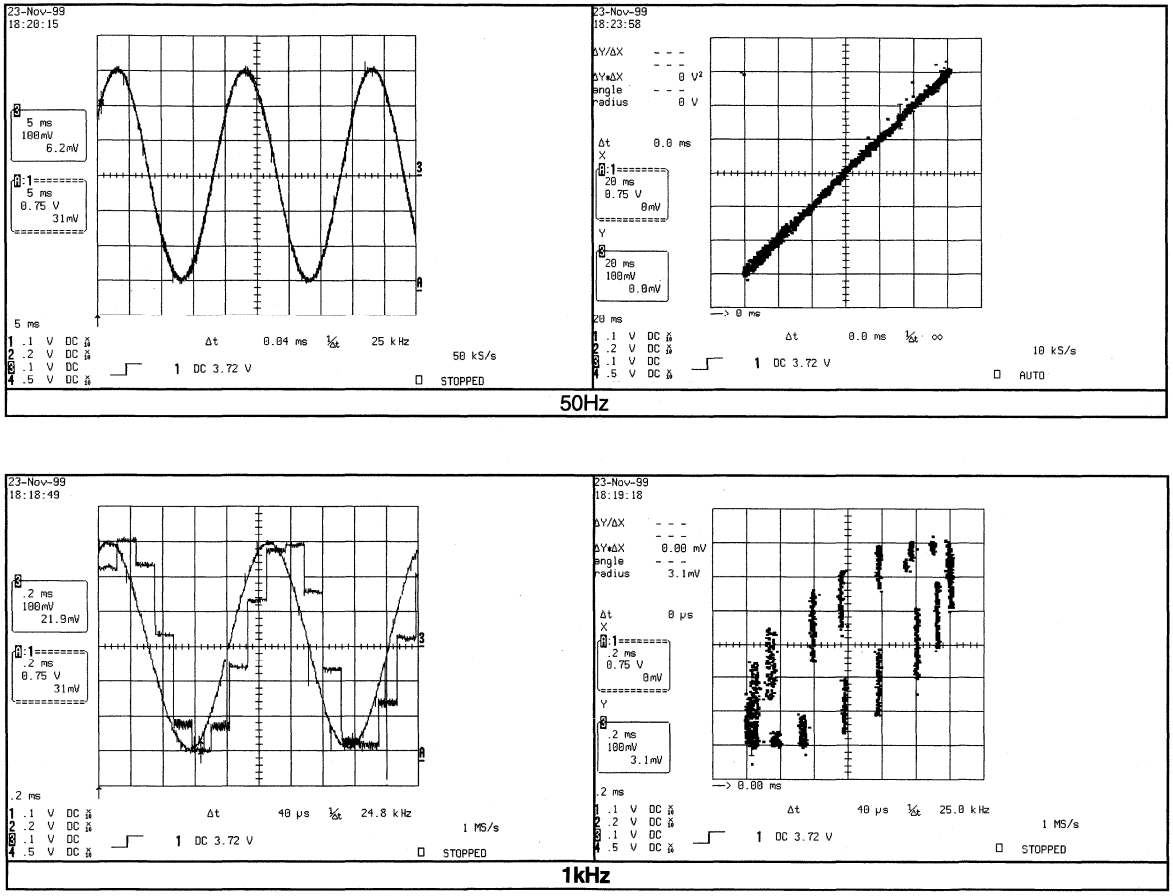

Figure 6 Transfer characteristics

5-E Operation at overvoltage

When the shunt resistor voltage is higher than the allowed maximum voltage at the IC input, IR2171/2172 automatically limits the pulse width and the resulting reconstructed signal is shown in Fig.7.
Trace 2=input voltage
Trace 3=D/A result

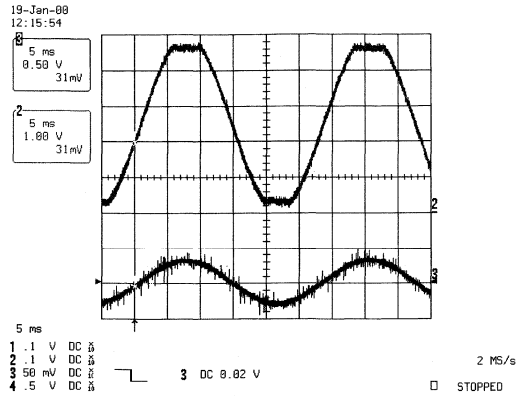

Fig.7 Voltage limitation at IR2172(40kHz). Results for 36Hz and 300mV

6. CONCLUSION

The suitability of IR2171/2172 to the DSP-controlled three-phase AC drives is herein demonstrated and a possible software implementation of the phase current measurement is detailed

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Bootstrap Component Selection For Control IC's

By Jonathan Adams

TOPICS COVERED

Operation Of The Bootstrap Circuit
Factors Affecting The Bootstrap Supply
Calculating The Bootstrap Capacitor Value
Selecting The Bootstrap Diode
Layout Considerations

1. OPERATION OF THE BOOTSTRAP CIRCUIT

The V_{bs} voltage (the voltage difference between the V_b and V_s pins on the control IC) provides the supply to the high side driver circuitry of the control IC's. This supply needs to be in the range of 10-20V to ensure that the Control IC can fully enhance the MOS Gated Transistor (MGT) being driven, some of International Rectifier's Control IC's include undervoltage detection circuits for V_{bs}, to ensure that the IC does not drive the MGT if the Vbs voltage drops below a certain voltage (V_{bsuv} in the datasheet). This prevents the MGT from operating in a high dissipation mode.

This V_{bs} supply voltage is a floating supply that sits on top of the Vs voltage (which in most cases will be a high frequency square wave). There are a number of ways in which the V_{bs} floating supply can be generated, one of these being the bootstrap method described here in this design tip. This method has the advantage of being simple and inexpensive but has some limitations, duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor (long on-times and high duty cycles require a charge pump circuit - see Application Note AN978). The bootstrap supply is formed by a diode and capacitor combination as shown in fig 1).

The operation of the circuit is as follows. When V_s is pulled down to ground (either through the low side FET or the load, depending on the circuit configuration), the bootstrap capacitor (C_{bs}) charges through the bootstrap diode (Dbs) from the 15V Vcc supply. Thus providing a supply to V_{bs}.

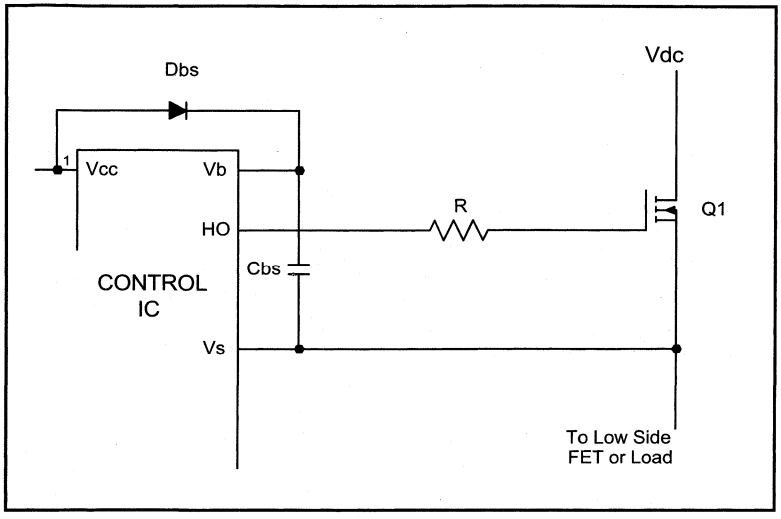


Fig 1) Bootstrap Diode/ Capacitor circuit used with IR Control IC's

2. FACTORS AFFECTING THE BOOTSTRAP SUPPLY

There are five influencing factors which contribute to the supply requirement from the V_{bs} capacitor. These are:

1. Gate Charge required to enhance MGT
2. I_{qbs} - quiescent current for the high side driver circuitry
3. Currents within the level shifter of the control IC
4. MGT gate-source forward leakage current
5. Bootstrap capacitor leakage current

Factor 5 is only relevant if the bootstrap capacitor is an electrolytic capacitor, and can be ignored if other types of capacitor are used. Therefore it is always better to use a non-electrolytic capacitor if possible.

3. CALCULATING THE BOOTSTRAP CAPACITOR VALUE

The following equation details the minimum charge which needs to be supplied by the bootstrap capacitor:

$$Q_{bs} = 2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f} \qquad \text{EQ(1)}$$

where:

Q_g=Gate charge of high side FET f=frequency of operation
$I_{cbs(leak)}$=Bootstrap capacitor leakage current
Q_{ls} = level shift charge required per cycle = 5nC (500V/600V IC's) or 20nC (1200V IC's)

The bootstrap capacitor must be able to supply this charge, and retain its full voltage, otherwise there will be a significant amount of ripple on the V_{bs} voltage, which could fall below the V_{bsuv} undervoltage

lockout, and cause the HO output to stop functioning. Therefore the charge in the C_{bs} capacitor must be a minimum of twice the above value. The minimum capacitor value can be calculated from the equation below.

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS}} \qquad \text{EQ(2)}$$

Where:

V_f= Forward voltage drop across the bootstrap diode

V_{LS}= Voltage drop across the low side FET

(or load for a high side driver)

IMPORTANT NOTE: The C_{bs} Capacitor value obtained from the above equation EQ(2) is the absolute minimum required, however due to the nature of the bootstrap circuit operation, a low value capacitor can lead to overcharging, which could in turn damage the IC. Therefore to minimize the risk of overcharging and further reduce ripple on the V_{bs} voltage the C_{bs} value obtained from the above equation should be should be multiplied by a factor of 15 (rule of thumb).

The C_{bs} capacitor only charges when the high side device is off, and the Vs voltage is pulled down to ground. Therefore the on time of the low side switch (or the off time of the high side switch for a high side driver) must be sufficient to ensure that the charge drawn from the C_{bs} capacitor by the high side driver, can be fully replenished. Hence there is inherently a minimum on time of the low side switch (or off time of the high side switch in a high side driver). Also in a high side switch configuration where the load is part of the charge path, the impedance of the load can have a significant effect on the charging of the C_{bs} bootstrap capacitor - if the impedance is too high the capacitor will not be able to charge properly, and a charge pump circuit may be required (see Application Note AN978).

4. SELECTING THE BOOTSTRAP DIODE

The bootstrap diode (D_{bs}) needs to be able to block the full power rail voltage, which is seen when the high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the Vcc supply, and similarly the high temperature reverse leakage current would be important if the capacitor has to store charge for long periods of time. The current rating of the diode is the product of the charge calculated from equation EQ(1) and the switching frequency.

Therefore:

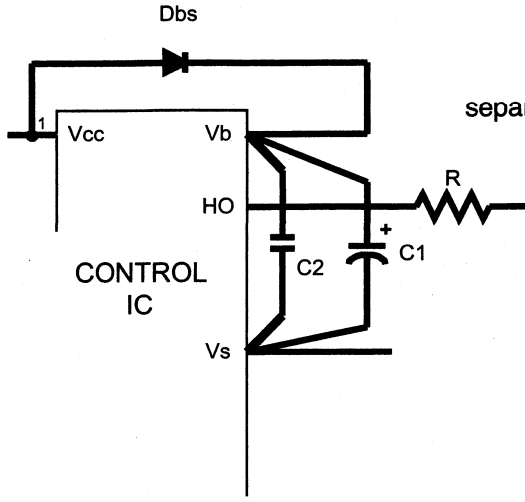
Diode Characteristics

V_{RRM} = Power rail voltage
max t_{rr} = 100ns
I_F = Q_{bs} x f

5. LAYOUT CONSIDERATIONS

The Bootstrap capacitor should always be placed as close to the pins of the IC as possible (as shown in Fig 2 on the left).

At least one low ESR capacitor should be de-coupling, e.g. a to the IC would be electrolytic capacitor capacitor. If the either a ceramic or should be sufficient decoupling.



used to provide good local separate ceramic capacitor close essential if an aluminum is used for the bootstrap bootstrap capacitor is tantalum type, this in itself as the local

Fig 2) Recommended layout of the Bootstrap Components

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Managing Transients in Control IC Driven Power Stages

By Chris Chey and John Parry

Topics covered:

1. CONTROL IC PRODUCT RANGE

International Rectifier offers a broad range of control ICs from single channel to complete three-phase bridge drivers. All types employ high-integrity level shifting techniques to simplify control of power transistors from logic circuits. Our latest products further enhance this capability to drive power switches relatively displaced by up to 1200V.

As leading edge performance demands switching more current at ever higher speeds, the unwanted effects of parasitics are magnified and warrant heightened attention. The aim here is to locate their source, quantify the immunity of the IC against a potentially troublesome effect and finally, show how to maximize the margin between the two.

2. PARASITIC ELEMENTS OF THE BRIDGE CIRCUIT

The circuit shown in figure 1 depicts a typical application in which two power MOSFETs are driven by a control IC in a half bridge configuration. Unwanted inductance in the power circuit from die bonding in the transistors, pinning and PCB tracks are lumped together and arbitrarily labeled LS1,2 and LD1,2.

Further parasitics will exist in the gate drive circuit and these should also be considered during circuit layout but for now, we will focus on the bridge itself as the highest currents and di/dt will occur here. During switching, rapidly changing bridge current induces voltage transients across all parasitics shown. Left unchecked, these transients may couple into other circuits causing noise problems, increased switch dissipation or even IC damage in extreme cases.

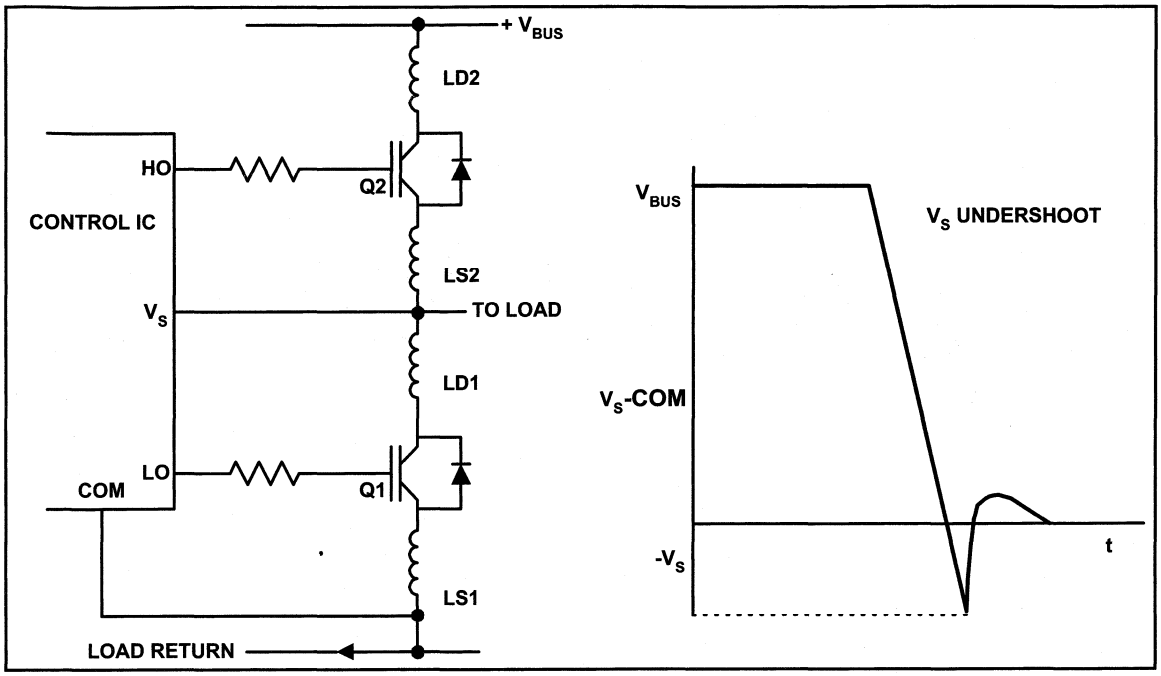

Figure 1. Parasitic Elements of the Half Bridge

3. V_S UNDERSHOOT: CAUSE

Of the problems caused by parasitics, one of the main issues for control ICs is a tendency for the V_S node to undershoot ground following switching events. Conversely, overshoot does not generally cause a problem due to the high differential voltage capability of International Rectifier's proven HVIC process.

With inductive loading of the bridge, high side transistor turn-off causes load current to suddenly flow in the low side free-wheeling diode. On top of the 'slack' from diode turn-on delay and forward voltage drop, stray inductance LS1+LD1 contribute to undershoot of the Vs node beyond ground, as shown in the graph of figure 1. If the load circuit does not totally self-commutate in the dead-time (both transistors off) V_S undershoot or ringing may occur when the low side device is hard switched.

4. V_S UNDERSHOOT: EFFECTS ON THE CONTROL IC

International Rectifier control ICs are guaranteed completely immune to V_S undershoot of at least 5V, measured with respect to COM. If undershoot exceeds this level, the high side output will temporarily latch in its current state. Provided V_S remains within absolute maximum limits the IC will not suffer damage, however the high-side output buffer will not respond to input transitions while undershoot persists beyond 5V. This mode should be noted but proves trivial in most applications, as the high-side is not usually required to change state immediately following a switching event.

5. AVOIDING LATCH-UP

The parasitic diode structure for a typical control IC is shown in appendix 1. - As with any CMOS device, driving any of these diodes into forward conduction or reverse breakdown may cause parasitic SCR latch-up. The ultimate outcome of latch-up often defies prediction and can range from temporary erratic operation to total device failure.

The control IC may also be damaged indirectly by a chain of events following initial overstress. By way of example, latch-up could conceivably result in both output drivers assuming a high state, causing cross-conduction followed by switch failure and finally catastrophic damage to the IC. This failure mode should be considered a possible root cause if power transistors and/or control IC are destroyed in the application.

The following theoretical extremes can be used to help explain the relationship between excessive V_S undershoot and the resulting latch-up mechanism.

In the first case an 'ideal bootstrap' circuit is used in which V_{CC} is driven from a zero-ohm supply with an ideal diode feeding V_B. Undershoot now sums with Vcc causing the bootstrap capacitor to overcharge as shown in figure 2. By way of example, if V_{CC}=15V then V_S undershoot in excess of 10V forces the floating supply above 25V, risking breakdown in diode D1 and subsequent latch-up. Suppose now that the bootstrap supply is replaced with the ideal floating supply of figure 3 such that V_{BS} is fixed under all circumstances. Note that using a low impedance auxiliary supply in place of a bootstrap circuit can approach this situation.

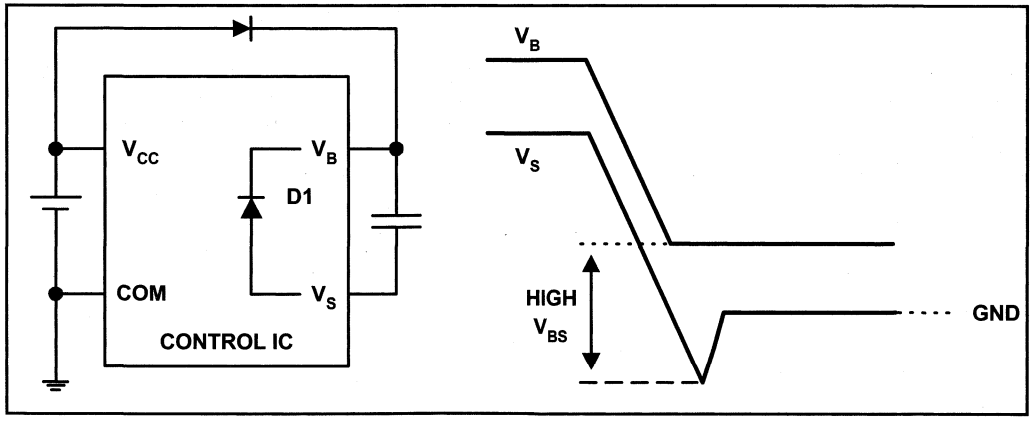

Figure 2. Case 1: Ideal Bootstrap Circuit

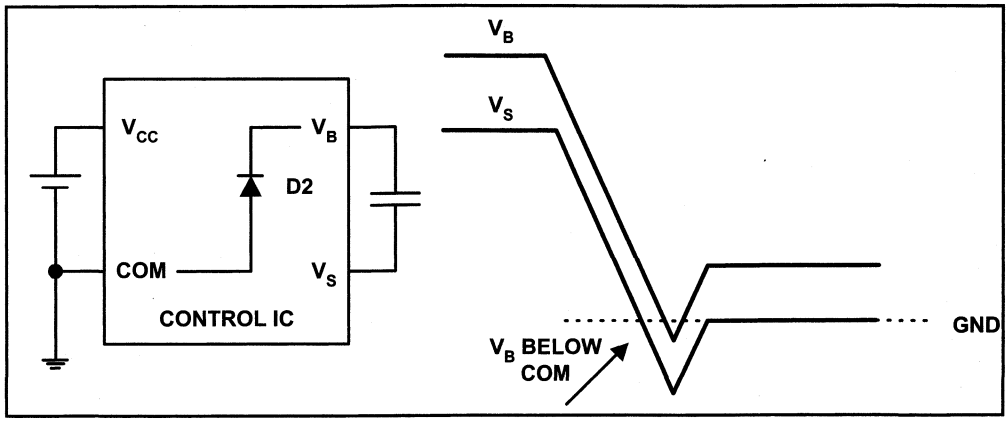

Figure 3. Case 2: Ideal Floating Supply

This time, latch-up risk appears if V_S undershoot exceeds V_{BS}, since parasitic diode D2 will ultimately enter conduction.

A practical circuit is likely to fall somewhere between these two extremes, resulting in both a small increase of V_{BS} and some V_B droop below V_{CC} as depicted by Figure 4.

Exactly which of the two extremes is prevalent can be checked as follows.

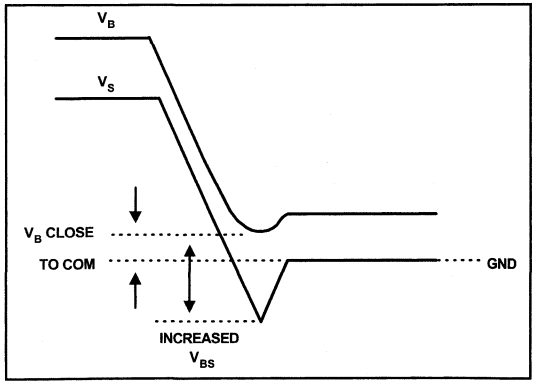

Figure 4. Typical Response

6. MONITOR AND VERIFY

The signals listed below should be observed both in normal operation and during high-stress events such as short circuit or over current shutdown, when di/dt is highest. Readings should always be taken directly across IC pins as shown in figure 5, so that contributions from parasitics in the drive coupling are included in the measurement.

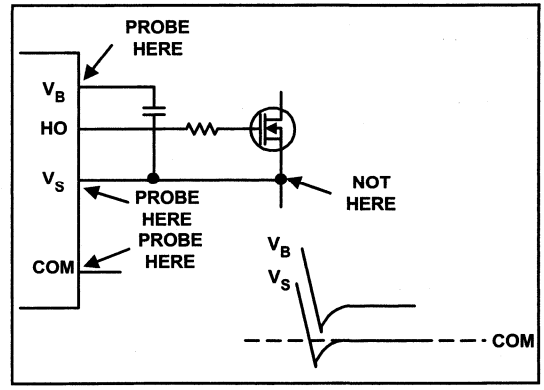

Figure 5. Measurement Points

Measurements to verify undershoot severity

(1) High side offset with respect to common; V_S-COM
(2) The floating supply; V_B - V_S

Most bridge circuits employ a bus of several hundred volts which means selecting an insensitive Y-axis scale to prevent distortion from saturation of the input amplifier. This can make the comparatively small Vs undershoot difficult to quantify.
For best resolution, check your oscilloscope manual and then select the highest useable sensitivity level.

For the second measurement, the signal of interest is permanently superimposed on the changing bridge voltage. The oscilloscope may be floated with a transformer, but this method is discouraged because capacitive loading can alter circuit performance and sometimes mask underlying problems by inadvertently reducing dv/dt.

A high-bandwidth differential voltage probe (or an isolated differential-input oscilloscope) can give good results here, allowing other ground referenced signals to be viewed at the same time. However, be aware of propagation delay mismatch between differential and conventional probes when comparing relative event times.

Always measure the noise floor prior to making measurements. Common-mode noise on high side referenced signals (Vb,HO) can be observed by joining probe tip and ground lead directly to the Vs node.

Do not assume that 'low-side' referenced signals are free from common-mode noise. Measure the noise floor by joining probe tip and ground lead together at the COM node.

7. GENERAL RECOMMENDATIONS

The following guidelines represent good practice in control IC circuits and warrant attention regardless of the observed latch-up safety margin. Design tip DT94-15 'Design Check List for IR21xx MGDs' may be consulted for pictorial representation of the suggestions listed below.

Minimize the parasitics of figure 1

1a. Use thick, direct tracks between switches with no loops or deviation.
1b. Avoid interconnect links. These can add significant inductance.
1c. Reduce the effect of lead-inductance by lowering package height above the PCB.
1d. Consider co-locating both power switches to reduce track lengths.

Reduce control IC exposure.

2a. Connect V_S and COM as shown in figure 6.
2b. Minimize parasitics in the gate drive circuit by using short, direct tracks.
2c. Locate the control IC as close as possible to the power switches.

Improve local decoupling.

3a. Increase the bootstrap capacitor (Cb) value using at least one low-ESR capacitor. This will reduce overcharging from severe Vs undershoot. See Design Tip DT98-2 for more information
3b. Use a second low-ESR capacitor from Vcc to COM. As this capacitor supports both the low-side output buffer and bootstrap recharge, we recommend a value at least ten times higher than Cb.
3c. Connect decoupling capacitors directly across appropriate pins as shown in figure 7.

3d. If a resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM, especially during start-up and extremes of fre quency and duty cycle.

Granted proper application of the above guidelines, the effects of V_S undershoot will be minimized at source. If the level of undershoot is still considered too high, then some reduction of dv/dt may be necessary.

External snubbing and/or increasing gate drive resistance may be used to trade efficiency for lower switching rate. If the system will not tolerate this, then fast anti-parallel clamping diodes may be considered appropriate. HEXFRED diodes are ideal for this purpose.

8. BOOSTING V_S UNDERSHOOT IMMUNITY.

If the key signals measured fall within specified limits under worst case conditions, then no further action should be necessary. However, in very noisy environments, where Vs undershoot remains excessive despite the measures above, then further steps may be taken to increase control IC tolerance. We recommend two different methods for improving undershoot immunity.

Method A:
A resistor between the V_S pin and the bridge center may be used to limit the current flow into the Vs pin during undershoot. This method is viable for resistor values of around 5 Ohms or less.

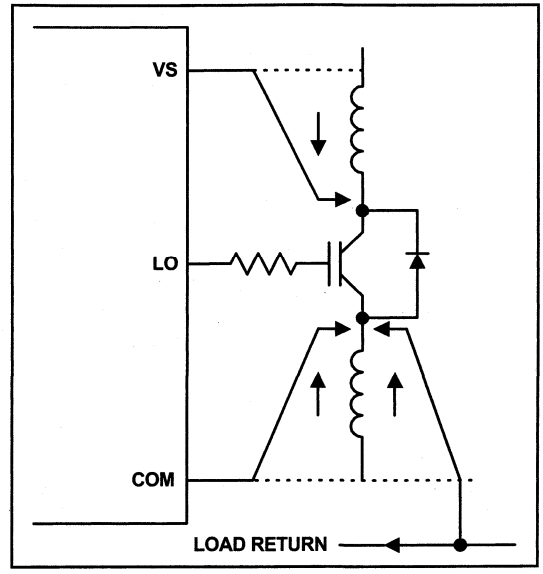

Figure 6. Bypass Parasitics

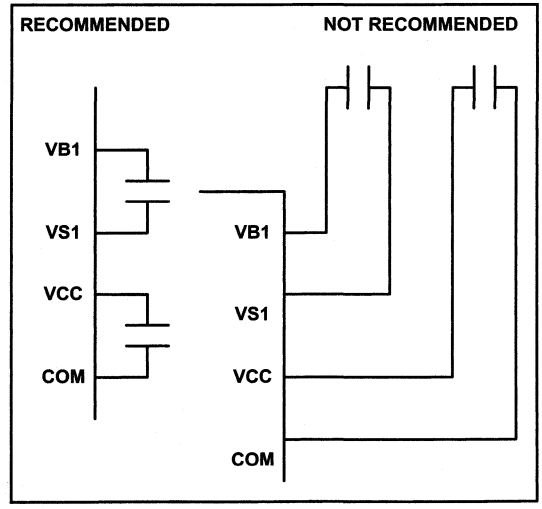

Figure 7. Decoupling Capacitor Location

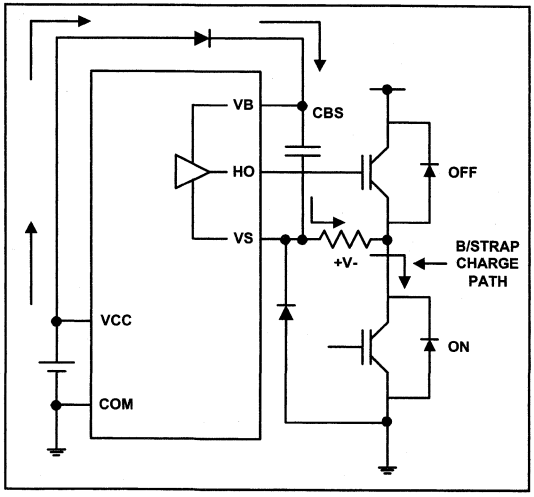

Figure 8. Boosting Immunity Method A

Since the bootstrap capacitor charges through this resistor, as shown in figure 8, inadvertent shoot-through may occur at start-up if the value is too high. If there is a series gate resistor, this should be reduced in value so the nett gate resistance of both high and low side transistors remains equal.

Method B:

By way of an alternative approach, we also recommend the insertion of a single resistor between COM and the low side source or emitter as depicted by figure 9. Since the bootstrap capacitor is not charged through the resistor, this method grants flexibility to choose a higher resistance and afford greater protection to the control IC.

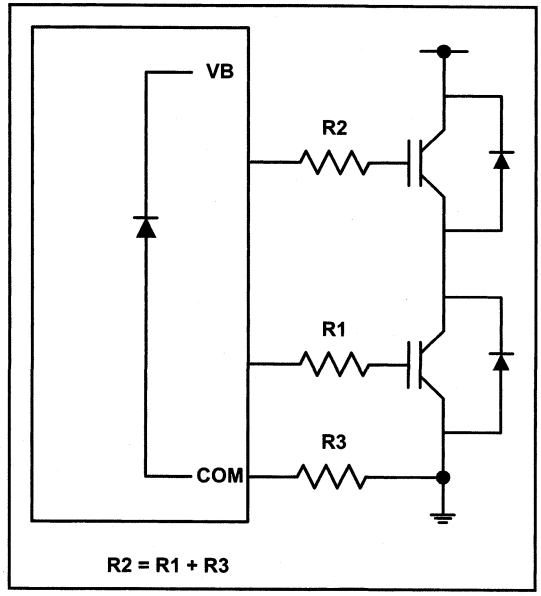

Figure 9. Boosting Immunity Method B

A resistor in this location has the effect of limiting peak current flow in the 600V diode D2 shown in figure 3. Again, drive symmetry requires that the total resistance in both gate drive circuits be equal, so the low-side gate resistor should be slightly reduced to accomplish this.

Note:

When using control ICs which do not have a separate logic ground, i.e. those which share COM for both input and output ground references, either of the two methods discussed may be applied. However, care should be taken to ensure that logic inputs fall within the permitted levels.

9. APPENDIX 1. IR2110 PARASITIC DIODE STRUCTURE

The parasitic diode structure of the IR2110 control IC is shown in Figure 10. This is, in essence, a pictorial representation of our Absolute Maximum Ratings table.

The IR2110 has separate logic and output supply rails, however, these rails are combined in some control IC types due to pinning restrictions.

Further details on the parasitic diode structure and latch-up mechanism may be found in design tip DT94-9A, 'Maximizing Latch Immunity of the IR2151 and IR2152 In Ballast Applications'

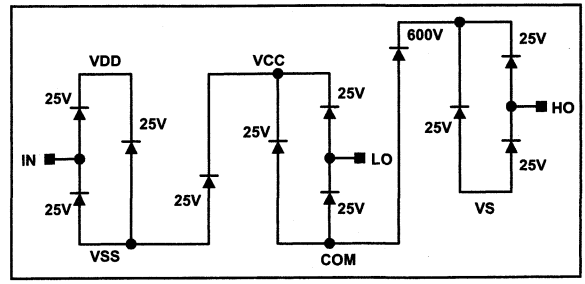

Figure 10. IR2110 Parasitic Diode Structure

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